Product Specification

PE9301

3500 MHz Low Power UltraCMOS™ Divide-by-2 Prescaler
Rad-hard for Space Applications

Features

- High-frequency operation: 1500 MHz to 3500 MHz
- Fixed divide ratio of 2
- Low-power operation: 13 mA typical @ 3 V across frequency
- Small package: 8-lead SOIC
- Low Cost

Product Description

The PE9301 is a high performance monolithic UltraCMOS™ prescaler with a fixed divide ratio of 2. Its operating frequency range is 1500 MHz to 3500 MHz. The PE9301 operates on a nominal 3 V supply and draws only 13 mA. It is packaged in a small 8-lead CSOIC and is ideal for Space microwave PLL synthesis solutions.

The PE9301 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

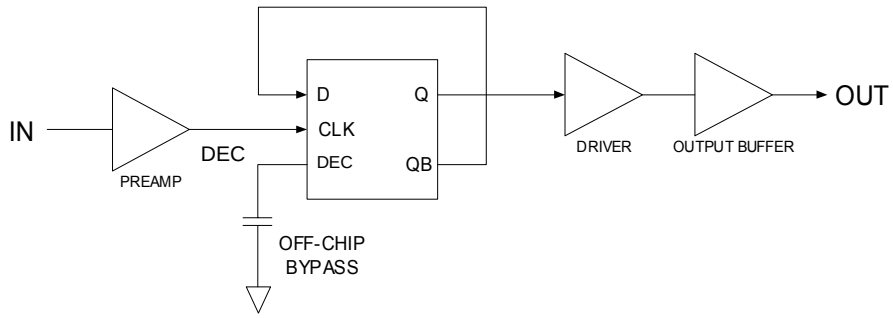


Figure 2. Package Type

8-lead CSOIC

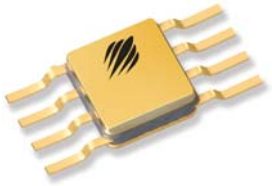


Table 1. Electrical Specifications @ +25 °C ($Z_S = Z_L = 50\ \Omega$)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Voltage		2.85	3.0	3.15	V
Supply Current			13	15	mA
Input Frequency (F_{IN})	P_{IN} = -5 dBm min.	1.5		3.5	GHz
Input Power (P_{IN})	F_{IN} = 1.5 to 3.5 GHz	-5		+5	dBm
Output Power		-10			dBm

Figure 3. Pin Configuration

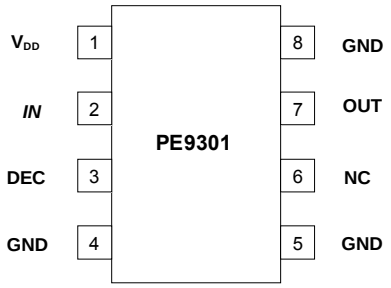


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Power supply pin. Bypassing is required.
2	IN	Input signal pin. Should be coupled with a capacitor (eg 15 pF).
3	DEC	Power supply decoupling pin. Place a capacitor as close as possible and connect directly to the ground plane.
4	GND	Ground pin. Ground pattern on the board should be as wide as possible to reduce ground impedance.
5	GND	Ground pin.
6	NC	No connection. This pin should be left open.
7	OUT	Divided frequency output pin. This pin should be coupled with a capacitor (eg 47 pF).
8	GND	Ground Pin.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Supply voltage		4.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
VESD	ESD voltage (Human Body Model)	250		V

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The PE9301 takes an input signal frequency from between 1.5 GHz to 3.5 GHz and produces an output signal frequency half that of the supplied input. In order for the prescaler to work properly, several conditions need to be adhered to. It is crucial that pin 3 be supplied with a bypass capacitor to ground. In addition, the input and output signals (pins 2 & 7, respectively) need to be AC coupled via an external capacitor as shown in Figure 5.

The ground pattern on the board should be made as wide as possible to minimize ground impedance.

Figure 4. Test Circuit Block Diagram

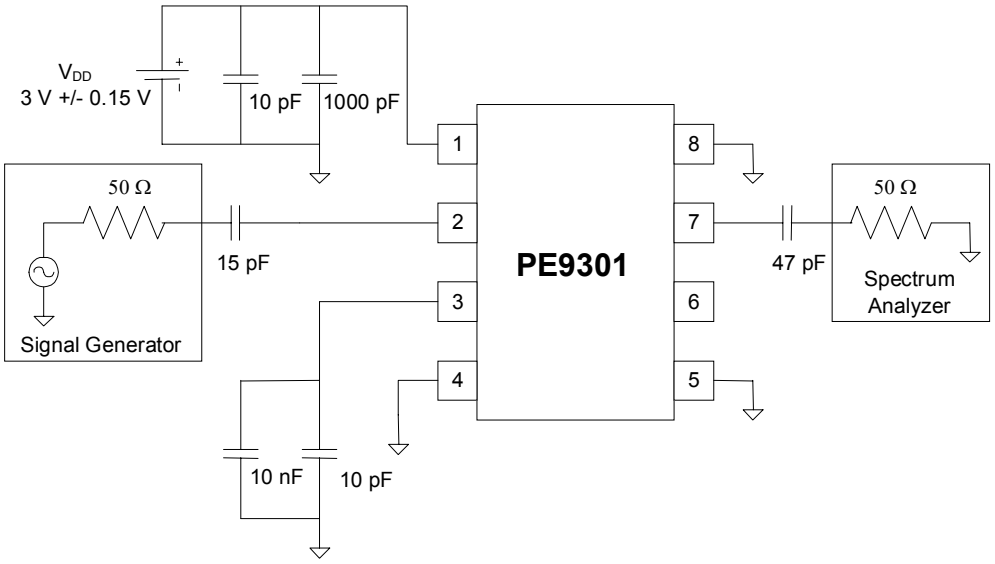
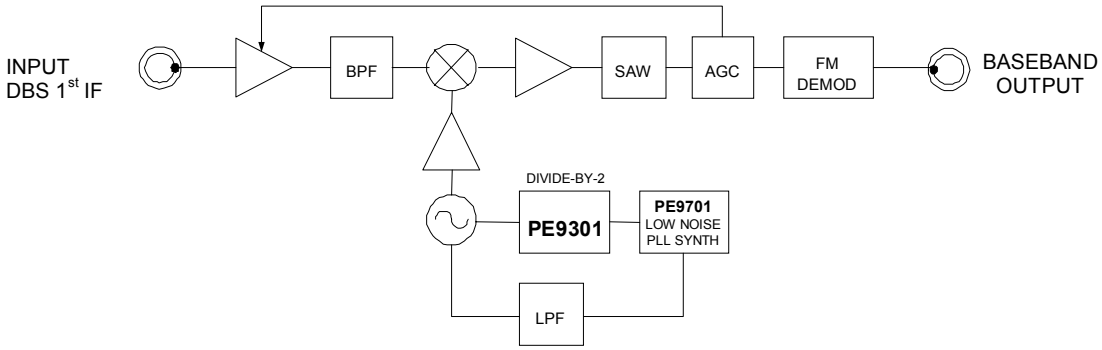


Figure 5. High Frequency System Application

The wideband frequency of operation of the PE9301 makes it an ideal part for use in a DBS down converter system.



Evaluation Kit Operation

The Ceramic SOIC Prescaler Evaluation Board was designed to help customers evaluate the *PE9301* divide-by-2 prescaler. On this board, the device input (pin 2) is connected to the SMA connector J1 through a 50 Ω transmission line. A series capacitor (C3) provides the necessary DC block for the device input. A value of 1000 pF was used for the evaluation board; other applications may require a different value. It is also possible to place a 0 Ω resistor in this location for very low frequency applications.

The device output (pin 7) is connected to SMA connector J3 through a 50 Ω transmission line. A series capacitor (C1) provides the necessary DC block for the device output. This capacitor value must be chosen to have a low impedance at the desired output frequency of the device. A value of 1000 pF was chosen for the evaluation board.

The board is constructed of a two-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide above ground plane model with trace width of 0.030", trace gaps of 0.0061", dielectric thickness of 0.028", metal thickness of 0.0014", and ε_r of 4.6. Note that the predominate mode of these transmission lines is coplanar waveguide.

J2 provides DC power to the device via pin 1. Two decoupling capacitors (C2=100 pF, C10=1000 pF) are included on this trace. It is the responsibility of the customer to determine proper supply decoupling for their design application.

Figure 6. Evaluation Board Layout
Peregrine specification 101/0034

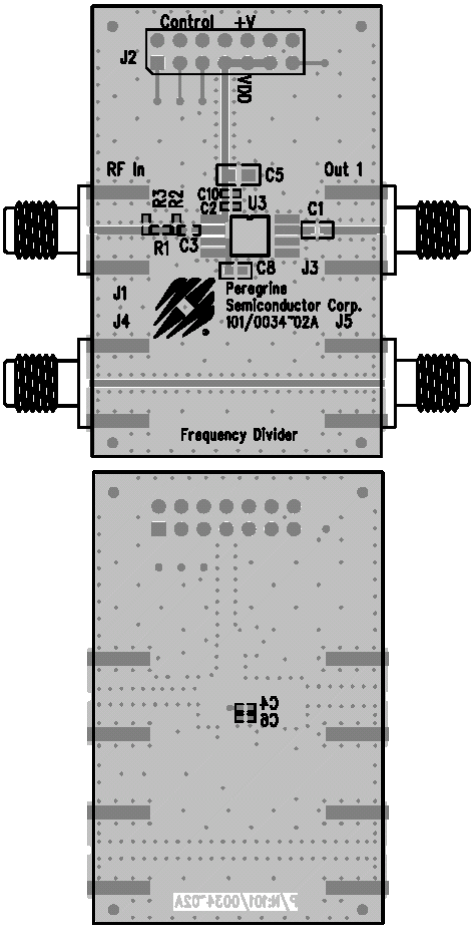
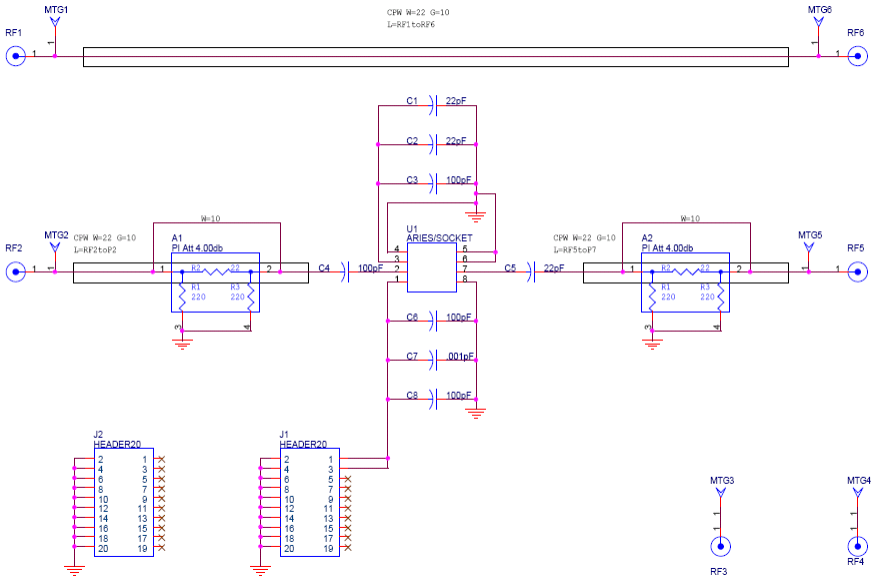


Figure 7. Evaluation Board Schematic
Peregrine specification 102/0062



Typical Performance Data @ +25 °C

Figure 8. Typical Input Sensitivity

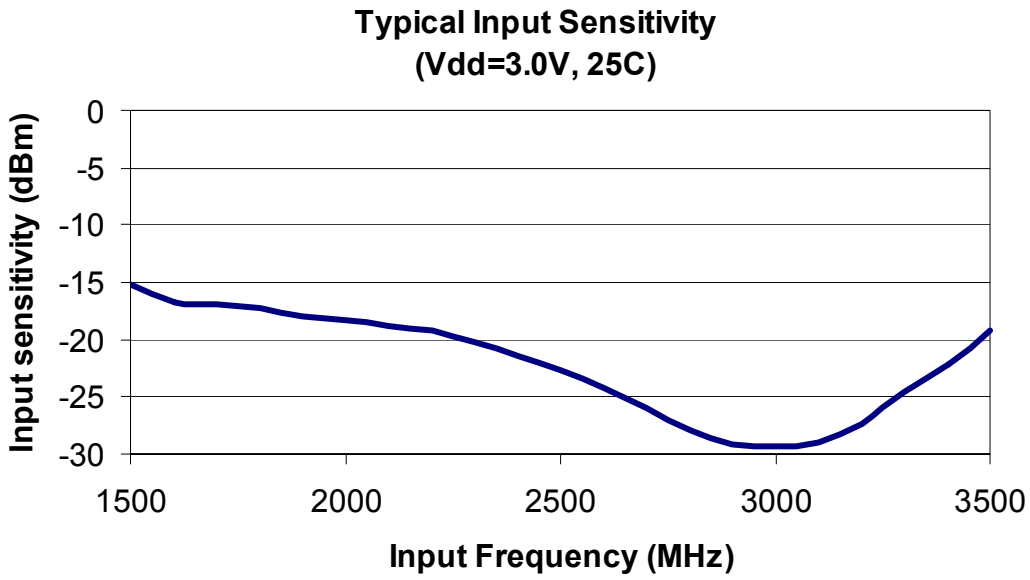


Figure 9. Typical Output Power

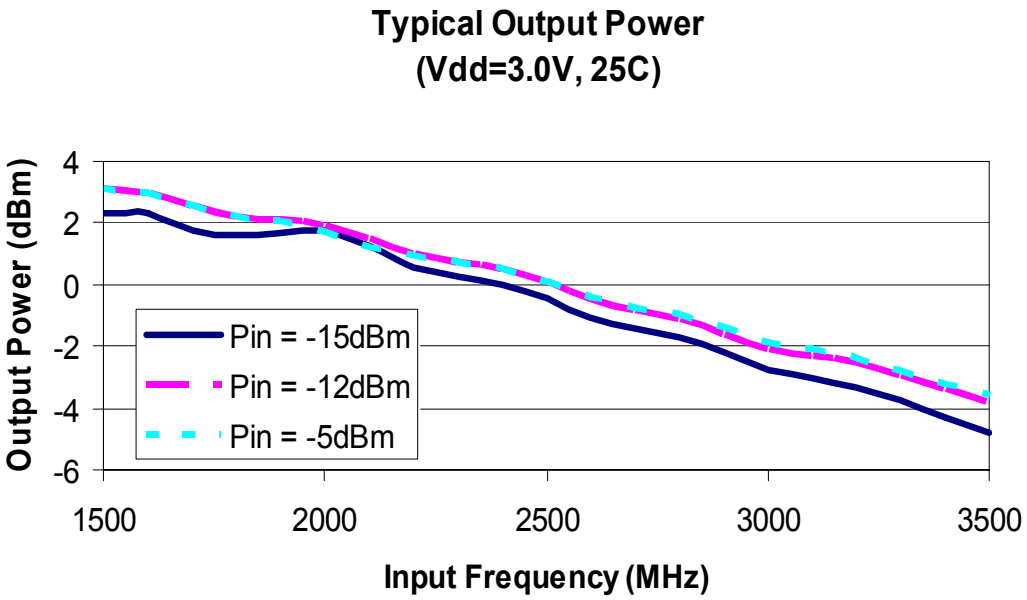


Figure 10. Package Drawing

8-lead CSOIC

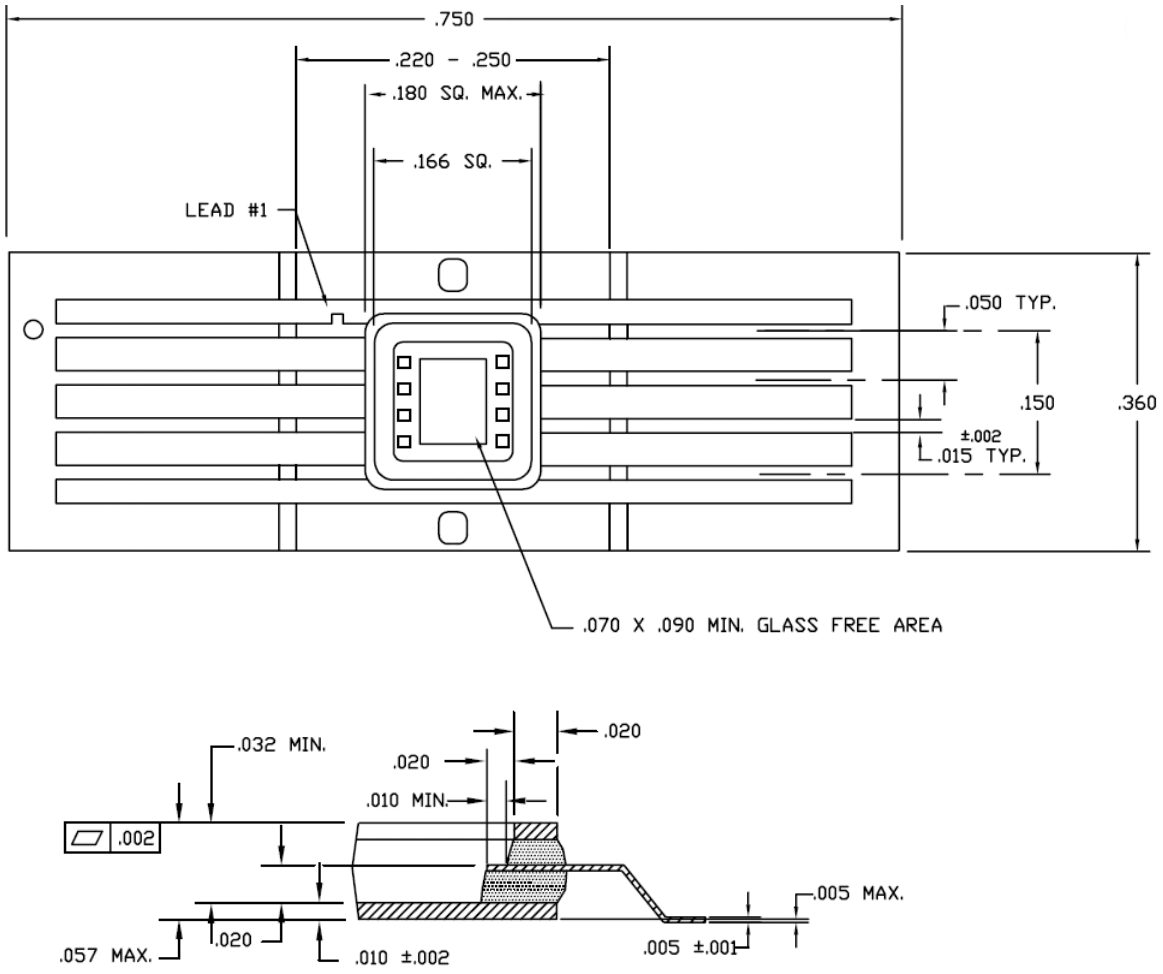


Table 4. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
9301-01	PE9301ES	PE9301-08CFP-50B Engineering Samples	8-lead CSOIC	50 / Tray
9301-11	PE9301	PE9301-08CFP-50B Production Units	8-lead CSOIC	50 / Tray
9301-00	PE9301-EK	PE9301 Evaluation Kit	Evaluation Board	1 / Box

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Data Sheet Identification

Advance Information

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Preliminary Specification

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Product Specification

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