PLL602-89D

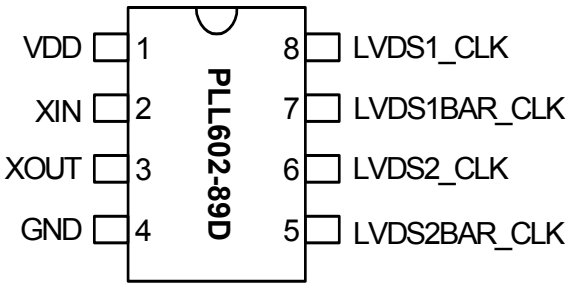
12-27 MHz XO IC with 2 Pairs of LVDS Outputs

FEATURES

- Low jitter XO for the 12MHz to 27MHz range.
- Integrated crystal load capacitor: no external load capacitor required.
- 2 pairs of LVDS outputs.
- 12-27 MHz fundamental crystal input.
- Low jitter (RMS): 2.5 ps period jitter (1 sigma).
- 2.5V to 3.3V operation.
- Available in 8-Pin SOIC package.

PIN CONFIGURATION

(Top View)

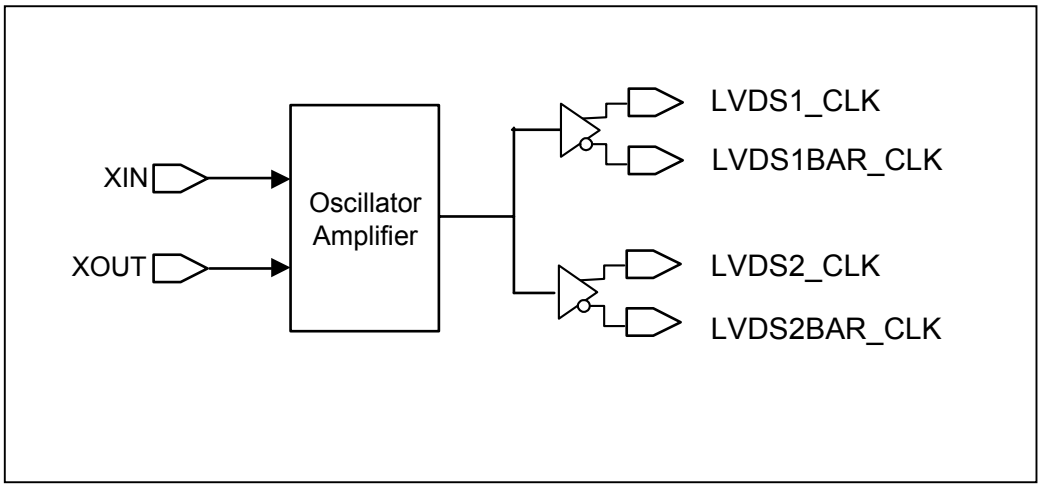


(8 pin SOIC)

DESCRIPTION

The PLL602-89D is a high performance multiple output XO IC chip. It provides 2 pairs of LVDS outputs. The chip combines a crystal oscillator (XO) with a multiple-output buffer. It accepts a low cost fundamental parallel resonant mode crystal from 12MHz to 27MHz, which is reproduced at the outputs. The very low jitter (2.5 ps RMS period jitter) makes this chip ideal for data and telecommunication applications.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Pin Number	Type	Description
VDD	1	P	Power supply.
XIN	2	I	Crystal input. This is the input of the crystal oscillator circuitry. The crystal should be mounted as close to the IC as possible, with minimum parasitic capacitance.
XOUT	3	I	Crystal output. This is the output of the crystal oscillator circuitry. The crystal should be mounted as close to the IC as possible, with minimum parasitic capacitance.
GND	4	P	Ground.
LVDSBAR_CLK	5,7	O	LVDS complementary output.
LVDS_CLK	6,8	O	LVDS output.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		27	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$			21.5		pF
Recommended ESR	R_E				30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	LVDS outputs loaded with 100Ω	Fout = 12 MHz		15	20	mA
			Fout = 25 MHz		20	25	
Operating Voltage	V_{DD}			2.25		3.63	V
Short Circuit Current					±50		mA

4. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			12		27	MHz
Output Clock Rise Time		0.8V ~ 2.0V with 10 pF load			1.5	ns
		0.3V ~ 3.0V with 15 pF load		2	5	
Output Clock Fall Time		2.0V ~ 0.8V with 10 pF load			1.5	
		3.0V ~ 0.3V with 15pF load		2	5	
Output Clock Duty Cycle		Measured @ 1.25 V (LVDS)	45	50	55	%
		Measured @ VDD/2 (CMOS)	45	50	55	

5. Jitter Specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND.	25MHz		2.5	4	ps
Peak to Peak jitter	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	25MHz		18	30	ps

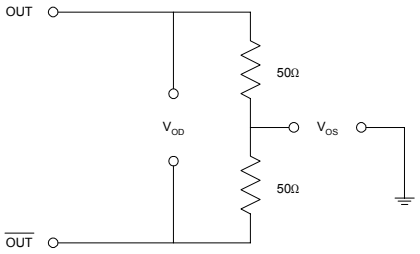
6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

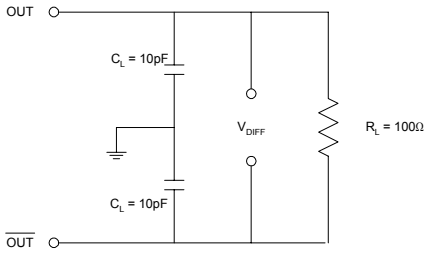
7. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

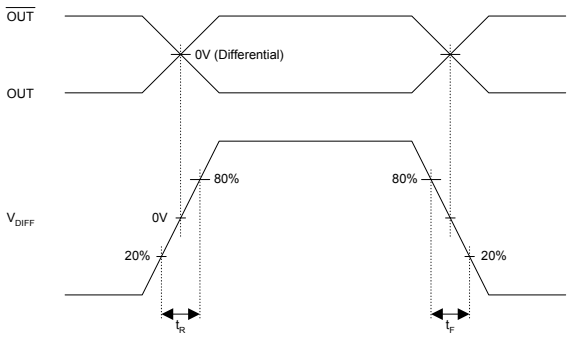
LVDS Levels Test Circuit



LVDS Switching Test Circuit



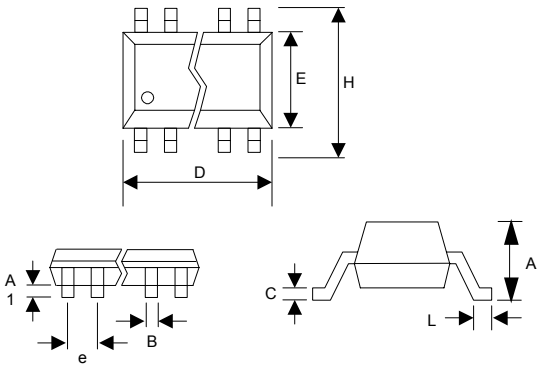
LVDS Transistion Time Waveform



PACKAGE INFORMATION

8 PIN SOIC (mm)

	Narrow SOIC	
Symbol	Min.	Max.
A	1.47	1.73
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	4.95
E	3.80	4.00
H	5.80	6.20
L	0.38	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL602-89D S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

PACKAGE TYPE
S=SOIC

Order Number	Marking	Package Option
PLL602-89DSC-R	P602-89D SC	SOIC - Tape and Reel
PLL602-89DSC	P602-89D SC	SOIC - Tube