NUP4201DR2

Low Capacitance Surface Mount TVS for High-Speed Data Interfaces

The NUP4201DR2 transient voltage suppressor is designed to protect equipment attached to high speed communication lines from ESD, EFT, and lightning.

Features:

- SO−8 Package
- Peak Power − 500 Watts 8 x 20 μS
- ESD Rating:
  IEC 61000−4−2 (ESD) 15 kV (air) 8 kV (contact)
  IEC 61000−4−4 (EFT) 40 A (5/50 ns)
  IEC 61000−4−5 (lightning) 23 (8/20 μs)
- UL Flammability Rating of 94V−0

Typical Applications:

- High Speed Communication Line Protection
- USB Power and Data Line Protection
- Video Line Protection
- Base Stations
- HDSL, IDSL Secondary IC Side Protection
- Microcontroller Input Protection

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μS @ T_A = 25°C (Note 1)	P_{pk}	500	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum 10 Seconds Duration	T_L	260	°C

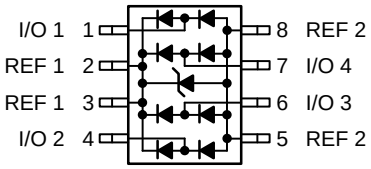
1. Non−repetitive current pulse 8 x 20 μS exponential decay waveform

ON Semiconductor®

http://onsemi.com

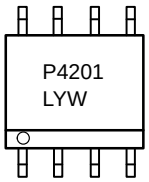
SO−8 LOW CAPACITANCE VOLTAGE SUPPRESSOR 500 WATTS PEAK POWER 6 VOLTS

PIN CONFIGURATION AND SCHEMATIC



SO−8
CASE 751
PLASTIC

MARKING DIAGRAM



P4201 = Device Code
L = Location Code
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NUP4201DR2	SO−8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

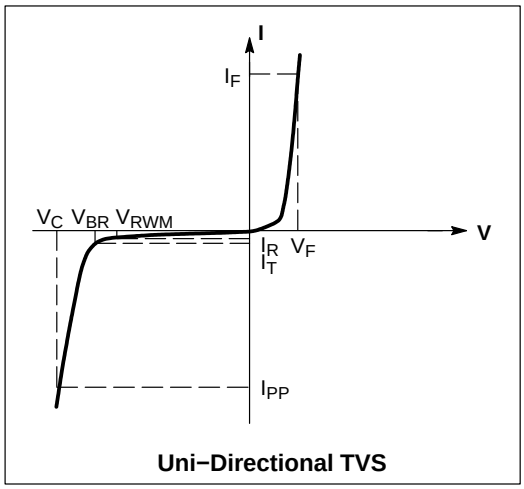
Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	6.0	–	–	V
Reverse Leakage Current @ V_{RWM} = 5.0 Volts	I_R	N/A	–	10	μA
Maximum Clamping Voltage @ I_{PP} = 1.0 A, 8 x 20 μS	V_C	N/A	–	9.8	V
Maximum Clamping Voltage @ I_{PP} = 10 A, 8 x 20 μS	V_C	N/A	–	12	V
Between I/O Pins and Ground @ DC Bias = 0 V, 1.0 MHz	Capacitance	–	5.0	10	pF
Between I/O Pins and I/O @ DC Bias = 0 V, 1.0 MHz	Capacitance	–	2.5	5.0	pF

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

UNIDIRECTIONAL (Circuit tied to Pins 1 and 3 or 2 and 3)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
ΘV_{BR}	Maximum Temperature Coefficient of V_{BR}
I_F	Forward Current
V_F	Forward Voltage @ I_F
Z_{ZT}	Maximum Zener Impedance @ I_{ZT}
I_{ZK}	Reverse Current
Z_{ZK}	Maximum Zener Impedance @ I_{ZK}



Uni−Directional TVS

TYPICAL CHARACTERISTICS

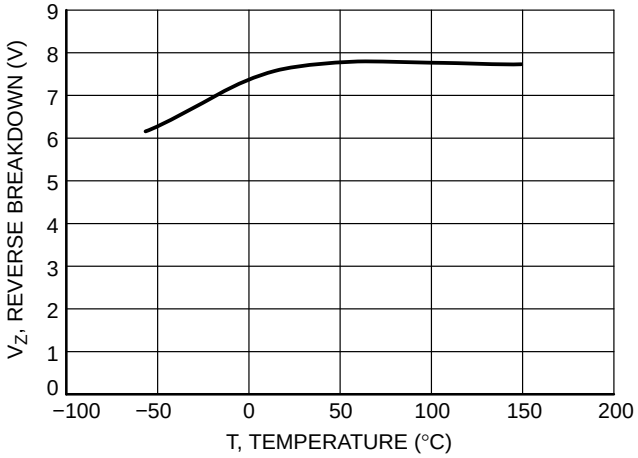


Figure 1. Reverse Breakdown versus Temperature

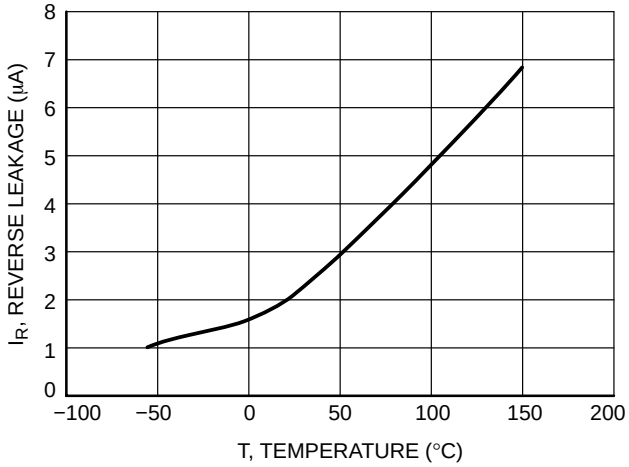


Figure 2. Reverse Leakage versus Temperature

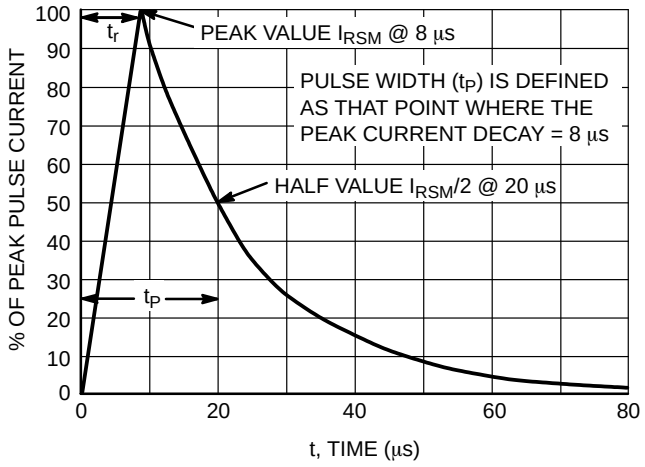


Figure 3. 8 × 20 μs Pulse Waveform

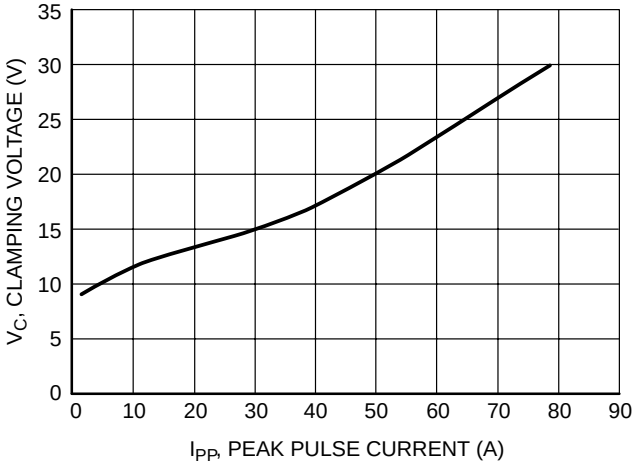


Figure 4. Clamping Voltage versus Peak Pulse Current

APPLICATIONS INFORMATION

The new NUP4201DR2 device is a low capacitance TVS Diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD conditions or transient voltage conditions. Because of its low capacitance array configuration, it can be used in high speed I/O data lines.

The integrated design of the NUP4201DR2 device offers surge rated, low capacitance steering diodes and a TVS diode integrated in a single package (SO−8). If a transient condition occurs, the steering diodes will drive the transient condition to the positive polarity of the power supply or to ground. The TVS device protects the power line against over−voltage conditions to avoid damage in any downstream components.

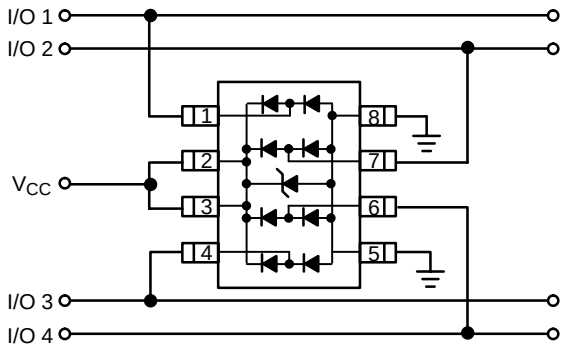
NUP4201DR2 Device's Configurations Options

The NUP4201DR2 is able to protect up to four data lines against transient over−voltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (Vcc+Vf). The diodes will drive the transient current away from the sensitive circuit.

Data lines are connected at pins 1,4,6 and 7. The negative reference is connected at pins 5 and 8. These pins must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce as much as possible the PCB trace lengths to minimize parasitic inductances.

Option 1

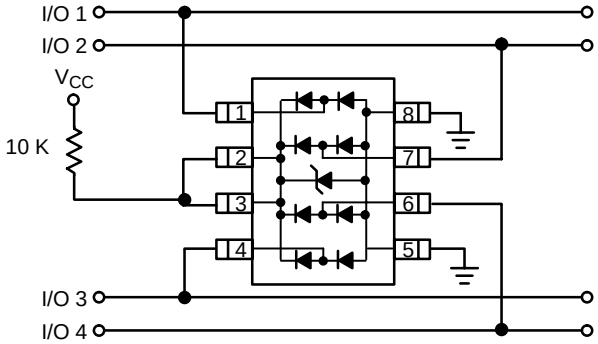
Four Data lines protection and power supply protection using Vcc as reference.



For this configuration, connect pins 2 & 3 directly to the positive supply rail (Vcc), the data lines are referenced to the supply voltage. The internal TVS diode prevents over−voltage on the supply rail.

Option 2

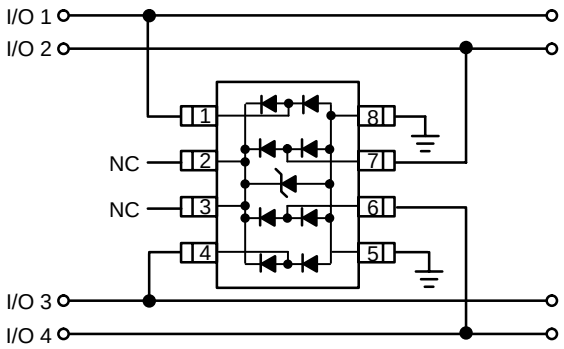
Four Data lines protection with Bias and power supply isolation resistor.



The NUP4201DR2 device can be isolated from the power supply by connecting a series resistor between pins 2 & 3 and Vcc. A resistor of 10KΩ is recommended for isolation purposes. The internal TVS and steering diodes remain biased, which provides the advantage of lower capacitance.

Option 3

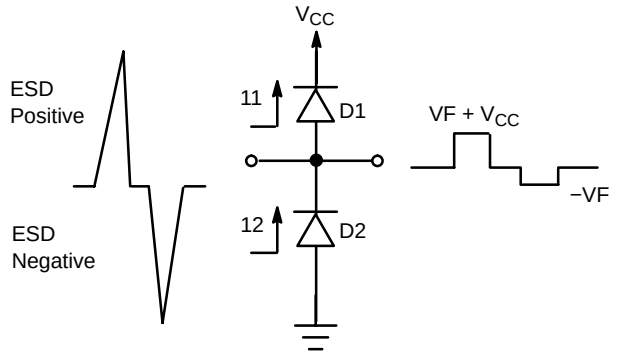
Four Data lines protection using internal TVS diode as reference.



In the case of applications in which a positive supply reference is not available or full isolation is required, the internal TVS could be used as the reference, so for this purpose, the pins 2 and 3 are not connected. In this case, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the TVS plus one diode drop ($V_C = V_f + V_{TVS}$).

“Rail to Rail” Protection Topology

The following figure shows a case when discrete diodes are configured for rail to rail protection on an I/O line:



Upon the above figure, it is possible to observe that if a positive ESD condition occurs, the D1 diode will be forward biased while the D2 diode will be biased when a negative ESD condition occurs. A valid first approximation of the resulting clamping voltage due to the protection diodes can be made as follows:

For positive pulse conditions:

$Vc = Vcc + Vf$

For negative pulse conditions:

$Vc = -Vf$

It is important to mention that effects of parasitic inductances must be considered for fast rise time transient conditions because the clamping voltage on the protected circuit will be different than in the previous case. A valid approximation of the resulting clamping voltage can be made as show below:

For positive pulse conditions:

$Vc = Vcc + Vf + (L\ di_{ESD}/dt)$

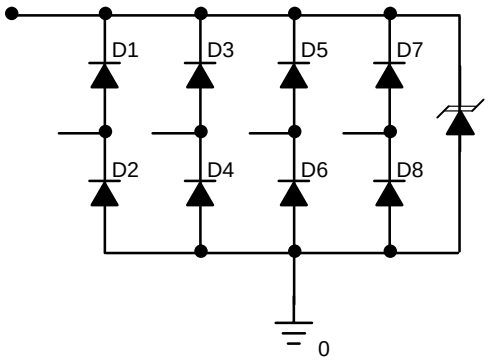
For negative pulse conditions:

$Vc = -Vf - (L\ di_{ESD}/dt)$

As shown in the formulas, the clamping voltage (Vc) not only depends on the Vf of the steering diodes but also in the $L\ di_{ESD}/dt$ factor, so this is why it is very important to have a good board layout to minimize the effects of the parasitic inductances.

Nevertheless, some disadvantages are still present when discrete diodes are used to suppress ESD conditions in “rail to rail” configuration. If the ESD current is too high, it can potentially result in the damage of any components connected to that rail and it is also possible to experience damage in the discrete diodes if their power dissipation capability is exceeded.

The NUP4201DR2 On Semiconductor’s device provides a concept named “RailClamp” which is designed to eliminate the disadvantages of the usage of discrete diodes for ESD protection. The RailClamp concept is achieved with the integration of the TVS device in together with the steering diodes.



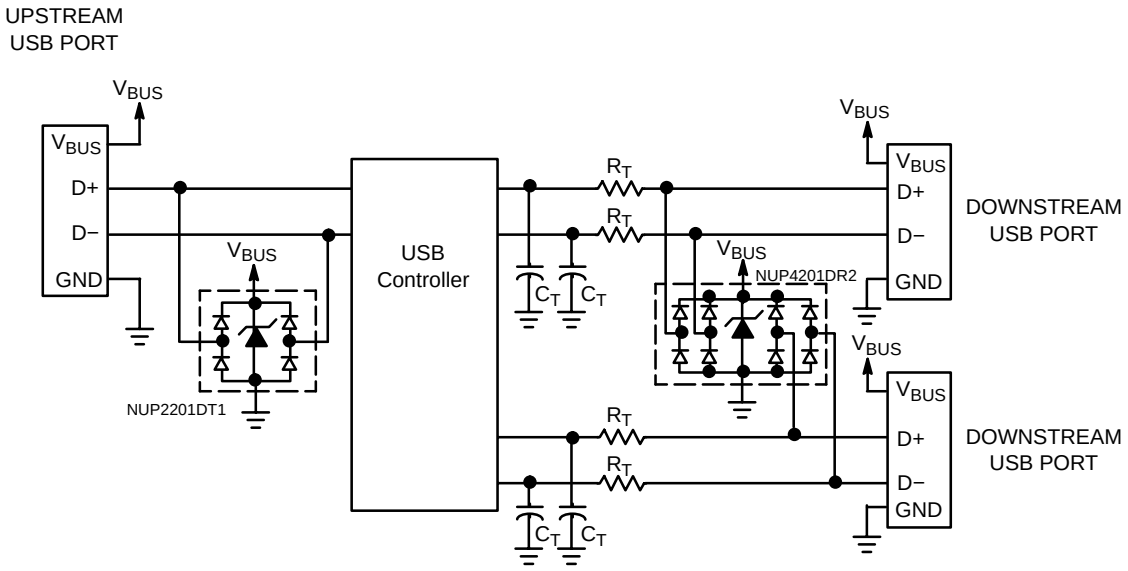
Rail to Rail Protection with integrated TBS to achieve the RailClamp concept

During an ESD condition, the ESD current will be driven to ground through the TVS device, so the resulting clamping voltage on the protected IC will be:

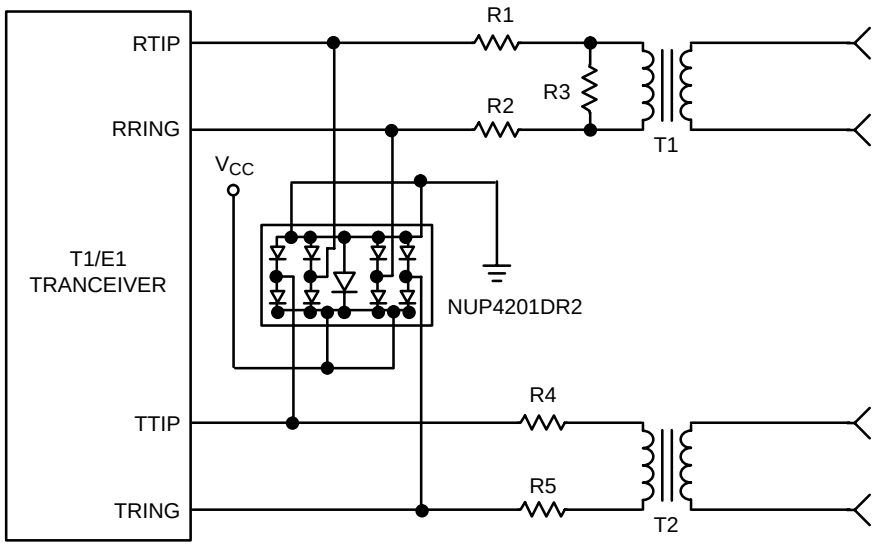
$Vc = V_{F(RailClamp)} + V_{TVS}$.

The clamping voltage of the TVS device is shown as part of the specifications of the NUP4201DR2 datasheet. The clamping voltage will depend on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

TYPICAL APPLICATIONS



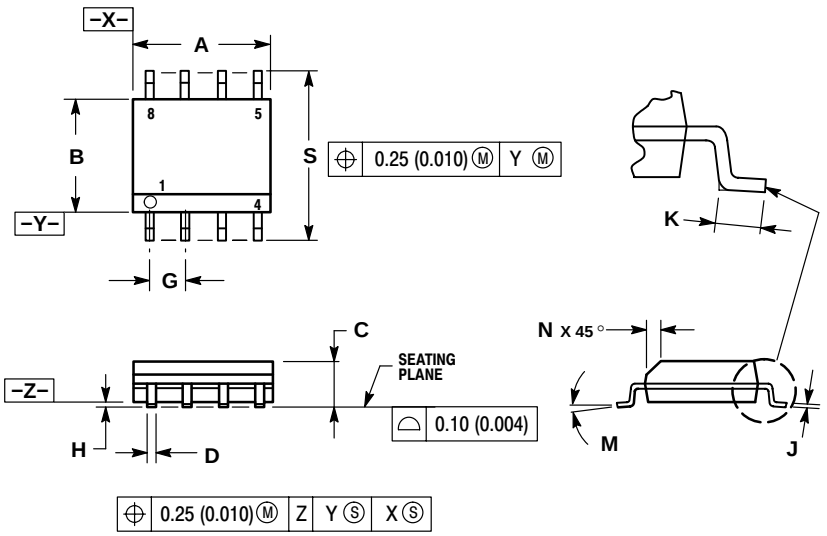
ESD Protection for USB Port



TI/E1 Interface Protection

PACKAGE DIMENSIONS

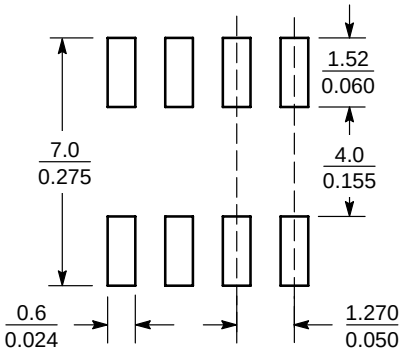
SO−8
CASE 751−07
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDAARD IS 751−07

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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