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NTE8374
Integrated Circuit
Seven–Segment Latch/Decoder/Driver for Common Anode LED's

Description:

The NTE 8374 is a 7–segment decoder driver in a 16–Lead DIP type package incorporating input latches and output circuits to directly drive common anode LED displays.

Features:

- High speed input latches for data storage
- 15mA constant current sink capability to directly drive common anode led displays
- Increases incandescent display life
- Active low latch enable for easy interface with MSI circuits
- Data input loading essentially zero when latch disabled
- Automatic ripple blanking for suppression of leading and/or trailing–edge zeroes.

Input Loading/Fan–Out:

Description	Pin Name	High	Low
Address (Data) Inputs,	$A_0 – A_3$	1.0	0.25 (Note 1)
Latch Enable Input (Active LOW)	$\overline{L_E}$	0.5	0.25
Ripple Blanking Input (Active LOW)	$\overline{RBI}$	0.5	0.25
Ripple Blanking as Output (Active LOW)	$\overline{RBO}$	1.0	0.5
Ripple Blanking as Input (Active LOW)	$\overline{RBO}$	–	0.75
Constant Current Outputs (Active LOW)	$\overline{a} – \overline{g}$	Open Collector	15mA

Note 1. Except Loading is 10μA @ 0.4V when $\overline{L_E}$ is HIGH.

Absolute Maximum Ratings:

Input Voltage . . . . . –0.5V to +5.5V
Input Current . . . . . –30mA to +5.0mA
Voltage Applied to Outputs in HIGH State:
  Standard TTL . . . . . –0.5V to V_{CC} value
  Open Collector . . . . . –0.5V to +7.0V
V_{CC} Pin Potential to GND Pin . . . . . –0.5V to +7.0V
Current Applied to Output in LOW State (Max) . . . . . twice the rated I_{OL}
Storage Temperature Range . . . . . –65° to +150°C
Ambient Temperature Range Under Bias . . . . . –55° to +125°C
Junction Temperature Range Under Bias . . . . . –55° to +175°C

Recommended Operating Conditions:

Supply Voltage . . . . . +4.75V to +5.25V
Free Air Ambient Temperature . . . . . 0°C to +70°C

Functional Description:

The NTE8374 is a 7–segment decoder/driver with latches on the address inputs and active LOW constant current outputs to drive LEDs directly. This device accepts a 4–bit binary code and produces output drive to the appropriate segments of the 7–segment display. It has a decode format which produces numeric codes “0” through “9” and other codes.

Latches on the four data inputs are controlled by an active $\overline{\text{LOW}}$ Latch Enable, $\overline{L_E}$. When $\overline{L_E}$ is LOW, the state of the outputs is determined by the input data. When $\overline{L_E}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{L_E}$ pulse width necessary to accept and store data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives LED displays with multiplexed data input from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs, since several circuits–seven resistors per display, strobe drivers, a separate display voltage source, and clock failure detect circuits–traditionally found in multiplexed display systems are eliminated. It also allos low strobing rates to be used without display flicker.

Another NTE8374 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10μA typ). This allows many NTE8374s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The NTE8374 also provides automatic blanking capability 0060.0300 would be displayed as 60.03. Leading–edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{\text{RBO}}$) of a decoder to the Ripple Blanking Input ($\overline{\text{RBI}}$) of the next lower stage device. The most significant decoder stage should have the $\overline{\text{RBI}}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the RBI input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing–edge zeros. The $\overline{\text{RBO}}$ terminal of the decoder can be or tied with a modulating signal via an isolating buffer to achieve duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

DC Characteristics: (T_A = 0 to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage, Applied (OFF)	V_{OUT}	Separate LED Supply	–	–	10	V
Output LOW Current, $\overline{a} – \overline{g}$	I_{OL}	V_{CC} = 5V, V_{OL} = 3V, T_A = +25°C	12	–	18	mA
Output HIGH Current, $\overline{a} – \overline{g}$	I_{OH}	V_{CC} = Max, V_{OUT} = 5.5V	–	–	250	μA
Power Supply Current	I_{CC}	V_{CC} = Max, V_{IN} = GND, V_{OUT} = 3V	–	–	50	mA

AC Characteristics: (V_{CC} = +5VT_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay, A_n to $\overline{a} – \overline{g}$	t_{PLH}, t_{PHL}	C_L = 15pF, R_L = 1kΩ	–	–	140	ns
Propagation Delay, $\overline{L_E}$ to $\overline{a} – \overline{g}$	t_{PLH}, t_{PHL}	C_L = 15pF, R_L = 1kΩ	–	–	140	ns

AC Operating Requirements: (V_{CC} = +5VT_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Setup Time HIGH or LOW, A_n to $\overline{L_E}$	t_s (H)		75	–	–	ns
	t_s (L)		30	–	–	ns
Hold Time HIGH or LOW, A_n to $\overline{L_E}$	t_h (H)		0	–	–	ns
	t_h (L)		0	–	–	ns
$\overline{L_E}$ Pulse Width LOW	t_w (L)		85	–	–	ns

Truth Table:

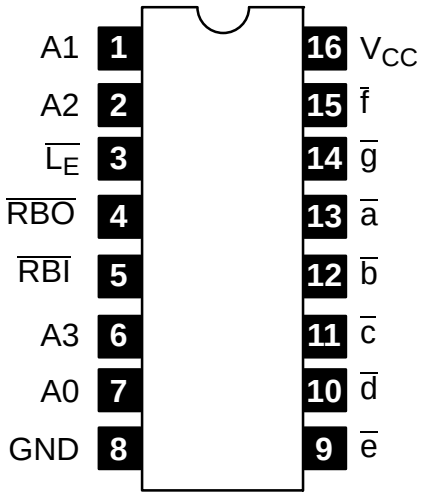
Binary State	Inputs						Outputs								Diaplay
	$\overline{L_E}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	
–	H	Note2	X	X	X	X	←——— STABLE ———→							H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	H	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	L	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	L	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	–
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	H	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	BLANK
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L Note 3	BLANK

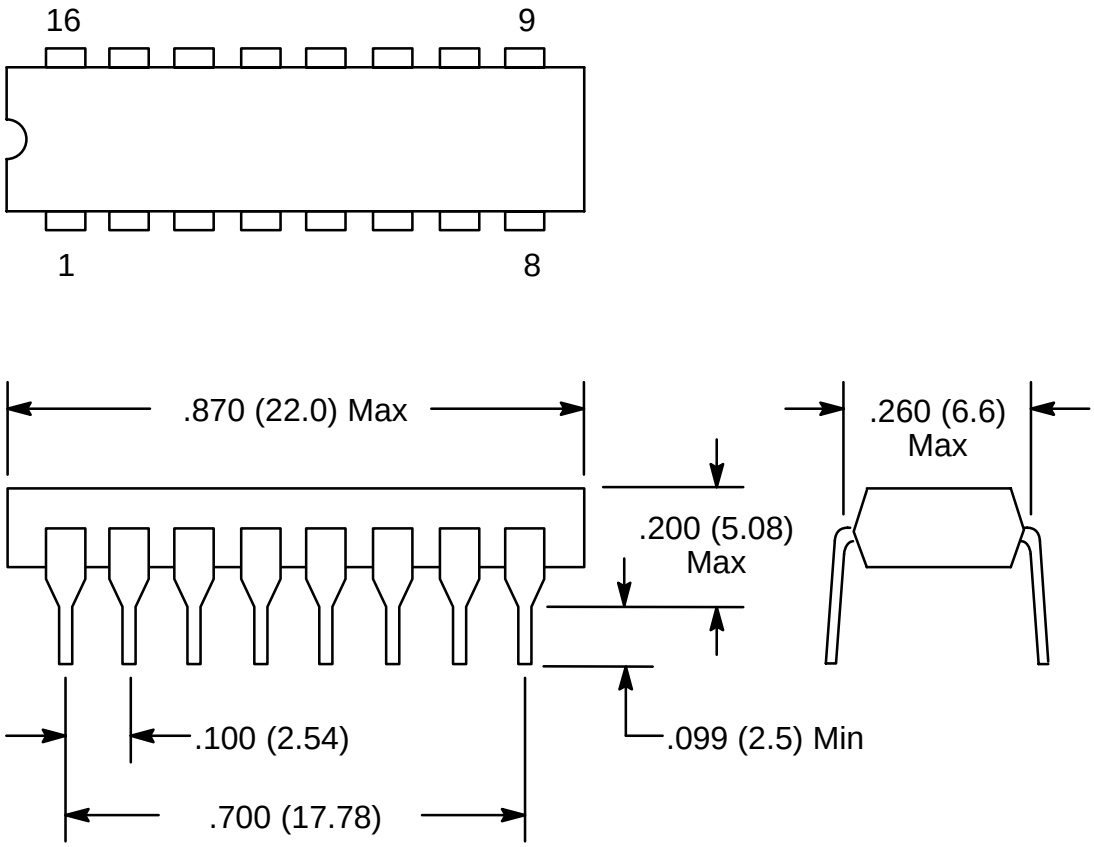
H = HIGH Voltage Level, L = LOW Voltage Level, X = Immaterial

Note 2. The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

Note 3. $\overline{RBO}$ used as an input overrides all other input conditions.

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200 (5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)