ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE6850
Integrated Circuit
NMOS, Asynchronous Communications Interface Adapter

Description:

The NTE6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the NTE6800 Microprocessing Unit.

The bus interface of the NTE6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8–bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. These lines allow the ACIA to interface directly with the NTE6860 0–600 bps digital modem.

Features:

- 8–Bit and 9–Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 1.0 Mbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One–Stop or Two–Stop Bit Operation

Absolute Maximum Ratings:

Supply Voltage, V_{CC} . . . . . –0.3 to +7.0V
Input Voltage, V_{in} . . . . . –0.3 to +7.0V
Operating Temperature Range, T_A . . . . . 0° to 70°C
Storage Temperature Range, T_{stg} . . . . . –55° to +150°C
Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 120°C/W

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{CC}).

Electrical Characteristics: (V_{CC} = 5V ± 5%, V_{SS} = 0, T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}		V_{SS}–0.3	–	V_{SS}+0.8	V
Input Leakage Current R/$\overline{W}$, CS0, CS1, $\overline{CS2}$, Enable, $\overline{RS}$, R_X D, R_X C, $\overline{CTS}$, $\overline{DCD}$	I_{in}	V_{in} = 0 to 5.25V	–	1.0	2.5	µA
Hi–Z (Off–State) Input Current D0 – D7	I_{TSI}	V_{in} = 0.4 to 2.4V	–	2.0	10.0	µA
Output High Voltage D0 – D7	V_{OH}	I_{Load} = 205µA, Enable Pulse Width < 25µs	V_{SS}+2.4	–	–	V
Output High Voltage T_X Data, $\overline{RTS}$		I_{Load} = 100µA, Enable Pulse Width < 25µs	V_{SS}+2.	–	–	V
Output Low Voltage	V_{OL}	I_{Load} = 1.6A, Enable Pulse Width < 25µs	–	–	V_{SS}+0.4	V
Output Leakage Current (Off–State) $\overline{IRQ}$	I_{LOH}	V_{OH} = 2.4V	–	1.0	10	µA
Internal Power Dissipation	P_{INT}	T_A = 0°C, Note 2	–	300	525	mW
Internal Input Capacitance D0 – D7	C_{in}	V_{in} = 0, T_A = +25°C, f = 1MHz	–	10.0	12.5	pF
Internal Input Capacitance E, T_X CLK, R_X CLK, R/$\overline{W}$, $\overline{RS}$, R_X Data, $\overline{CS0}$, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$			–	7.0	7.5	pF
Output Capacitance RTS, T_X Data	C_{out}	V_{in} = 0, T_A = +25°C, f = 1MHz	–	–	10	pF
Output Capacitance $\overline{IRQ}$			–	–	5	pF

Note 2. For temperatures less than T_A = 0°C, P_{INT} maximum will increase.

Serial Data Timing Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Data Clock Pulse Width, Low	PW_{CL}	÷16, ÷64 Modes	600	–	450	ns
		÷1 Mode	900	–	650	ns
Data Clock Pulse Width, High	PW_{CH}	÷16, ÷64 Modes	600	–	450	ns
		÷1 Mode	900	–	650	ns
Data Clock Frequency	f_C	÷16, ÷64 Modes	–	–	0.8	MHz
		÷1 Mode	–	–	500	kHz
Data Clock–to–Data Delay for Transmitter	t_{TDD}		–	–	600	ns
Receive Data Setup Time	t_{RDS}	÷1 Mode	250	–	–	ns
Receive Data Hold Time	t_{RDH}	÷1 Mode	250	–	–	ns
Interrupt Request Release Time	t_R		–	–	1.2	µs
Request–to–Send Delay Time	t_{RTS}		–	–	560	ns
Input Rise and Fall Times	t_r, t_f	or 10% of the pulse width if smaller	–	–	1.0	µs

Bus Timing Characteristics: ($V_L \leq 4V$, $V_H \geq 2.4V$, measurement points 0.8V and 2V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time	t_{cyc}		1.0	–	10.0	µs
Pulse Width, E Low	PW_{EL}		430	–	9500	ns
Pulse Width, E High	PW_{EH}		450	–	9500	ns
Clock Rise and Fall Time	t_r, t_f		–	–	25	ns
Address Hold Time	t_{AH}		10	–	–	ns
Address Setup Time Before E	t_{AS}		80	–	–	ns
Chip Select Setup Time Before E	t_{CS}		80	–	–	ns
Chip Select Hold Time	t_{CH}		10	–	–	ns
Read Data Hold Time	t_{DHR}	Note 3	20	–	50	ns
Write Data Hold Time	t_{DHW}		10	–	–	ns
Output data Delay Time	t_{DHW}		–	–	290	ns
Input Data Setup Time	t_{DSW}		165	–	–	ns

Note 3. The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

Pin Connection Diagram