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NTE5536
Silicon Controlled Rectifier (SCR)

Description:

The NTE5536 is a silicon controlled rectifier (SCR) in a TO220 type package designed for use as back–to–back SCR output devices for solid state relays or applications requiring high surge operation.

Features:

- 400A Surge Capability
- 800V Blocking Voltage

Absolute Maximum Ratings:

Peak Reverse Blocking Voltage (Note 1), V_{RRM} 800V
RMS Forward Current (T_C = +80°C, Note 2), $I_{T(RMS)}$ 40A
Average Forward Current (All Conduction Angles, Note 2), $I_{T(AV)}$ 25A
Peak Non–Repetitive Surge Current (1/2 Cycle, Sine Wave), I_{TSM}
8.3ms 400A
1.5ms 450A
Forward Peak Gate Power, P_{GM} 20W
Forward Average Gate Power, $P_{G(AV)}$ 500mW
Forward Peak Gate Current (300µs, 120 PPS), I_{GM} 2A
Operating Junction Temperature Range, T_J . . . . . –40° to +125°C
Storage Temperature Range, T_{stg} . . . . . –40° to +150°C
Thermal Resistance, Junction–to–Case, R_{thJC} . . . . . 1°C/W
Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 60°C/W

Note 1. V_{RRM} can be applied on a continuous DC basis without incurring damage. Ratings apply for zero or negative voltage. Device should be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

Note 2. This device is rated for use in applications subject to high surge conditions. Care must be taken to insure proper heat sinking when the device i to be used at high sustained currents.

Electrical Characteristics: (T_C = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Peak Forward Blocking Voltage	V_{DRM}	T_J = +125°C	800	–	–	V
Peak Forward or Reverse Blocking Current	I_{DRM}, I_{RRM}	Rated V_{DRM} or V_{RRM}, T_J = +25°C	–	–	10	μA
		Rated V_{DRM} or V_{RRM}, T_J = +125°C	–	–	2	mA
Forward ON Voltage	V_{TM}	I_{TM} = 80A, Note 3	–	1.6	2.0	V
Gate Trigger Current, Continuous DC	I_{GT}	Anode Voltage = 12V, R_L = 100Ω	–	15	50	mA
		Anode Voltage = 12V, R_L = 100Ω, T_C = –40°C	–	30	90	mA
Gate Trigger Voltage, Continuous DC	V_{GT}	Anode Voltage = 12V, R_L = 100Ω	–	1.0	1.5	V
Gate Non–Trigger Voltage	V_{GD}	Anode Voltage = 800V, R_L = 100Ω, T_J = +125°C	0.2	–	–	V
Holding Current	I_H	Anode Voltage = 12V	–	30	60	mA
Turn–On Time	t_{gt}	I_{TM} = 40A, I_{GT} = 60mA	–	1.5	–	μs
Critical Rate of Rise of Off–State Voltage	dv/dt	V_{DRM} = 800V, Gate Open, Exponential Waveform	–	50	–	V/μs

Note 3. Pulse test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.