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NTE3880
Integrated Circuit
NMOS, 8–Bit Microprocessor (MPU), 4MHz

Description:

The NTE3880 is a third generation single chip microprocessor with unrivaled computational power. This increased computational power results in higher system through–put and more efficient memory utilization when compared to second generation microprocessors. In addition it is very easy to implement into a system because of it's single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N–channel, ion implanted, silicon gate MOS process.

This device has an internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8–bit registers or as 16–bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast interrupt response. The NTE3880 also contains a 16–bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

The two 16–bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

Features:

- Single Chip, N–Channel Silicon Gate
- 158 Instructions – Includes all 78 of the 8080A Instructions with Total Software Compatibility. New Instructions Include 4–, 8– and 16–Bit Operations with more useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Fast Interrupt Response plus a Non–Maskable Interrupt
- Directly Interfaces Standard Speed Static or Dynamic Memories with Virtually No External Logic
- 1.0μs Instruction Execution Speed
- Single 5VDC Supply and Single–Phase 5V Clock
- Out–Performs any other Single–Phase 5V Clock
- All Pins TTL Compatible
- Built–In Dynamic RAM Refresh Circuitry

Absolute Maximum Ratings:

Temperature Under Bias . . . . . 0° to +70°C
Storage Temperature Range . . . . . –65° to +150°C
Voltage On Any Pin With Respect to GND . . . . . –0.3V to +7V
Power Dissipation 1.5W

Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics: (T_A = 0° to 70°C, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Input Low Voltage	V_{ILC}		–0.3	–	0.80	V
Clock Input High Voltage	V_{IHC}		V_{CC}–0.6	–	V_{CC}+3	V
Input Low Voltage	V_{IL}		–0.3	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 1.8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –250µA	2.4	–	–	V
Power Supply Current	I_{CC}		–	90	200	mA
Input Leakage Current	I_{L1}	V_{IN} = 0 to V_{CC}	–	–	10	µA
Tri–State Output Leakage Current in Float	I_{LOH}	V_{OUT} = 2.4 to V_{CC}	–	–	10	µA
Tri–State Output Leakage Current in Float	I_{LOL}	V_{OUT} = 0.4V	–	–	–10	µA
Data Bus Leakage Current in Input Mode	I_{LD}	$0 \le V_{IN} \le V_{CC}$	–	–	±10	µA

Capacitance: (T_A = +25°C, f = 1MHz, unmeasured pins to GND unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Capacitance	C_ϕ		–	–	35	pF
Input Capacitance	C_{IN}		–	–	5	pF
Output Capacitance	C_{OUT}		–	–	10	pF

AC Characteristics: (T_A = 0°C to +70°C, V_{CC} = +15V ± 5% unless otherwise specified)

Parameter	Symbol	Signal	Test Conditions	Min	Typ	Max	Unit
Clock Period	t_c	ϕ		25	–	Note 2	µs
Clock Pulse Width, Clock High	t_w (ϕH)			110	–	Note 3	ns
Clock Pulse Width, Clock Low	t_w (ϕL)			110	–	2000	ns
Clock Rise and Fall Time	t_r, t_f			–	–	30	ns
Address Output Delay	t_D (AD)	$A_{0–15}$	C_L = 50pF	–	–	110	ns
Data to Float	t_F (AD)			–	–	90	ns
Address Stable Prior to $\overline{\text{MRFQ}}$ (Memory Cycle)	t_{acm}			Note 4	–	–	ns
Address Stable Prior to $\overline{\text{IOFQ}}$, $\overline{\text{RD}}$ or $\overline{\text{WR}}$ (I/O Cycle)	t_{aci}			Note 5	–	–	ns
Address Stable from $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, or $\overline{\text{MREQ}}$	t_{ca}			Note 6	–	–	ns
Address Stable from RD or WR During Float	t_{caf}			Note 7	–	–	ns

Note 2. $t_c = t_w (\phi H) + t_w (\phi L) + t_r + t_f$.
Note 3. Although static by design, testing guarantees $t_w (\phi H)$ of 200µs maximum.
Note 4. $t_{acm} = t_w (\phi H) + t_f – 65$.
Note 5. $t_{aci} = t_c – 70$.
Note 6. $t_{ca} = t_w (\phi L) + t_r – 50$.
Note 7. $t_{caf} = t_w (\phi L) + t_r – 45$.

AC Characteristics (Cont'd): (T_A = 0°C to +70°C, V_{CC} = +15V ± 5% unless otherwise specified)

Parameter	Symbol	Signal	Test Conditions	Min	Typ	Max	Unit
Data Output Delay	t_D (D)	D_{0-7}	C_L = 50pF	–	–	150	ns
Delay to Float During Write Cycle	t_F (D)			–	–	90	ns
Data Setup Time to Rising Edge of Clock During M_1 Cycle	$t_{S\phi}$ (D)			35	–	–	ns
Data Setup Time to falling Edge of Clock During M_2 to M_5				50	–	–	ns
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}			Note 8	–	–	ns
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}			Note 9	–	–	ns
Data Stable From $\overline{WR}$	t_{cdf}			Note 10	–	–	ns
Any Hold Time for Setup Time	t_H			–	–	0	ns
$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low	$t_{DL\phi}$ (MR)	$\overline{MREQ}$	C_L = 50pF	–	–	85	ns
$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High	$t_{DH\phi}$ (MR)			–	–	85	ns
$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High				–	–	85	ns
Pulse Width, $\overline{MREQ}$ Low	t_w ($\overline{MR}$L)			Note 11	–	–	ns
Pulse Width, $\overline{MREQ}$ High	t_w ($\overline{MR}$H)			Note 12	–	–	ns
$\overline{IORQ}$ Delay From Rising Edge of Clock $\overline{IORQ}$ Low	$t_{DL\phi}$ (IR)	$\overline{IORQ}$	C_L = 50pF	–	–	75	ns
$\overline{IORQ}$ Delay From Falling Edge of Clock $\overline{IORQ}$ Low				–	–	85	ns
$\overline{IORQ}$ Delay From Rising Edge of Clock $\overline{IORQ}$ High	$t_{DH\phi}$ (IR)			–	–	85	ns
$\overline{IORQ}$ Delay From Falling Edge of Clock $\overline{IORQ}$ High				–	–	85	ns
$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low	$t_{DL\phi}$ ($\overline{RD}$)	$\overline{RD}$	C_L = 50pF	–	–	85	ns
$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low				–	–	95	ns
$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High	$t_{DH\phi}$ ($\overline{RD}$)			–	–	85	ns
$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High				–	–	85	ns
$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low	$t_{DL\phi}$ ($\overline{WR}$)	$\overline{WR}$	C_L = 50pF	–	–	65	ns
$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low				–	–	80	ns
$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High	$t_{DH\phi}$ ($\overline{WR}$)			–	–	80	ns
Pulse Width, $\overline{WR}$ Low	t_w ($\overline{WR}$L)			Note 13	–	–	ns

Note 8. $t_{dcm} = t_c – 170$.
Note 9. $t_{dci} = t_w (\phi L) + t_r – 170$.
Note 10. $t_{cdf} = t_w (\phi L) + t_r – 70$.
Note 11. $t_w (\overline{MR}L) = t_c – 30$.
Note 12. $t_w (\overline{MR}H) = t_w (\phi H) + t_r – 20$.
Note 13. t_w (WRL) = $t_c – 30$.

AC Characteristics (Cont'd): (T_A = 0°C to +70°C, V_{CC} = +15V ± 5% unless otherwise specified)

Parameter	Symbol	Signal	Test Conditions	Min	Typ	Max	Unit
$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low	t_{DL} ($\overline{M1}$)	$\overline{M1}$	C_L = 50pF	–	–	100	ns
$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High	t_{DH} ($\overline{M1}$)			–	–	100	ns
$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low	t_{DL} (RF)	$\overline{RFSH}$	C_L = 50pF	–	–	130	ns
$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High	t_{DH} (RF)			–	–	120	ns
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	t_s (WT)	$\overline{WAIT}$		70	–	–	ns
$\overline{HALT}$ Delay Time From Falling Edge of Clock	t_D (HT)	$\overline{HALT}$	C_L = 50pF	–	–	300	ns
$\overline{INT}$ Setup Time to Rising Edge of Clock	t_s (IT)	$\overline{INT}$		80	–	–	ns
Pulse Width, $\overline{NM1}$ Low	t_w ($\overline{NML}$)	$\overline{NM1}$		80	–	–	ns
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	t_s (BQ)	$\overline{BUSRQ}$		50	–	–	ns
$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low	t_{DL} (BA)	$\overline{BUSAK}$	C_L = 50pF	–	–	100	ns
$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ High	t_{DH} (BA)			–	–	100	ns
$\overline{RESET}$ Setup Time to Rising Edge of Clock	t_s (RS)	$\overline{RESET}$		60	–	–	ns
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	t_F (C)			–	–	80	ns
$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}			Note 14	–	–	ns

Note 14. $t_{mr} = 2t_c + t_w (\phi H) + t_f - 65$.

Note 15. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

Note 16. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

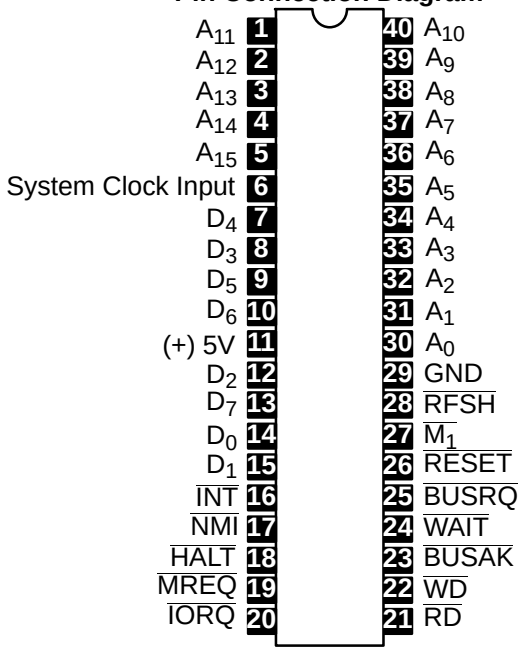
Note 17. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

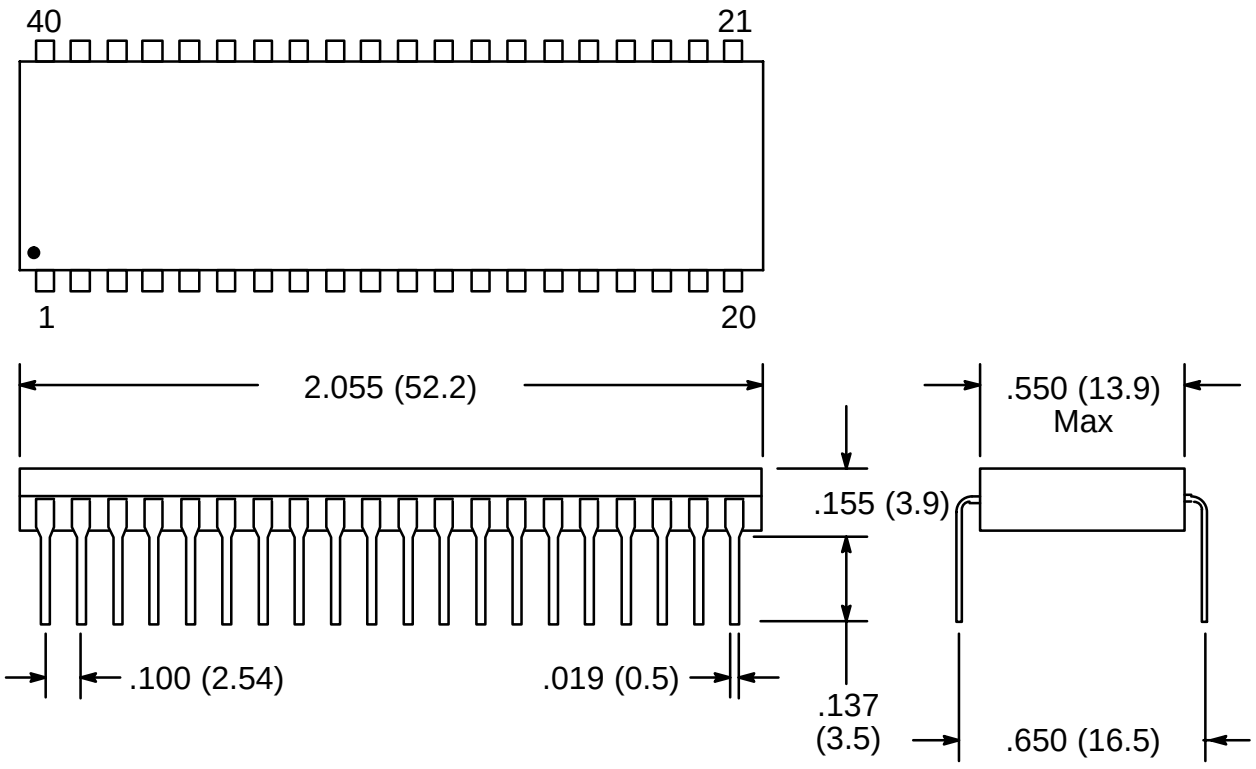
Note 18. Output Delay vs. Loaded Capacitance

T_A = +70°C V_{CC} = 5V ±5%

Add 10ns delay for each 50pf increase in load up to maximum of 200pF for data bus and 100pF for address & control lines.

Pin Connection Diagram




40
21
1
20
2.055 (52.2)
.550 (13.9)
Max
.155 (3.9)
.100 (2.54)
.019 (0.5)
.137
(3.5)
.650 (16.5)