NCP585

Tri-Mode 300 mA CMOS LDO Regulator with Enable

The NCP585 series of low dropout regulators are designed for portable battery powered applications which require precise output voltage accuracy, low supply current, and high ripple rejection. These devices feature an enable function which lowers current consumption significantly and are offered in the SOT23−5 and the HSON−6 packages.

This series of devices have three modes. Chip Enable (CE mode), Fast Transient Mode (FT mode), and Low Power Mode (LP mode). Both the FT and LP mode are utilized via the ECO pin.

Features

- Low Dropout Voltage of 480 mV at 300 mA, Output Voltage = 1.0 V
  310 mV at 300 mA, Output Voltage = 1.5 V
  230 mV at 300 mA, Output Voltage = 3.0 V
- Excellent Line and Load Regulation
- High Output Voltage Accuracy of ±2% (±3% LP mode)
- Ultra−Low Supply Current of:
  3.5 μA (LP mode, Output Voltage < 1.6 V)
  80 μA (FT mode, Output Voltage < 1.8 V)
  60 μA (FT mode, Output Voltage ≥ 1.8 V)
- Excellent Power Supply Rejection Ratio of 65 dB
- Output Voltage Options: 0.9, 1.2 and 1.8 V
- Low Temperature Drift Coefficient on the Output Voltage
- Low Quiescent of 0.1 μA
- Fold Back Protection Circuit
- These are Pb−Free Devices

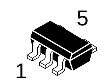
Typical Applications

- Portable Equipment
- Hand−Held Instrumentation
- Camcorders and Cameras

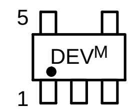
ON Semiconductor®

http://onsemi.com

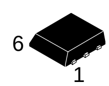
MARKING DIAGRAM



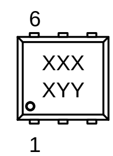
SOT23−5
SN SUFFIX
CASE 1212



DEV = Specific Device Code
M = Date Code



HSON−6
SAN SUFFIX
CASE 506AE



XXXX = Specific Device Code
YY = Wafer Lot

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

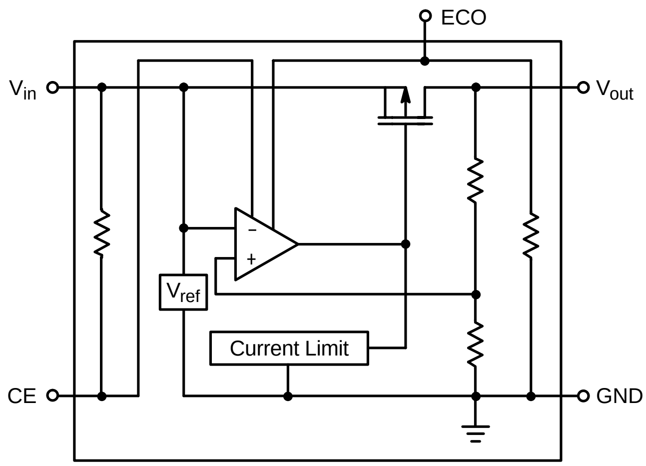


Figure 1. Simplified Block Diagram for Active Low

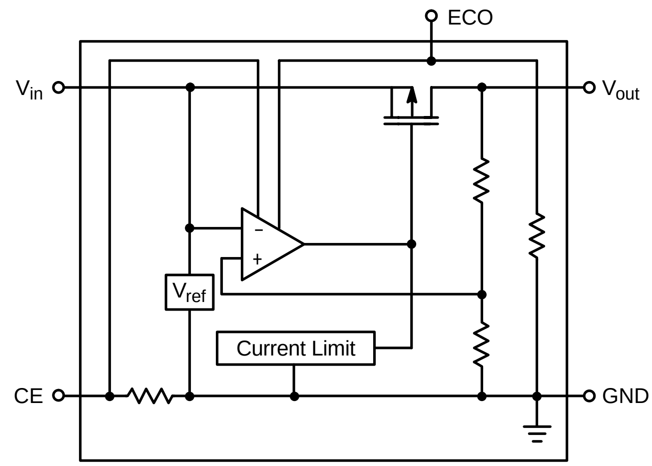


Figure 2. Simplified Block Diagram for Active High

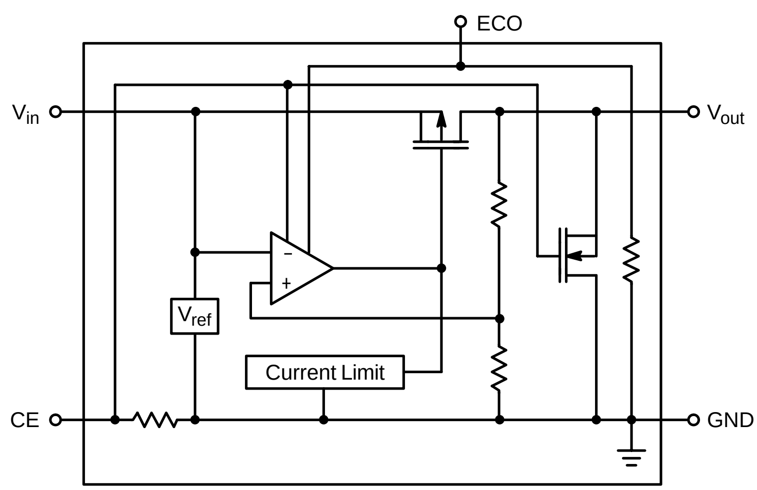


Figure 1. Simplified Block Diagram for Active High with Auto Discharge

PIN FUNCTION DESCRIPTION

HSON−6	SOT23−5	Pin Name	Description
1	1	V_{in}	Power supply input voltage.
2	−	NC	No Connect.
3	5	V_{out}	Regulated output voltage.
4	4	ECO	Mode alternative pin.
5	2	GND	Power supply ground.
6	3	$\overline{CE}$ or CE	Chip enable pin.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input Voltage		V_{in}	6.5	V
Input Voltage ($\overline{CE}$ or CE Pin)		V_{CE}	−0.3 to 6.5	V
Input Voltage (ECO Pin)		V_{ECO}	−0.3 to 6.5	V
Output Voltage		V_{out}	−0.3 to V_{in} +0.3	V
Output Current		I_{out}	350	mA
Power Dissipation	SOT23−5 HSON−6	P_D	250 400	mW
Operating Junction Temperature Range		T_J	−40 to +85	°C
Storage Temperature Range		T_{stg}	+150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (V_{in} = V_{out} + 1.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ		Max		Unit
Input Voltage	V_{in}	1.4	–		6.0		V
Output Voltage (1.0 μA ≤ I_{out} ≤ 30 mA) V_{ECO} = V_{in} V_{ECO} = GND	V_{out}	 V_{out} x 0.980 V_{out} x 0.970	 – –		 V_{out} x 1.020 V_{out} x 1.030		V
Line Regulation (I_{out} = 30 mA, V_{out} + 0.5 V ≤ V_{in} ≤ 6.0 V) FT Mode V_{ECO} = V_{in} LP Mode V_{ECO} = GND	Reg_{line}	 – –	 0.01 0.05		 0.15 0.20		%/V
Load Regulation FT Mode (1.0 mA ≤ I_{out} ≤ 300 mA), V_{ECO} = V_{in} LP Mode (1.0 mA ≤ I_{out} ≤ 100 mA), V_{ECO} = GND	Reg_{load}	 – –	 40 15		 70 30		mV
Dropout Voltage (I_{out} = 300 mA) V_{out} = 0.9 V 1.0 ≤ V_{out} ≤ 1.4 V 1.5 ≤ V_{out} ≤ 2.5 V	V_{DO}	 – – –	ECO = H 0.55 0.48 0.31	ECO = L 0.59 0.51 0.32	ECO = H 0.78 0.70 0.45	ECO = L 0.80 0.75 0.48	V
Power Supply Current (I_{out} = 0 mA) FT Mode, V_{ECO} = V_{in} V_{out} < 1.8 V V_{out} ≥ 1.8 V LP Mode, V_{ECO} = GND V_{out} < 1.6 V V_{out} ≥ 1.6 V	I_{supply}	 – – – –	 80 60 3.5 4.5		 111 90 8.0 9.0		μA
Output Current (V_{in} − V_{out} = 1.0 V)	I_{out}	300	–		–		mA
Quiescent Current (V_{CE} = V_{in})	I_Q	–	0.1		1.0		μA
Output Short Circuit Current (V_{out} = 0 V)	I_{lim}	–	50		–		mA
Enable Input Threshold Voltage Active Low, ECO Input Voltage = High Active High, ECO Input Voltage = Low	 Vth_{enl} Vth_{enh}	 1.0 1.0	 – –		 0.6 V_{in}		V
Output Noise Voltage (10 Hz − 100 kHz)	V_n	–	30		–		μVrms
N−Channel On Resistance for Auto Discharge	R_{Low}	–	60		–		Ω

TYPICAL CHARACTERISTICS

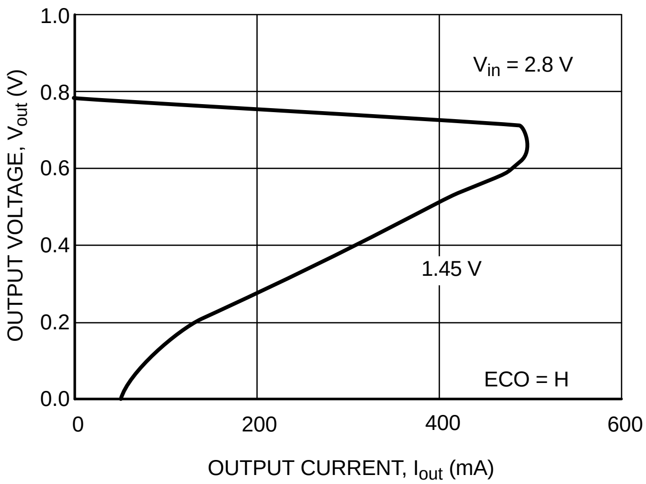


Figure 3. Output Voltage vs. Output Current

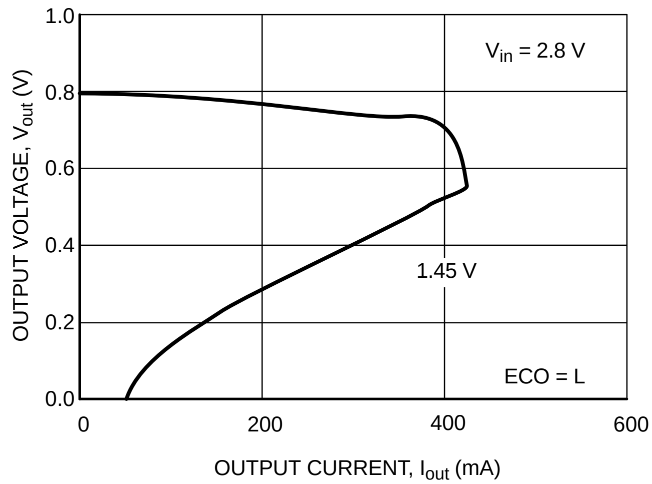


Figure 4. Output Voltage vs. Output Current

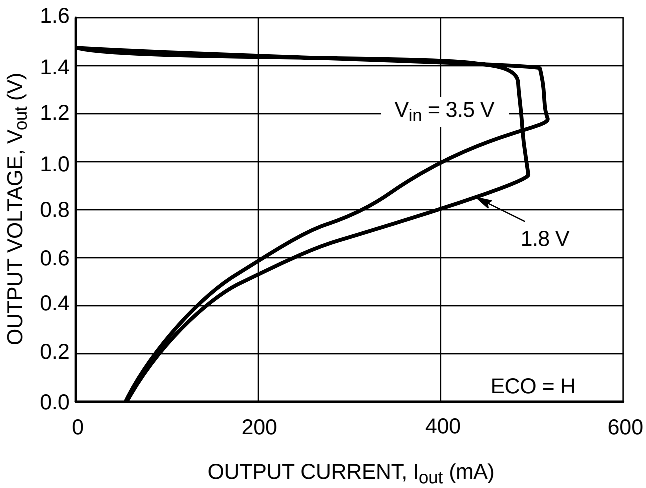


Figure 5. Output Voltage vs. Output Current

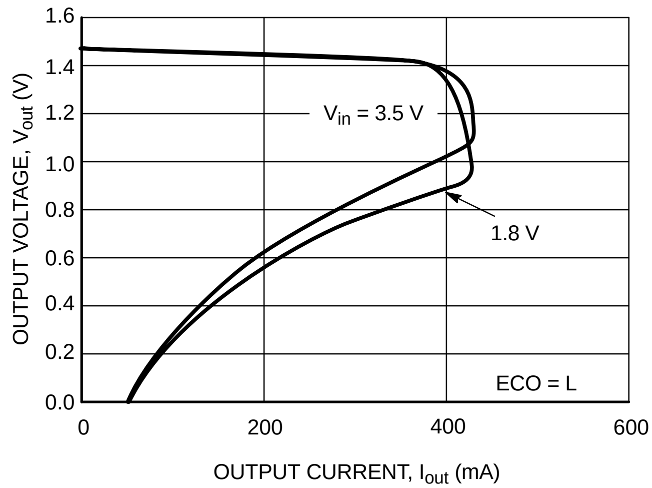


Figure 6. Output Voltage vs. Output Current

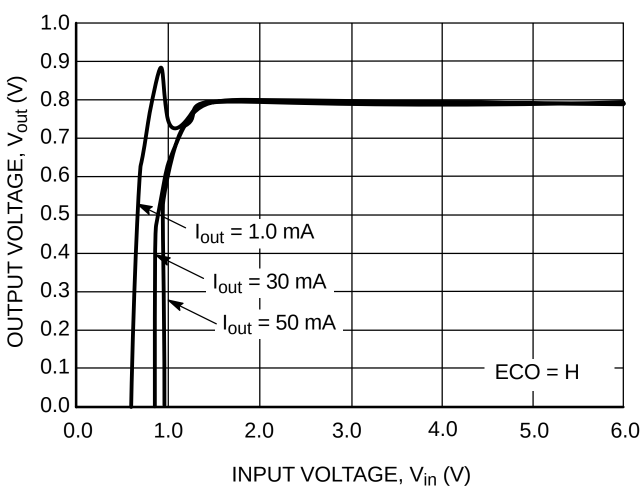


Figure 7. Output Voltage vs. Input Voltage

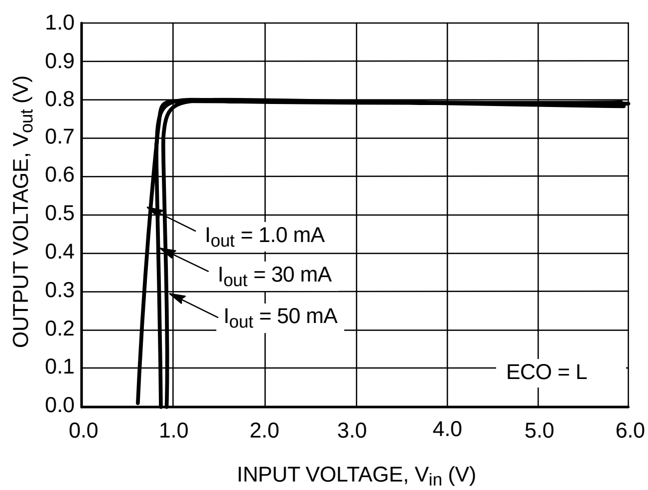


Figure 8. Output Voltage vs. Input Voltage

TYPICAL CHARACTERISTICS

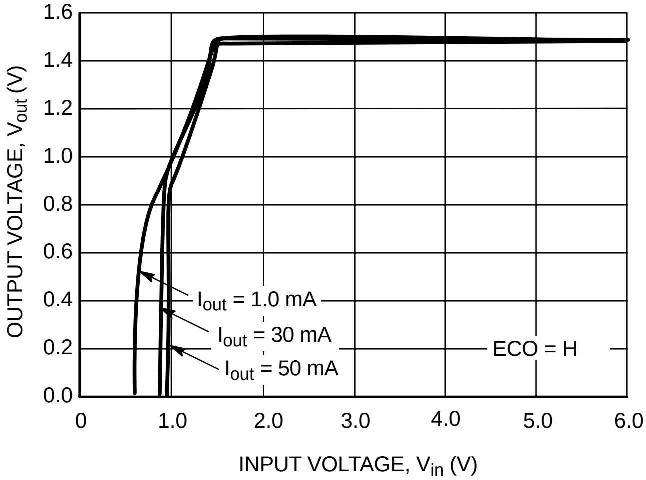


Figure 9. Output Voltage vs. Input Voltage

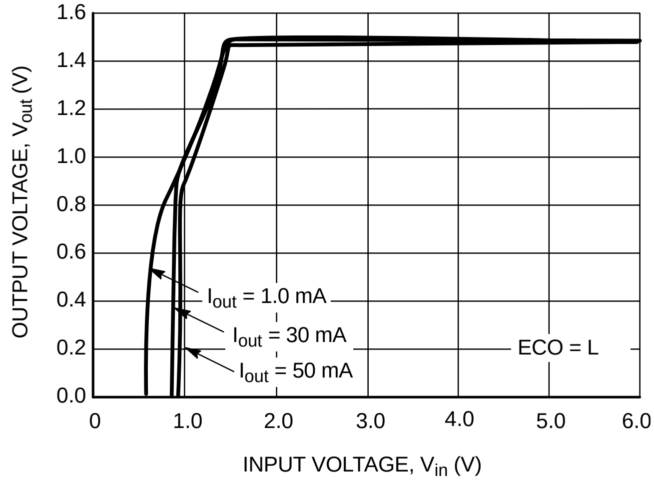


Figure 10. Output Voltage vs. Input Voltage

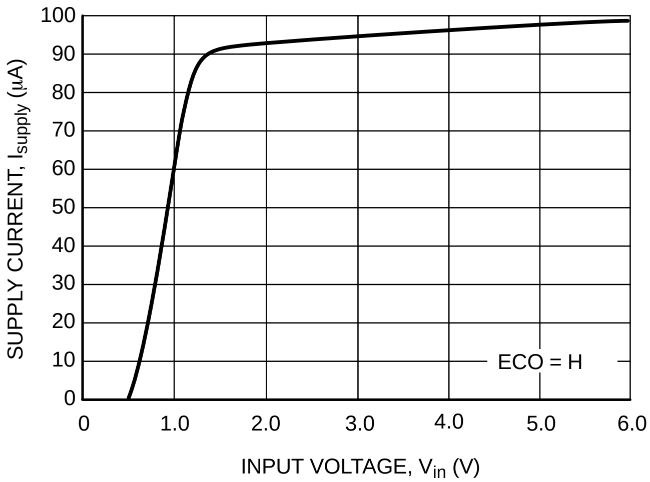


Figure 11. Power Supply Current vs. Input Voltage

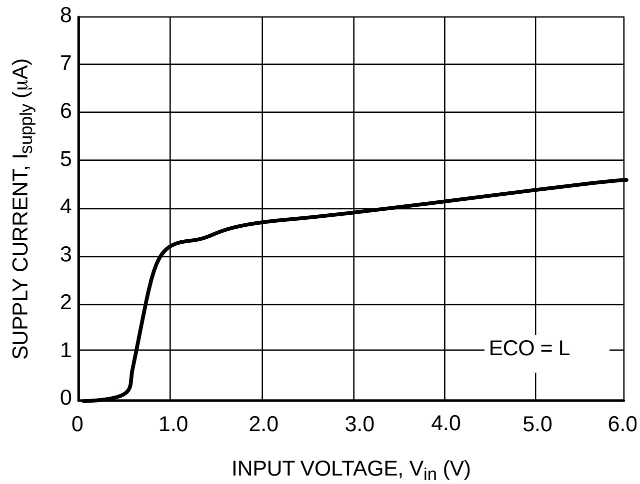


Figure 12. Power Supply Current vs. Input Voltage

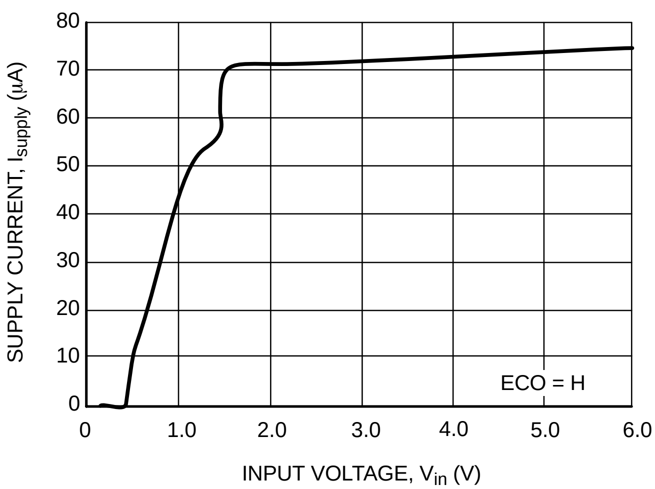


Figure 13. Power Supply Current vs. Input Voltage

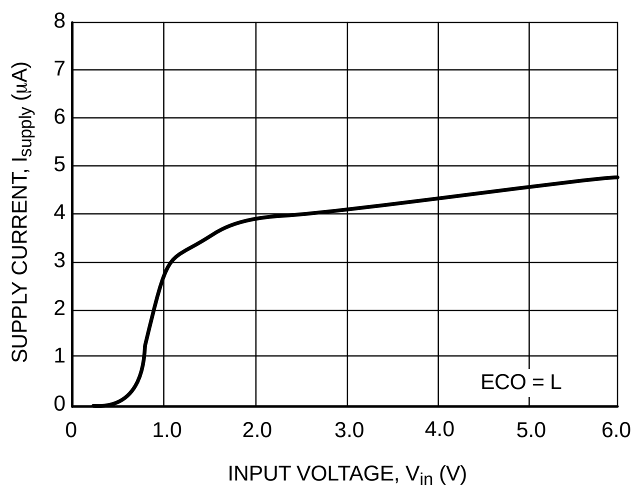


Figure 14. Power Supply Current vs. Input Voltage

TYPICAL CHARACTERISTICS

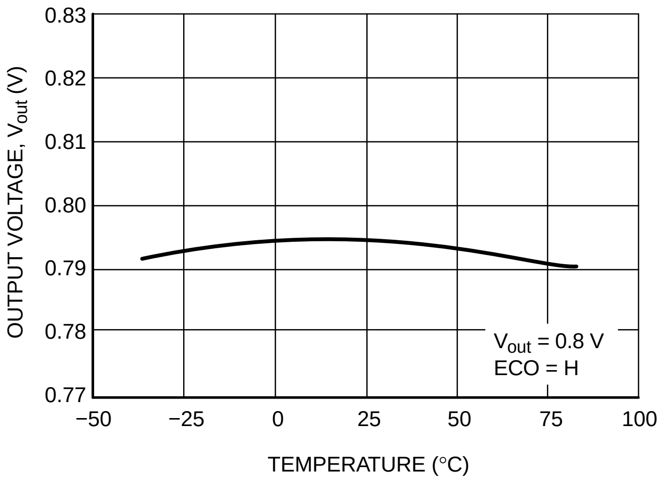


Figure 15. Output Voltage vs. Temperature

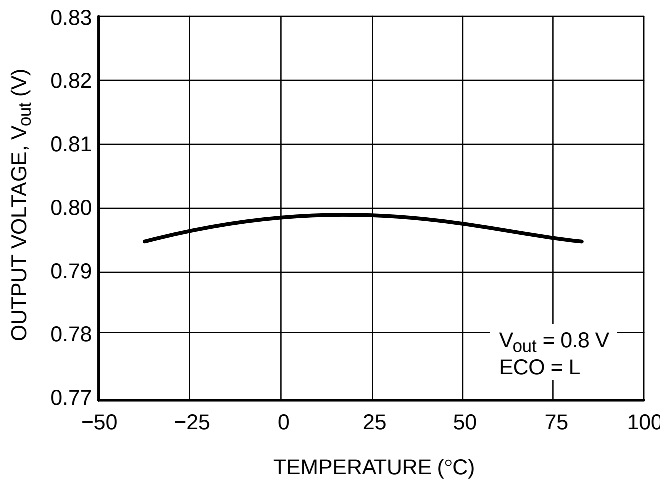


Figure 16. Output Voltage vs. Temperature

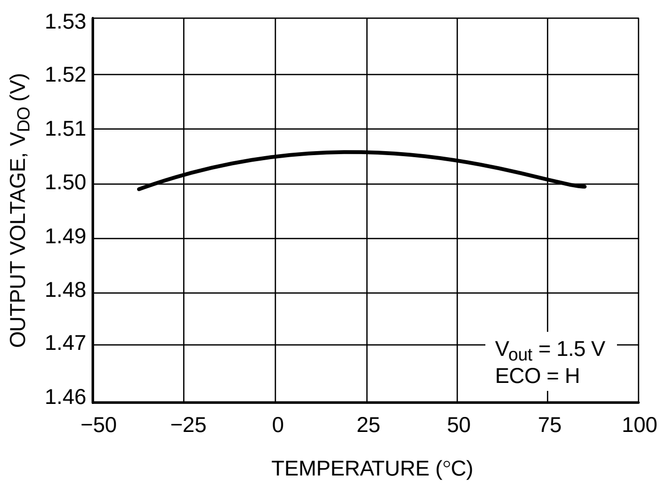


Figure 17. Output Voltage vs. Temperature

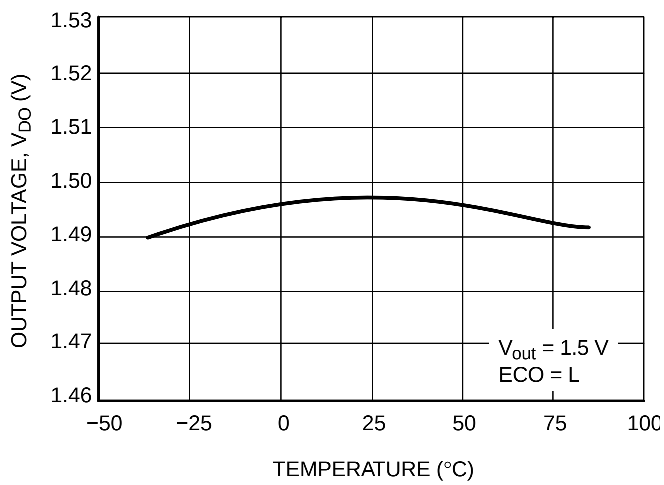


Figure 18. Output Voltage vs. Temperature

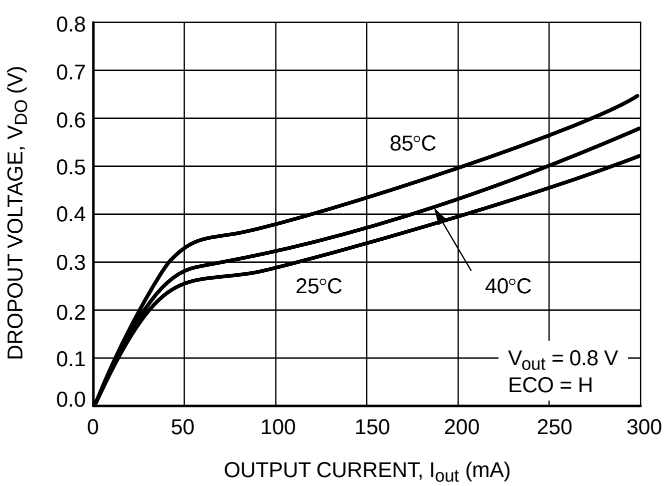


Figure 19. Dropout Voltage vs. Output Current

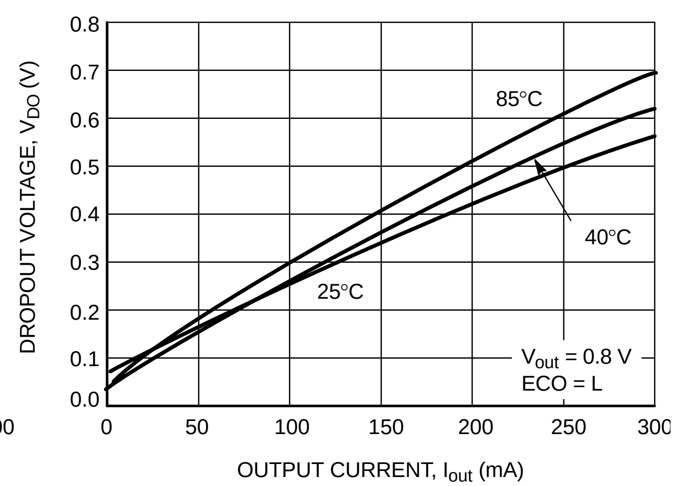


Figure 20. Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

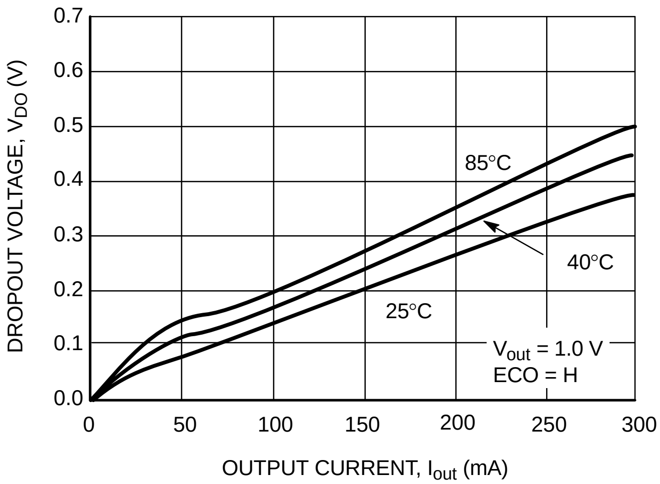


Figure 21. Dropout Voltage vs. Output Current

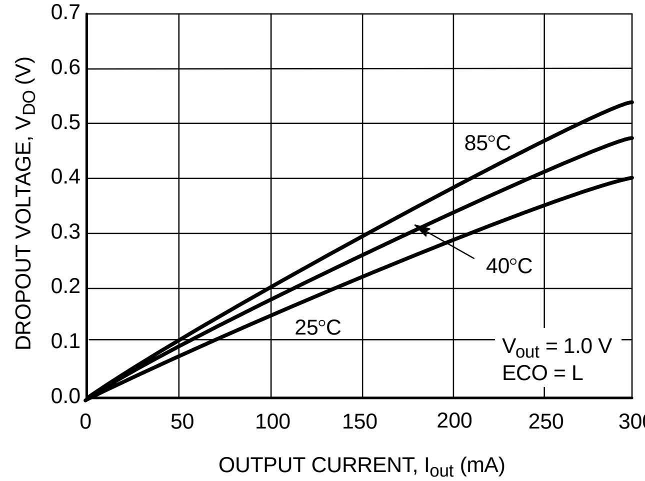


Figure 22. Dropout Voltage vs. Output Current

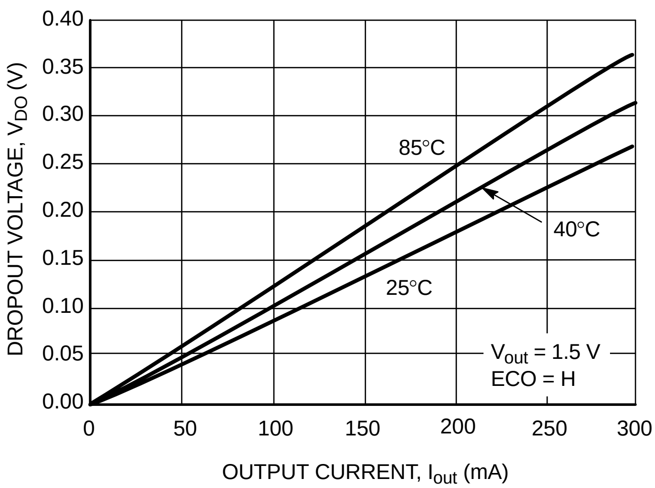


Figure 23. Dropout Voltage vs. Output Current

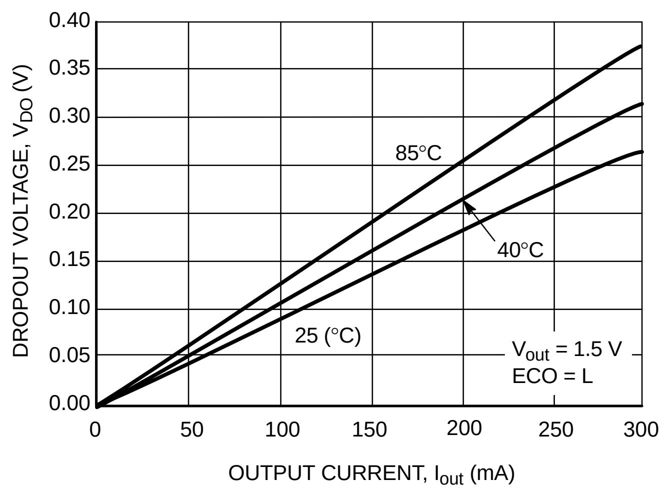


Figure 24. Dropout Voltage vs. Output Current

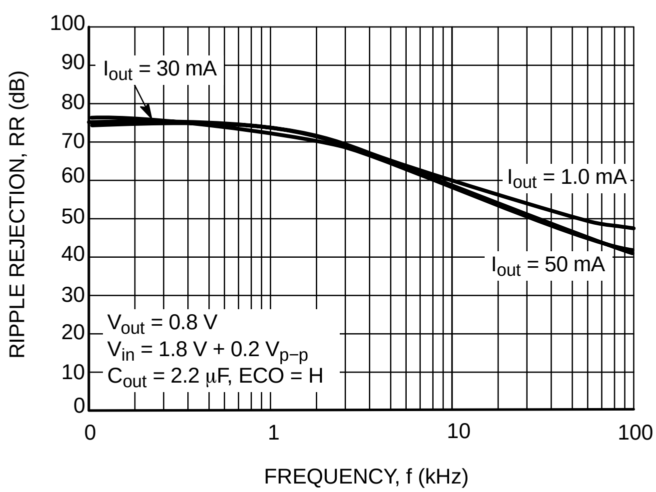


Figure 25. Ripple Rejection vs. Frequency

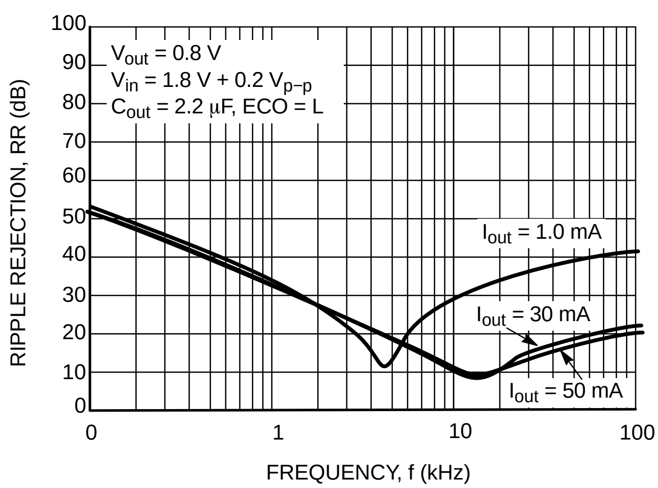


Figure 26. Ripple Rejection vs. Frequency

TYPICAL CHARACTERISTICS

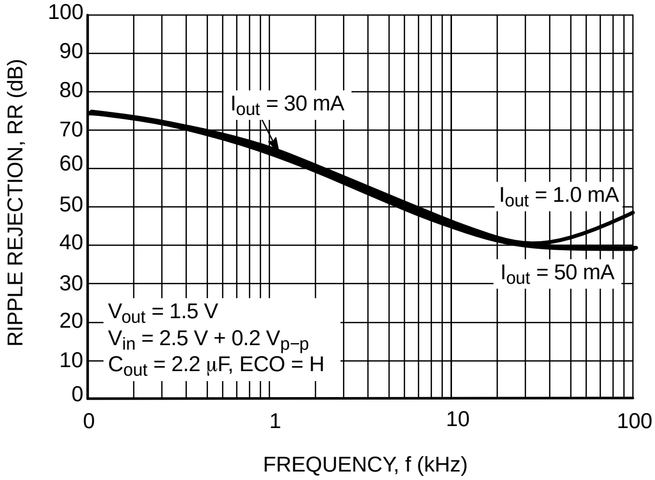


Figure 27. Ripple Rejection vs. Frequency

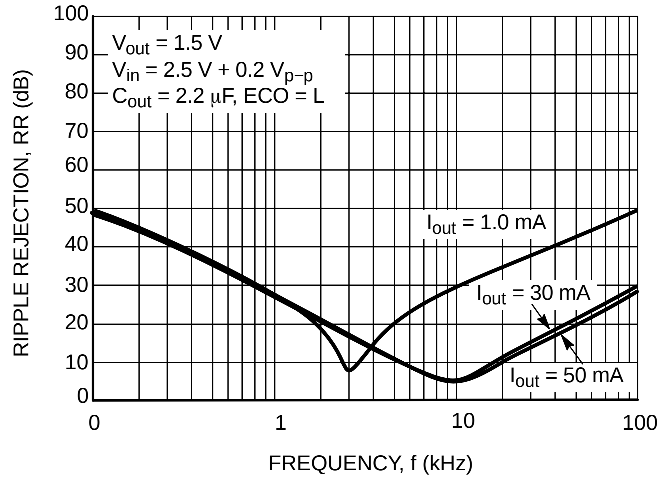


Figure 28. Ripple Rejection vs. Frequency

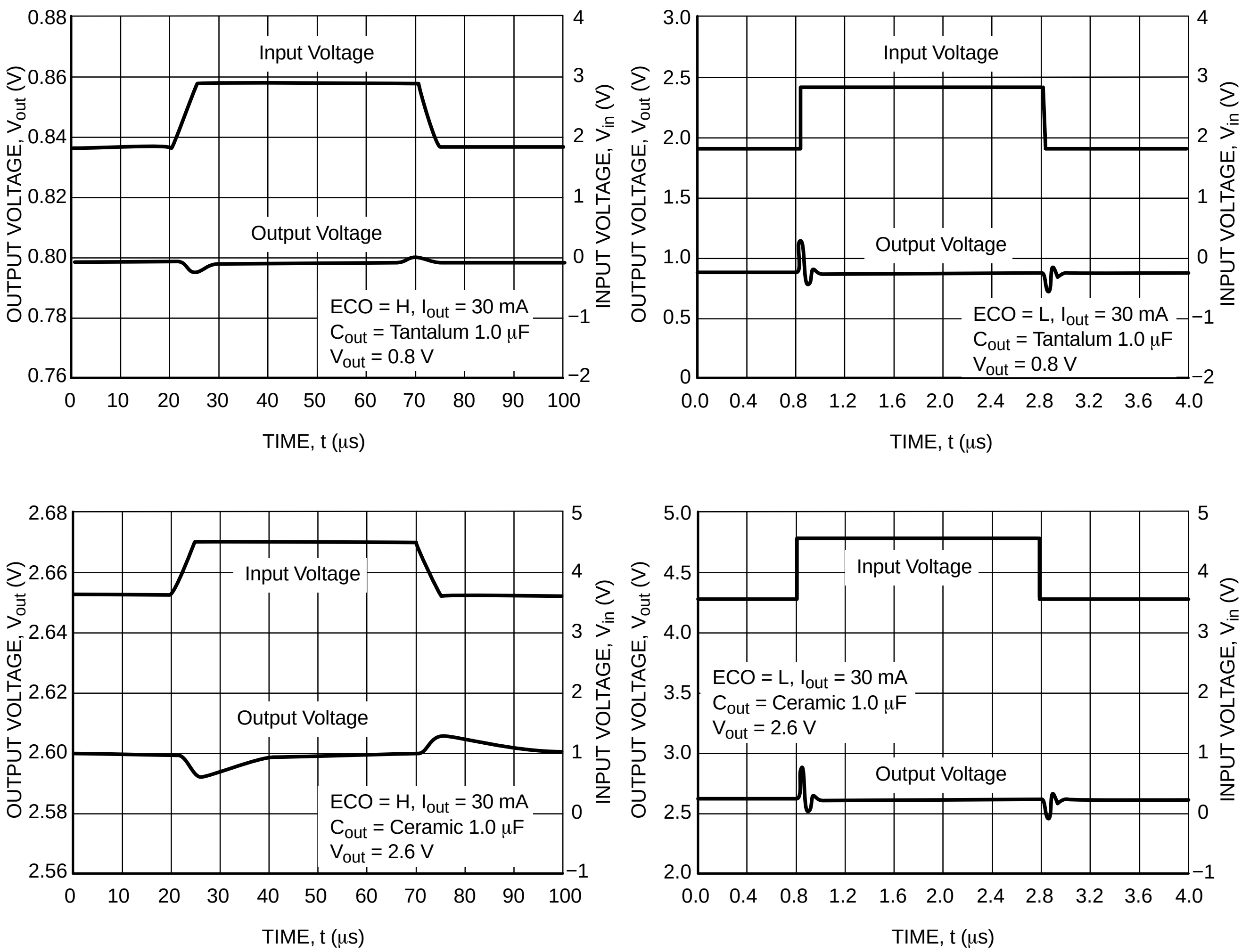


Figure 29. Input Transient Response

TYPICAL CHARACTERISTICS

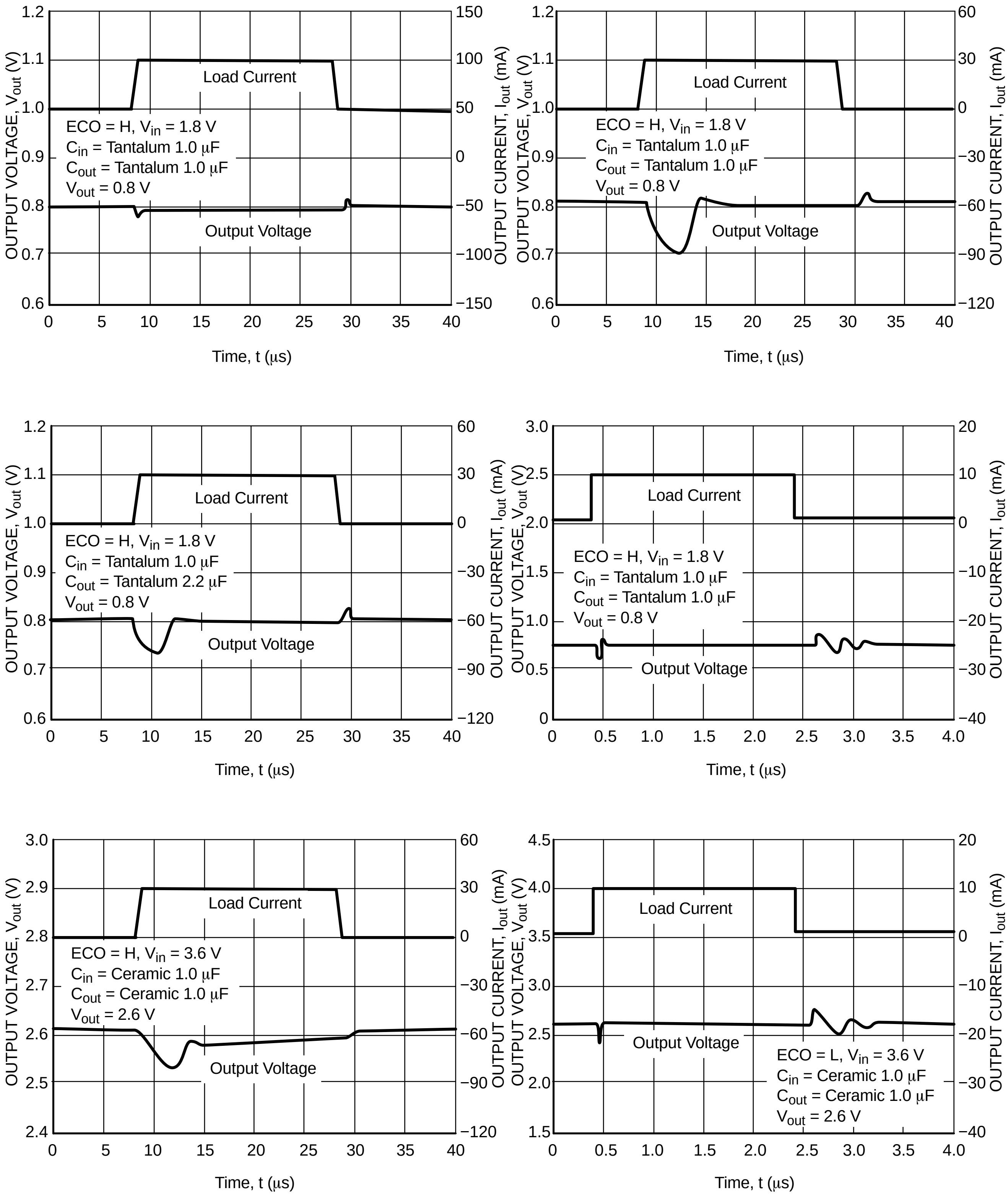


Figure 30. Load Transient Response

TYPICAL CHARACTERISTICS

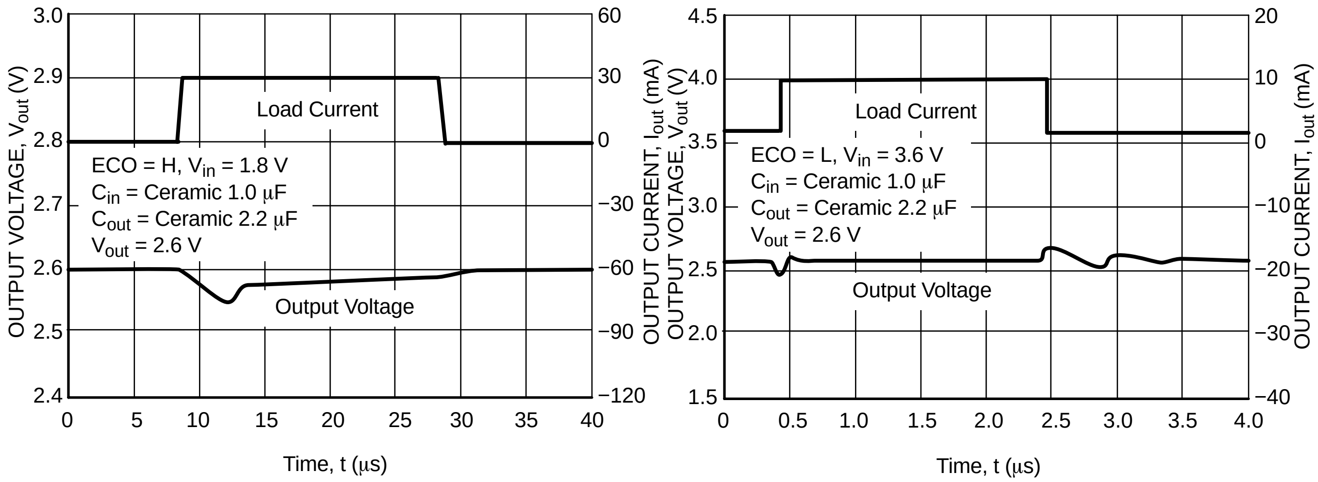


Figure 30. (continued) **Load Transient Response**

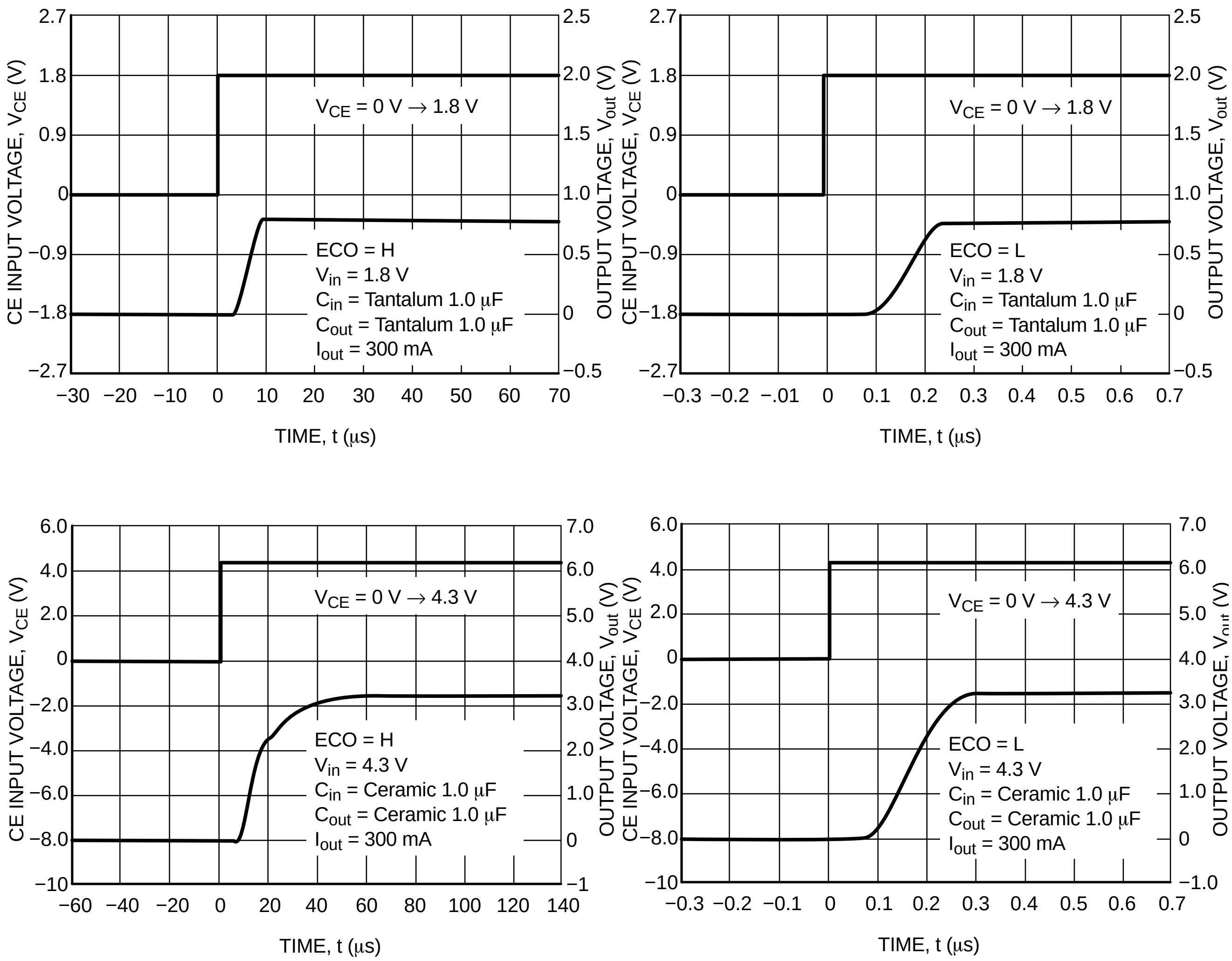
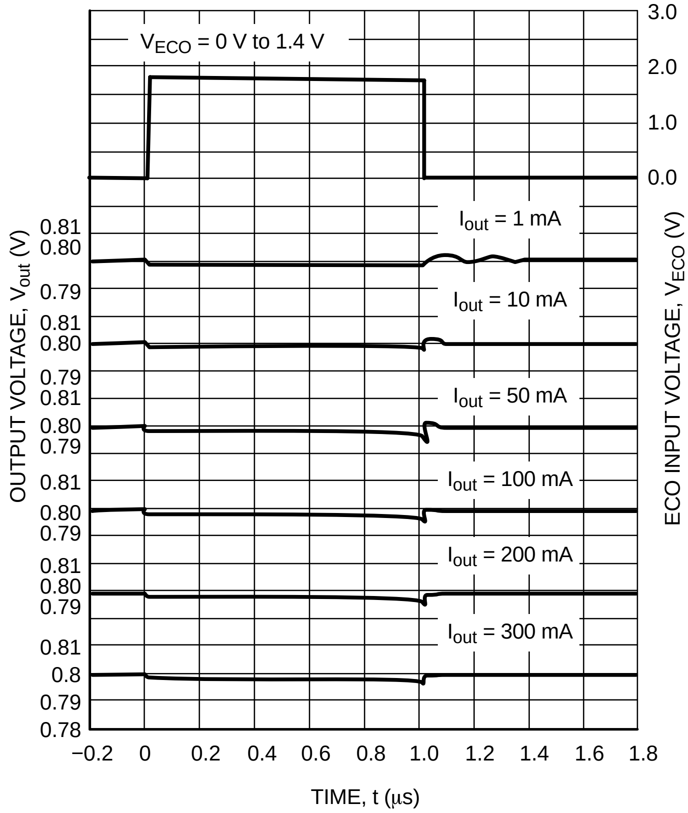


Figure 31. Turn−On Speed with CE Pin, V_{out} = 0.8 V

TYPICAL CHARACTERISTICS

V_{in} = 1.8 V, C_{in} = Tantalum 1.0 μF, C_{out} = Tantalum 1.0 μF, V_{out} = 0.8 V



V_{in} = 2.0 V, C_{in} = Ceramic 1.0 μF, C_{out} = Ceramic 1.0 μF, V_{out} = 1.0 V

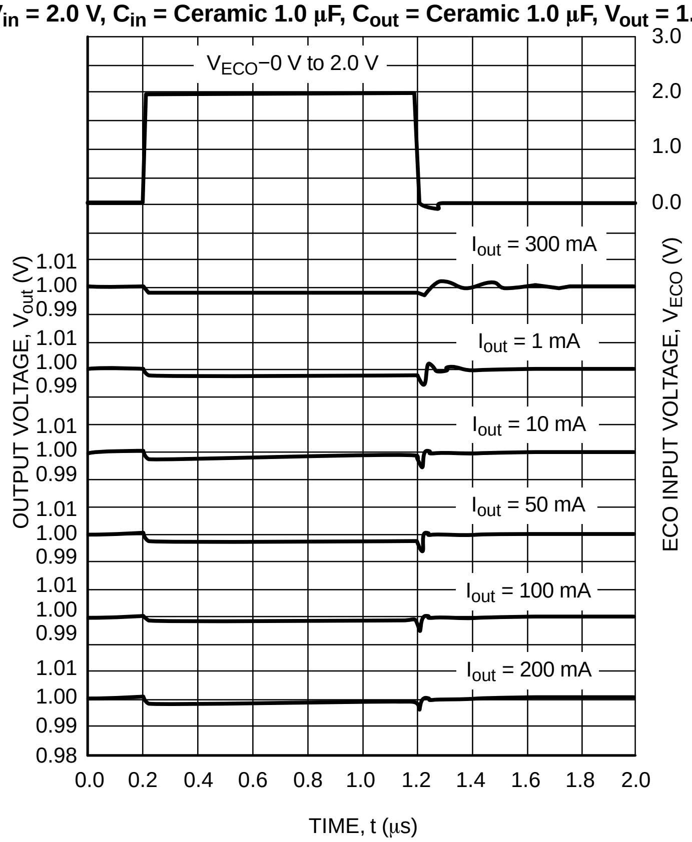


Figure 32. Output Voltage at Mode Alternative Point

APPLICATION INFORMATION

Input Decoupling

A 1.0 μF ceramic capacitor is the recommended value to be connected between V_{in} and GND. For PCB layout considerations, the traces on V_{in} and GND should be sufficiently wide in order to minimize noise and prevent unstable operation.

Output Decoupling

It is best to use a 1.0 μF capacitor value on the V_{out} pin. For better performance, select a capacitor with low Equivalent Series Resistance (ESR). For PCB layout considerations, place the output capacitor close to the output pin and keep the leads short as possible.

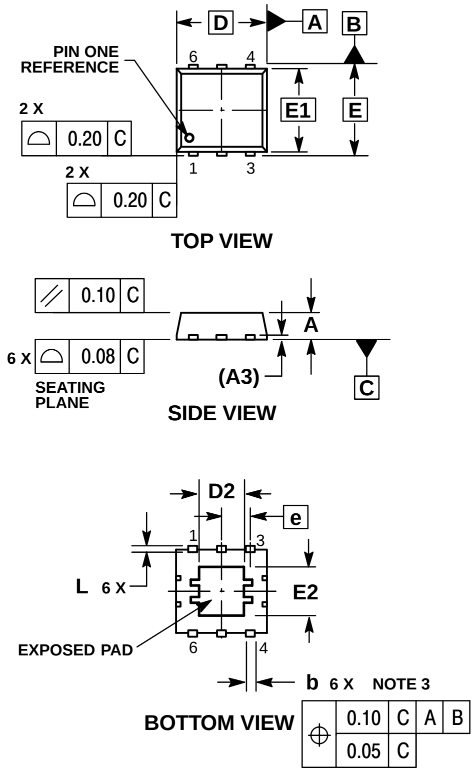
ORDERING INFORMATION

Device	Output Type / Features	Nominal Output Voltage	Marking	Package	Shipping†
NCP585DSAN09T1G	Active High w/Auto Discharge, LP and FT Mode	0.9	B09D	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585DSAN12T1G	Active High w/Auto Discharge, LP and FT Mode	1.2	B12D	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585DSAN18T1G	Active High w/Auto Discharge, LP and FT Mode	1.8	B18D	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585DSN09T1G	Active High w/Auto Discharge, LP and FT Mode	0.9	R09	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585DSN12T1G	Active High w/Auto Discharge, LP and FT Mode	1.2	R12	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585DSN18T1G	Active High w/Auto Discharge, LP and FT Mode	1.8	R18	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585HSAN09T1G	Active High, LP and FT Mode	0.9	B09B	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585HSAN12T1G	Active High, LP and FT Mode	1.2	B12B	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585HSAN18T1G	Active High, LP and FT Mode	1.8	B18B	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585HSN09T1G	Active High, LP and FT Mode	0.9	Q09	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585HSN12T1G	Active High, LP and FT Mode	1.2	Q12	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585HSN18T1G	Active High, LP and FT Mode	1.8	Q18	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585LSAN09T1G	Active Low, LP and FT Mode	0.9	B09A	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585LSAN12T1G	Active Low, LP and FT Mode	1.2	B12A	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585LSAN18T1G	Active Low, LP and FT Mode	1.8	B18A	HSON−6 (Pb−Free)	3000 Tape & Reel
NCP585LSN09T1G	Active Low, LP and FT Mode	0.9	P09	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585LSN12T1G	Active Low, LP and FT Mode	1.2	P12	SOT23−5 (Pb−Free)	3000 Tape & Reel
NCP585LSN18T1G	Active Low, LP and FT Mode	1.8	P18	SOT23−5 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

HSON−6
SAN SUFFIX
CASE 506AE−01
ISSUE A

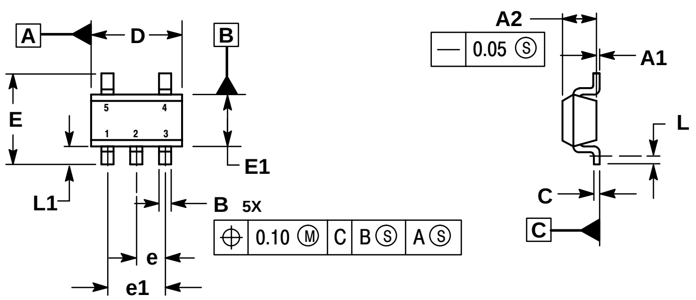


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.15 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.90
A3	0.15 REF	
b	0.20	0.40
D	2.90 BSC	
D2	1.40	1.60
E	3.00 BSC	
E1	2.80 BSC	
E2	1.50	1.70
e	0.95 BSC	
L	0.15	0.25

PACKAGE DIMENSIONS

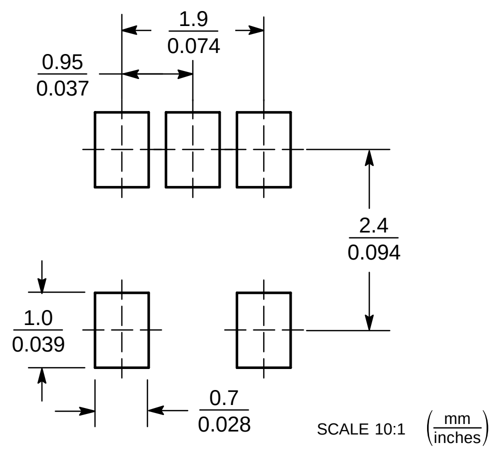
SOT23−5
SN SUFFIX
CASE 1212−01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A1	0.00	0.10
A2	1.00	1.30
B	0.30	0.50
C	0.10	0.25
D	2.80	3.00
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	---
L1	0.45	0.75

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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