

# NCP4672

## Dual Linear Voltage Regulators with $V_{in}$ and $V_{out}$ Voltage Detector

The NCP4672 is a dual linear voltage regulator with input voltage and output voltage detectors. This part is useful in systems where multiple voltages are required such as for core and I/O. The NCP4672 is very accurate at 2% over full input voltage and full load current. The NCP4672 eliminates the need for external voltage supervision due to the two built in voltage detectors. The voltage detector on the input is set to 7.0 V. The output voltage detector is for channel 1 and is set to 2.9 V. An external capacitor is used to set the duration of this reset signal. Other features include short circuit protection and thermal shutdown protection. The NCP4672 has been designed to work with a 4.7  $\mu\text{F}$  output capacitor having an ESR between 0.1  $\Omega$  and 5.0  $\Omega$ .

### Features

- Accuracy: 2% at Full Voltage and Load
- Excellent Ripple Rejection: 70 dB @ 1 kHz
- Voltage Detector for Input Voltage
- Voltage Detector for Output Voltage
- Programmable Delay of Reset Signal
- Thermal Short Circuit Protection
- This is a Pb-Free Device

### Typical Application

- Small Core and I/O Power
- Consumer Equipment
- Measurement Equipment
- Industrial Equipment

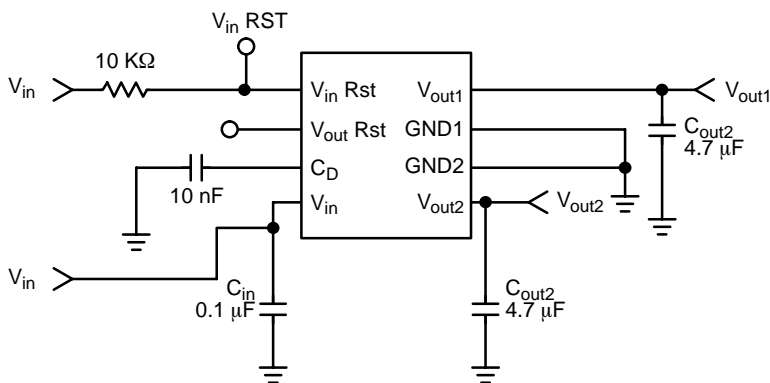


Figure 1. Typical Application Circuit



ON Semiconductor®

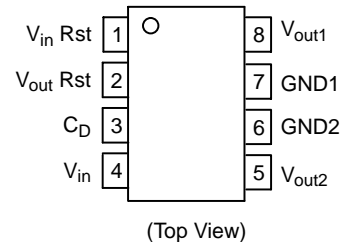
<http://onsemi.com>

### MARKING DIAGRAM



4672G = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 YW = Date Code

### PIN CONFIGURATION



### ORDERING INFORMATION

| Device      | Package          | Shipping†        |
|-------------|------------------|------------------|
| NCP4672DR2G | SOIC-8 (Pb-Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP4672

## MAXIMUM RATINGS

| Rating   | Symbol                         | Value                  | Unit     |
|--|--------------------------------|------------------------|----------|
| Input Voltage  | $V_{inmax}$                    | -0.3 ~ 18              | V        |
| Output Voltage   | $V_{out}$                      | -0.3 to $V_{in} + 0.3$ | V        |
| Output Current 1<br>Output Current 2                   | $I_{out1max}$<br>$I_{out2max}$ | 30<br>80               | mA<br>mA |
| Output Short Circuit Duration                          | -                              | Infinite               | -        |
| Power Dissipation and Thermal Characteristics – SOIC-8 |                                |                        |          |
| Power Dissipation                                      | $P_D$                          | Internally Limited     | W        |
| Thermal Resistance, Junction-to-Ambient                | $R_{\theta JA}$                | 190                    | °C/W     |
| Minimum Pad Size                                       |                                | 160                    | °C/W     |
| 200 mm <sup>2</sup> Pad Size (Note 1)                  |                                | 25                     | °C/W     |
| Thermal Resistance, Junction-to-Case                   | $R_{\theta JC}$                |                        |          |
| Operating Junction Temperature Range                   | $T_{stg}$                      | -40 to 125             | °C       |
| Storage Temperature Range                              | $T_{solder}$                   | -55 to 150             | °C       |

1. Refer to Figure 4 for more information.

## PIN DESCRIPTION

| Pin Number | Symbol       | Description   |
|------------|--------------|---|
| 1          | $V_{in RST}$ | Open-collector, active-low output of the input voltage detector with hysteresis. Threshold levels are typical 7.0 V/ 7.35 V at $V_{CC}$ pin.  |
| 2          | $V_o RST$    | Active-low output of the reset generator. Reset generator is based on sensing of the $V_{out1}$ voltage. Sensing is with hysteresis – threshold levels are typically 2.9 V/ 2.95 V at $V_{out1}$ . Reset is generated at rising edge of the $V_{out1}$ and it's duration is set by external capacitor connected to $C_D$ pin. |
| 3          | $C_D$        | Programmable delay of the reset generator. Delay is adjusted by inserting a capacitor between $C_D$ and GND (typically 10 ms for 10 nF capacitor).  |
| 4          | $V_{CC}$     | Supply Voltage  |
| 5          | $V_{out2}$   | 1.8 V/ 80 mA LDO Regulator Output   |
| 6          | GND2         | Ground for $V_{out2}$ (internally connected with GND1)  |
| 7          | GND1         | Ground for $V_{out1}$ (internally connected with GND2)  |
| 8          | $V_{out1}$   | 3.5 V/30 mA LDO Regulator Output  |

**Recommended Conditions** ( $T_A = 25^\circ\text{C}$ ,  $C_{in} = 0.1 \mu\text{F}$  Ceramic,  $C_{out} = 4.7 \mu\text{F}$ )

| Characteristics  | Symbol                   | Min    | Typ    | Max      | Unit |
|--|--------------------------|--------|--------|----------|------|
| Input Voltage  | $V_{in}$                 | 3.8    | 12     | 16       | V    |
| Output Current (where $V_{out}$ remains within accuracy) | $I_{out1}$<br>$I_{out2}$ | 0<br>0 | -<br>- | 20<br>70 | mA   |

# NCP4672

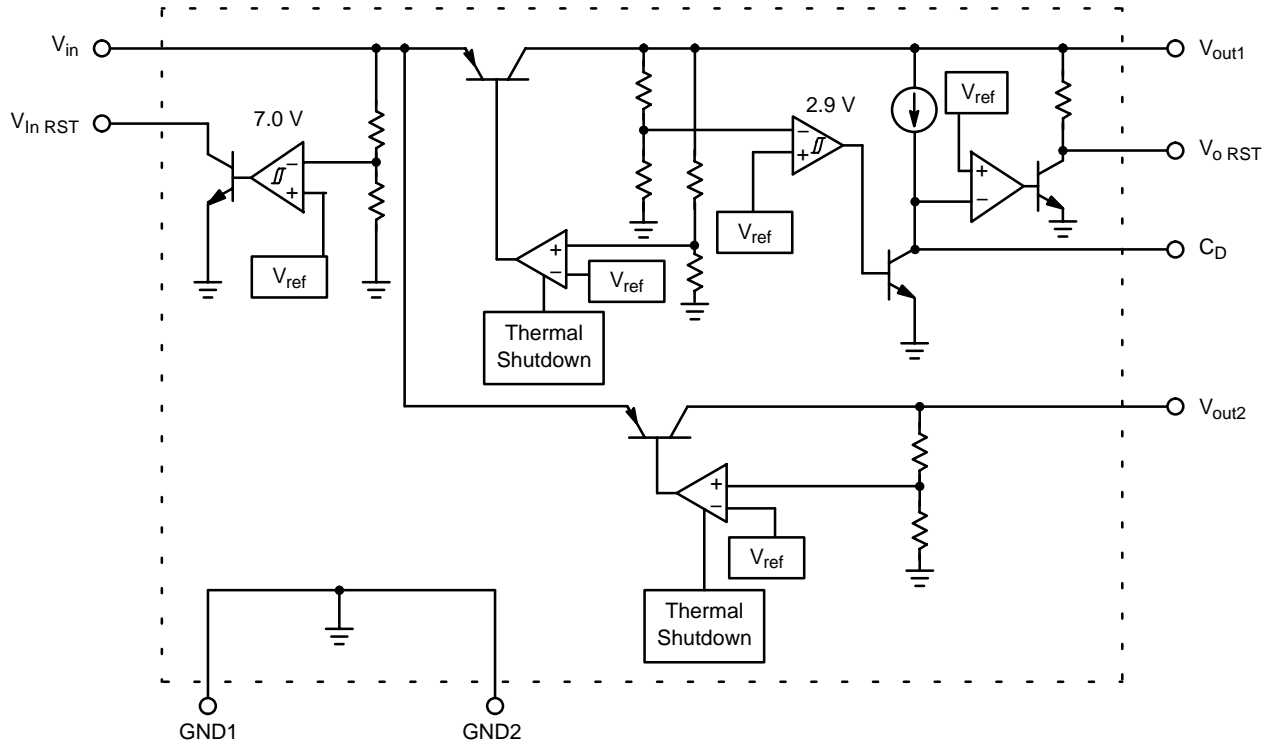


Figure 1.

# NCP4672

## ELECTRICAL CHARACTERISTICS (C<sub>in</sub> = 0.1 μF Ceramic, C<sub>out</sub> = 4.7 μF with ESR = 0.1 – 5.0 Ω, V<sub>in</sub> = 12 V, T<sub>A</sub> = 25°C)

| Characteristics   | Symbol                              | Min           | Typ        | Max           | Unit              |
|---|-------------------------------------|---------------|------------|---------------|-------------------|
| Output Voltage<br>V <sub>out1</sub> (V <sub>in</sub> = 4.5 V, I <sub>out1</sub> = 20 mA)<br>V <sub>out2</sub> (V <sub>in</sub> = 4.5 V, I <sub>out2</sub> = 40 mA)  | V <sub>adj</sub>                    | 3.43<br>1.764 | 3.5<br>1.8 | 3.57<br>1.836 | V                 |
| Line Regulation<br>V <sub>out1</sub> (V <sub>in</sub> = 4.5 V, I <sub>out1</sub> = 20 mA)<br>V <sub>out2</sub> (V <sub>in</sub> = 4.5 V to 10 V, I <sub>out2</sub> = 40 mA)   | Reg <sub>line</sub>                 | –<br>–        | 3.0<br>3.0 | 30<br>30      | mV                |
| Load Regulation<br>V <sub>out1</sub> (V <sub>in</sub> = 4.5 V, I <sub>out1</sub> = 0.1 mA to 20 mA)<br>V <sub>out2</sub> (V <sub>in</sub> = 4.5 V, I <sub>out2</sub> = 0.1 mA to 70 mA)   | Reg <sub>load</sub>                 | –<br>–        | 3.0<br>2.0 | 40<br>40      | mV                |
| Dropout Voltage<br>V <sub>out1</sub> (V <sub>in</sub> = 3.3 V, I <sub>out1</sub> = 20 mA)   | V <sub>in</sub> – V <sub>out1</sub> | –             | 150        | 300           | mV                |
| Ground Pin Current<br>(V <sub>in</sub> = 8.0 V, I <sub>out1</sub> = I <sub>out2</sub> = 0 mA)<br>(V <sub>in</sub> = 2.7 V, I <sub>out1</sub> = I <sub>out2</sub> = 0 mA, R <sub>pu</sub> = infinite)  | I <sub>GND</sub>                    | –<br>–        | 1.0<br>3.0 | 2.0<br>–      | mA                |
| Short Current Limit<br>V <sub>out1</sub><br>V <sub>out2</sub>   | I <sub>SC</sub>                     | 30<br>80      | 60<br>150  | –<br>–        | mA                |
| Thermal Shutdown  |                                     | –             | 165        | –             | °C                |
| Temperature Coefficient<br>V <sub>out1</sub> (T <sub>J</sub> = –30 to 85°C, V <sub>in</sub> = 4.5 V, I <sub>out1</sub> = 20 mA)<br>V <sub>out2</sub> (T <sub>J</sub> = –30 to 85°C, V <sub>in</sub> = 4.5 V, I <sub>out2</sub> = 40 mA)                 | T <sub>C</sub>                      | –<br>–        | 100<br>100 | –<br>–        | ppm/°C            |
| Ripple Rejection (Note 6)<br>V <sub>out1</sub> (V <sub>in</sub> = 4.5 V, V <sub>ripple</sub> = 1.0 V, I <sub>out1</sub> = 20 mA, 120 Hz)<br>V <sub>out2</sub> (V <sub>in</sub> = 4.5 V, V <sub>ripple</sub> = 1.0 V, I <sub>out2</sub> = 40 mA, 120 Hz) | R <sub>R</sub>                      | –<br>–        | 65<br>70   | –<br>–        | dB                |
| Output Noise Voltage<br>V <sub>out1</sub> (V <sub>in</sub> = 4.5 V, f = 20 Hz – 80 kHz, I <sub>out1</sub> = 20 mA)<br>V <sub>out2</sub> (V <sub>in</sub> = 4.5 V, f = 20 Hz – 80 kHz, I <sub>out2</sub> = 40 mA)  | V <sub>n</sub>                      | –<br>–        | 80<br>50   | –<br>–        | μV <sub>rms</sub> |

### V<sub>in</sub> Detect

|   |                                  |      |      |      |        |
|---|----------------------------------|------|------|------|--------|
| Detecting Voltage L (V <sub>in</sub> = H to L)  | V <sub>SLin</sub>                | 6.72 | 7.0  | 7.28 | V      |
| Detecting Voltage H (V <sub>in</sub> = L to H)  | V <sub>SHin</sub>                | –    | 7.35 | –    | V      |
| Hysteresis Voltage (V <sub>in</sub> = H to L to H)  | Δ V <sub>Sin</sub>               | 140  | 350  | 560  | mV     |
| V <sub>SLin</sub> Temperature Coefficient (T <sub>J</sub> = –30°C to +85°C)                                   | V <sub>SLin</sub> T <sub>C</sub> | –    | 100  | –    | ppm/°C |
| Low-Level Output Voltage (V <sub>in</sub> = 6.0 V, V <sub>t1</sub> = 5.0 V, R <sub>t1</sub> = 10 kΩ) (Note 5) | V <sub>OLin1</sub>               | –    | 100  | 200  | mV     |
| Threshold Operating Voltage (V <sub>OPLin</sub> = V <sub>t1</sub> = 1.0 V)                                    | V <sub>OLin2</sub>               | –    | –    | 0.4  | V      |

### V<sub>out</sub> Detect

|   |                                  |      |      |       |        |
|---|----------------------------------|------|------|-------|--------|
| Detecting Voltage L (V <sub>in</sub> = H to L)                              | V <sub>SLout</sub>               | 2.78 | 2.9  | 3.020 | V      |
| Detecting Voltage H (V <sub>in</sub> = L to H)                              | V <sub>SHout</sub>               | –    | 2.95 | –     | V      |
| Hysteresis Voltage (V <sub>in</sub> = H to L to H)                          | Δ V <sub>Sout</sub>              | 25   | 50   | 100   | mV     |
| V <sub>SLin</sub> Temperature Coefficient (T <sub>J</sub> = –30°C to +85°C) | V <sub>SLin</sub> T <sub>C</sub> | –    | 100  | –     | ppm/°C |
| Low-Level Output Voltage (V <sub>out1</sub> = 2.6 V)                        | V <sub>OLout1</sub>              | –    | 100  | 200   | mV     |
| Threshold Operating Voltage (V <sub>OPLout</sub> = 0.85 V)                  | V <sub>OLout2</sub>              | –    | –    | 0.4   | V      |
| Reset Delay Time (C <sub>D</sub> = 10 nF)                                   | t <sub>PLH</sub>                 | 5    | 10   | 15    | ms     |
| “L” Transmission Delay Time (C <sub>D</sub> = 10 nF)                        | t <sub>PHL</sub>                 | –    | 30   | 90    | μs     |

2. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015  
Machine Model Method 200 V.

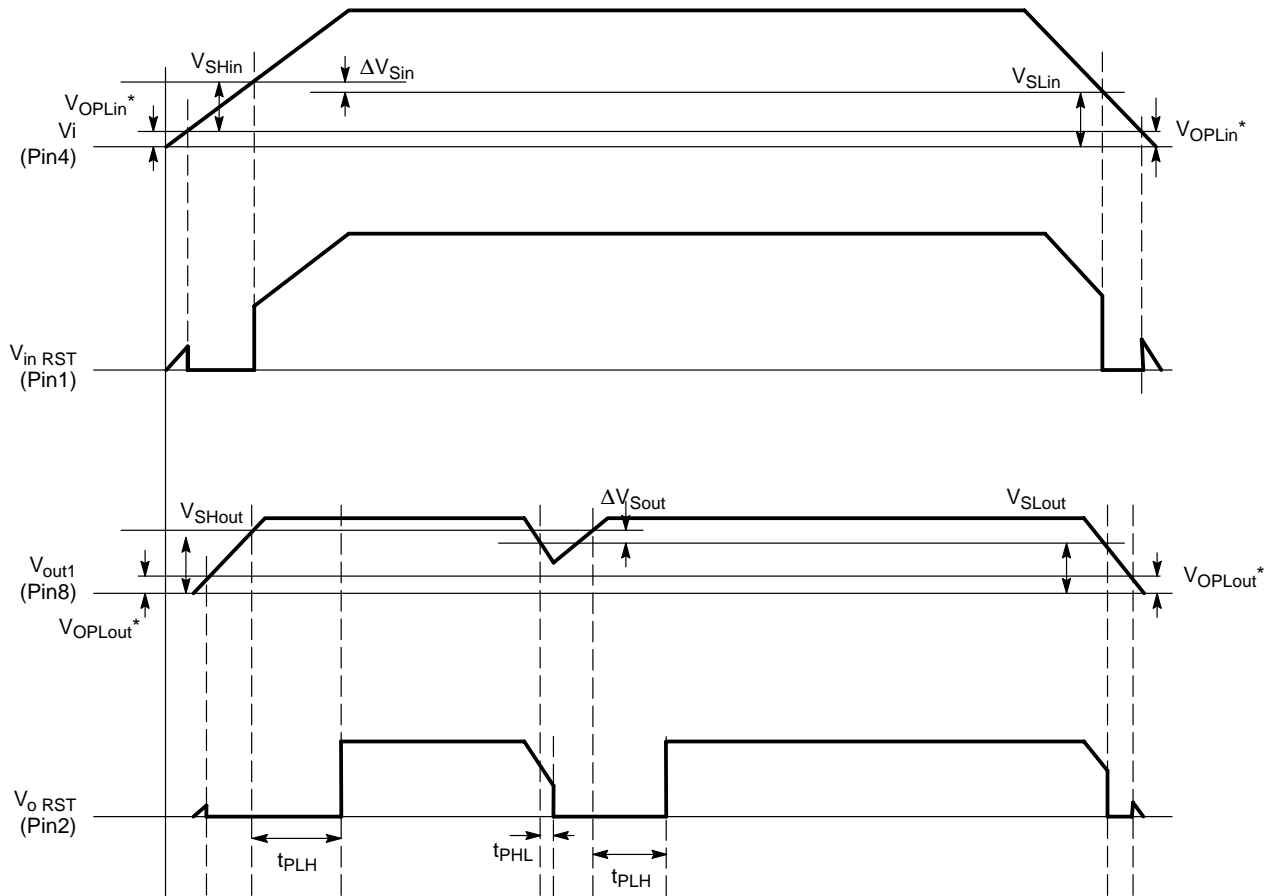
3. The maximum package power dissipation is:  $P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

5. Refer to Figure 3.

6. Guaranteed by design.

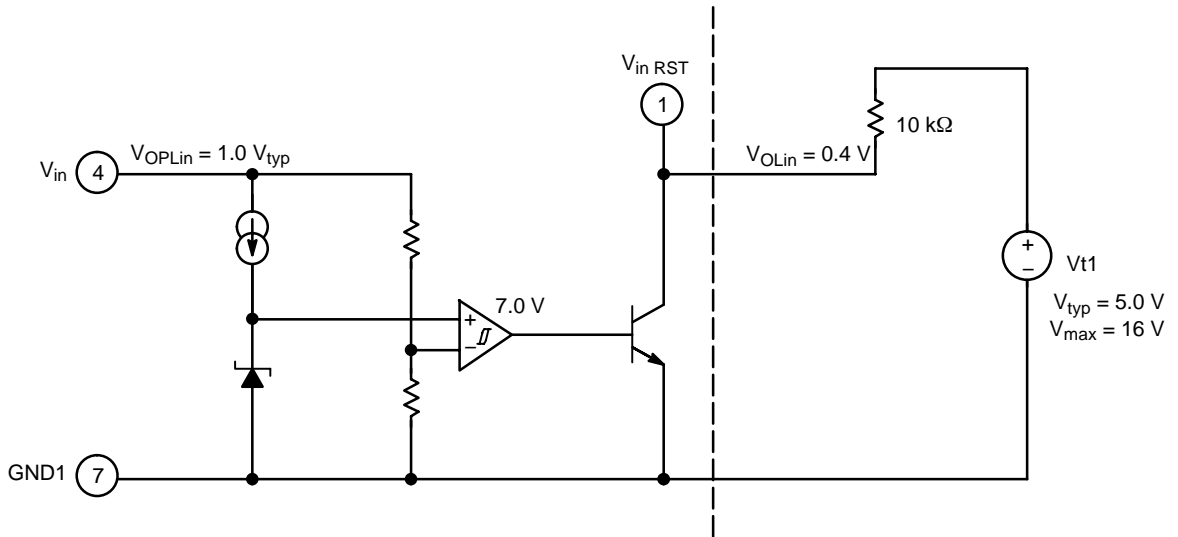
# NCP4672



\*;  $V_{OPLin}$  shows theoretical on this chart.  
 $V_{OPLin}$  spec. must be specified on Pin 1 voltage (0.4 V)

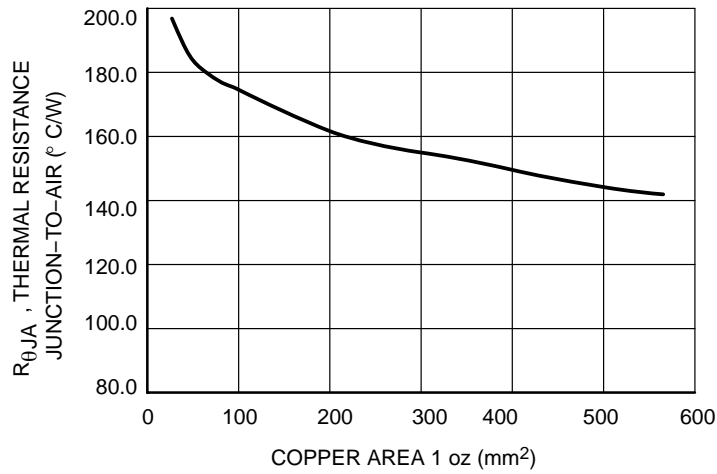
\*;  $V_{OPLout}$  shows theoretical on this chart.  
 $V_{OPLout}$  spec. must be specified on Pin 2 voltage (0.4 V)

**Figure 2. Dual Regulator Timing**

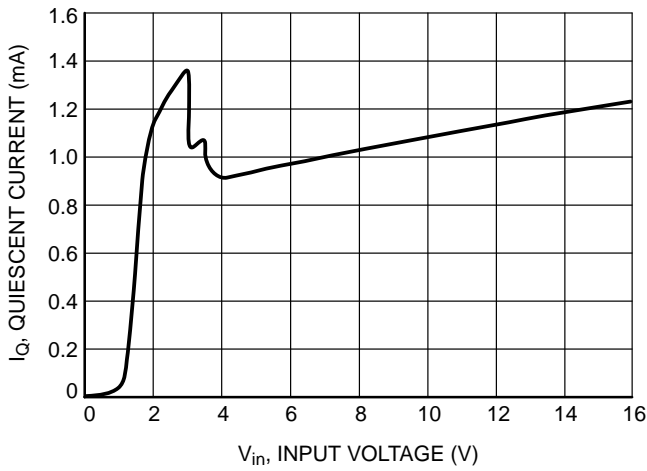


**Figure 3. Threshold Operating Voltage  $V_{OPLin}$  Under Condition  $V_{OLin} = 0.4$  V**

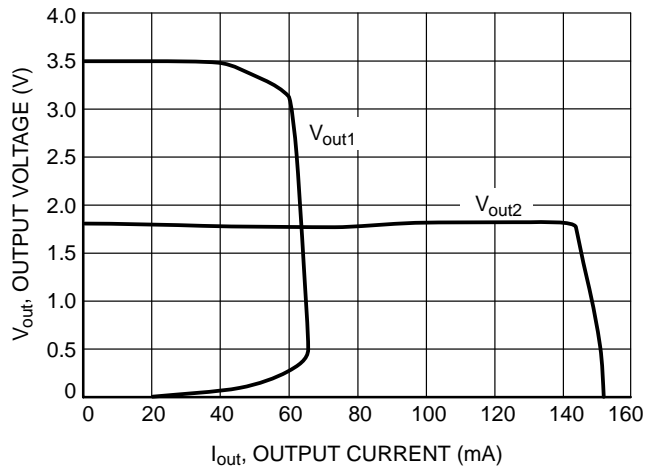
# NCP4672



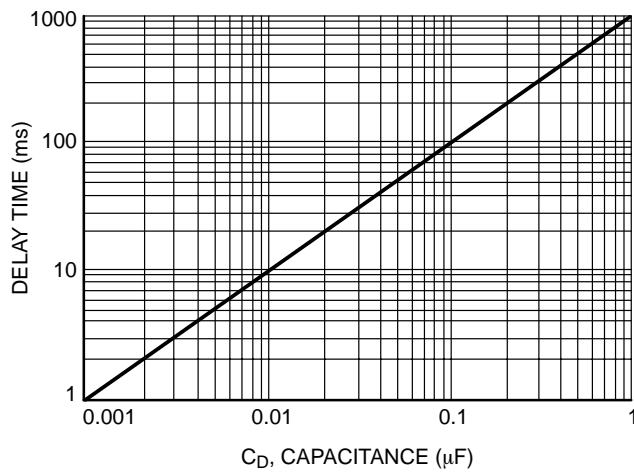
**Figure 4. SOP-8 Thermal Resistance versus P.C.B. Copper Area**



**Figure 5. Quiescent Current versus Input Voltage**



**Figure 6. Peak Current Limit**



**Figure 7. Delay Time versus Capacitance**

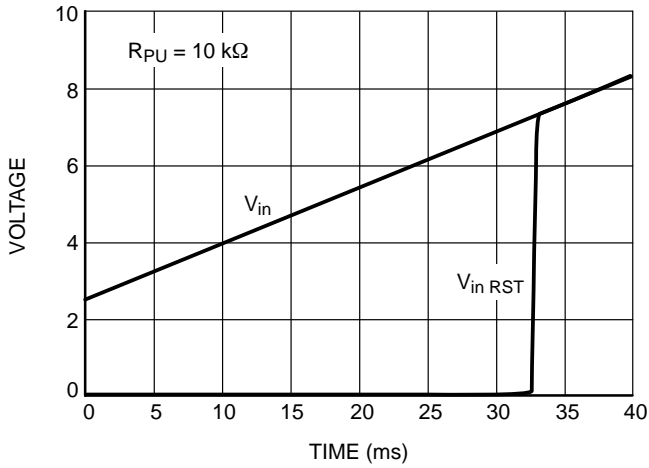


Figure 8.  $V_{in}$  and  $V_{in RST}$  versus Time

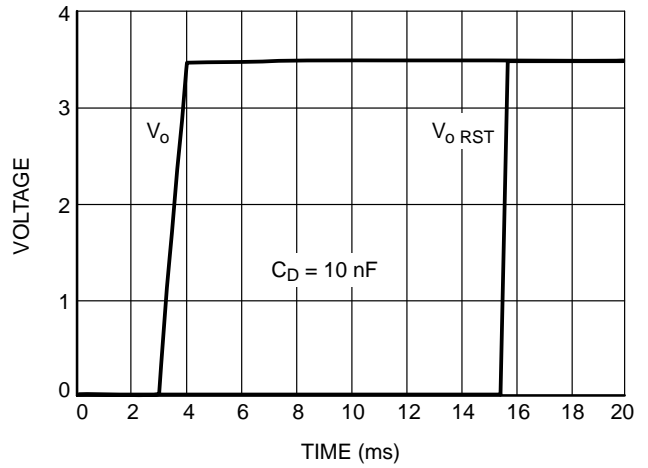


Figure 9.  $V_o$  and  $V_o RST$  versus Time

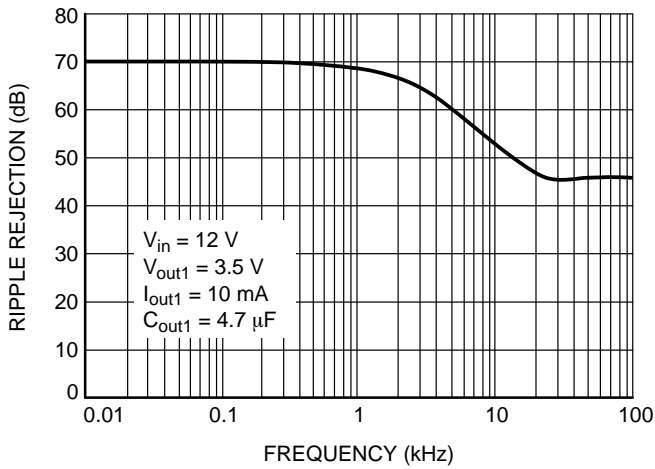


Figure 10.  $V_{out1}$  Ripple Rejection

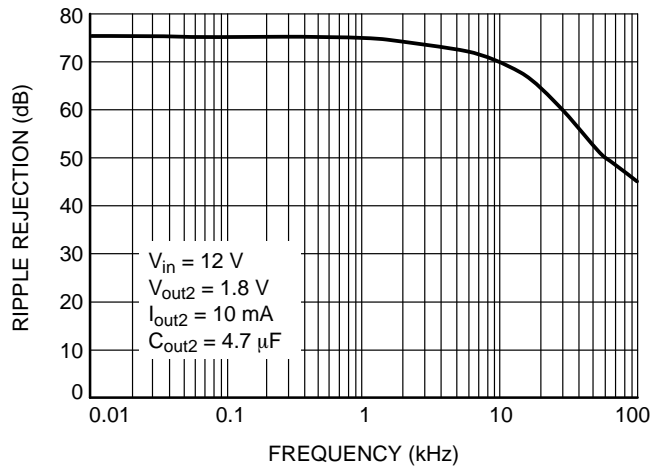
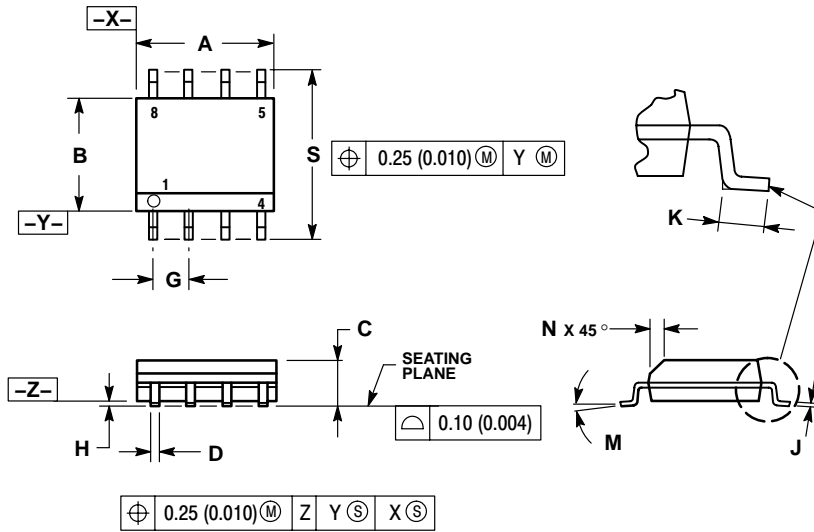


Figure 11.  $V_{out2}$  Ripple Rejection

# NCP4672

## PACKAGE DIMENSIONS

SOIC-8  
NB SUFFIX  
CASE 751-07  
ISSUE AB

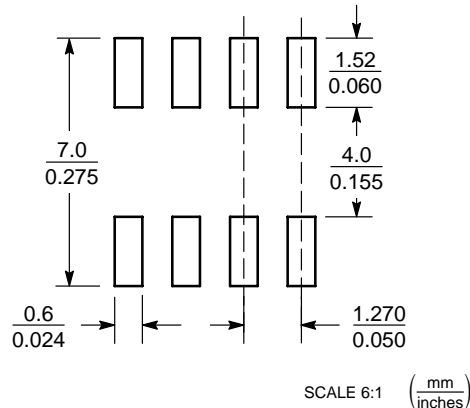


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



### SOIC-8

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.