

# DATA SHEET

**74F564**

Octal D flip-flop (3-State)

Product specification

1996 Jan 05

IC15 Data Handbook

# Octal D flip-flop (3-State)

# 74F564

## FEATURES

- 74F564 is broadside pinout version of 74F534
- Inputs and Outputs on opposite side of package allow easy interface to Microprocessors
- Useful as an Input or Output port for Microprocessors
- 3-State Outputs for Bus interfacing
- Common Output Enable
- 74F574 is a non-inverting version of 74F564

## DESCRIPTION

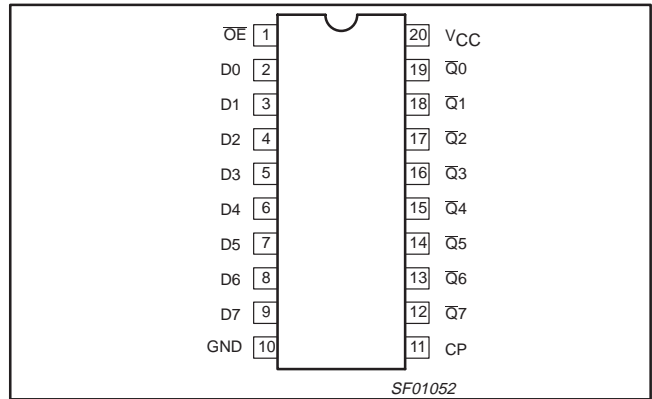
The 74F564 has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ( $\overline{OE}$ ) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's  $\overline{Q}$  output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independently of the register operation. When  $\overline{OE}$  is Low, data in the register appears at the outputs. When  $\overline{OE}$  is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F564	180MHz	50mA

## ORDERING INFORMATION

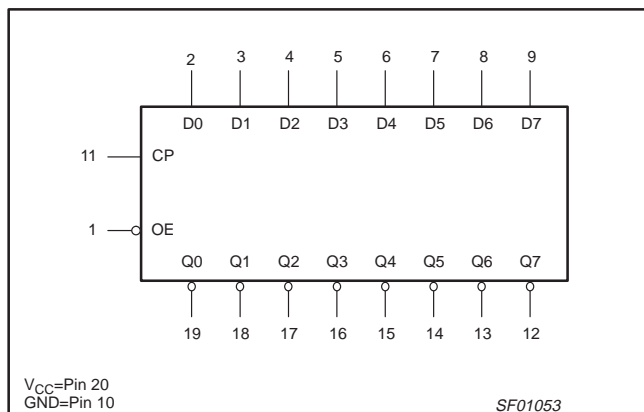
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG. DWG #
20-Pin Plastic DIP	N74F564N	SOT146-1
20-Pin Plastic SOL	N74F564D	SOT163-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

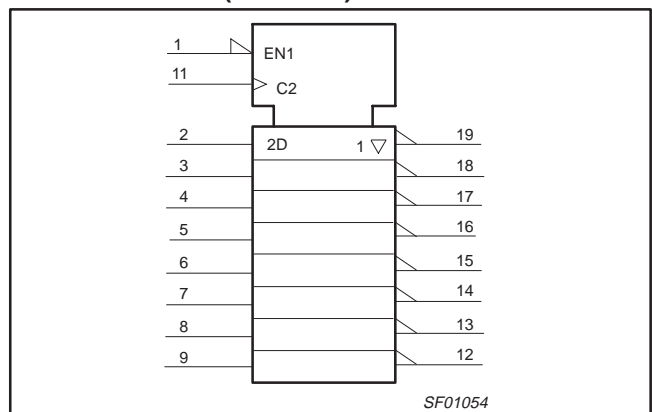
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{Q0} - \overline{Q7}$	3-State outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL



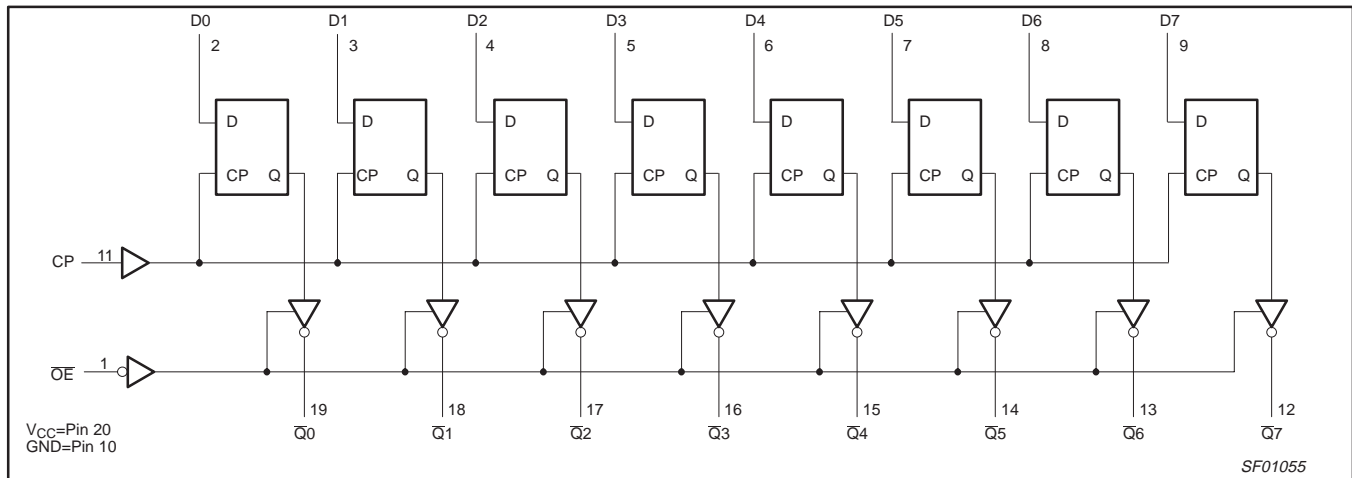
## LOGIC SYMBOL (IEEE/IEC)



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## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
OE	CP	Dn		Q0 – Q7	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

- H = High voltage level
- h = High voltage level one setup time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one setup time prior to the Low-to-High clock transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↑ = Low-to-High clock transition
- ↕ = Not a Low-to-High clock transition

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5.0	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to +V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	48	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-3	mA
$I_{OL}$	Low-level output current			24	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>NO TAG</sup>	LIMITS			UNIT	
			MIN	TYP NO TAG	MAX		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.4		V	
			$\pm 5\%V_{CC}$	2.7	3.4	V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
			$\pm 5\%V_{CC}$		0.35	0.50	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	$\mu\text{A}$	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	$\mu\text{A}$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
$I_{OZH}$	Off-state output current, High-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7V$			50	$\mu\text{A}$	
$I_{OZL}$	Off-state output current, Low-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.5V$			-50	$\mu\text{A}$	
$I_{OS}$	Short-circuit output current <sup>NO TAG</sup>	$V_{CC} = \text{MAX}$	-60		-150	mA	
$I_{CC}$	Supply current (total)	$I_{CCH}$		45	65	mA	
		$I_{CCL}$		50	75	mA	
		$I_{CCZ}$		55	80	mA	

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5V, T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum Clock frequency	Waveform NO TAG	160	180		150		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	Waveform NO TAG	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	8.5 8.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.5 4.0	4.5 5.5	7.5 8.0	2.0 3.5	8.0 8.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns

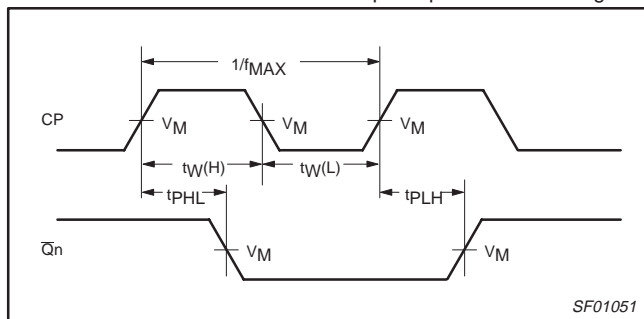
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, D <sub>n</sub> to CP	Waveform 3	2.0 2.0			2.0 2.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, D <sub>n</sub> to CP	Waveform 3	1.0 1.0			1.5 1.5		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP pulse width, High or Low	Waveform NO TAG	3.5 3.5			3.5 3.5		ns

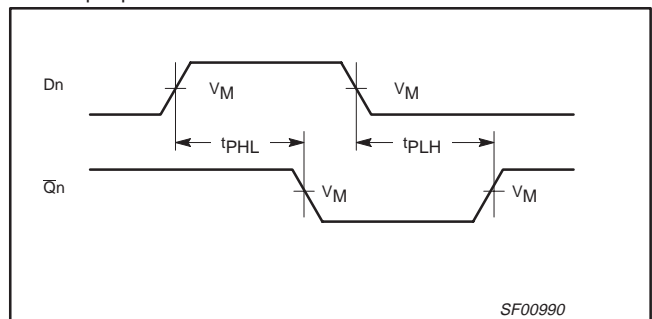
## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



**Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency**



**Waveform 2. Propagation Delay for Data to Outputs**

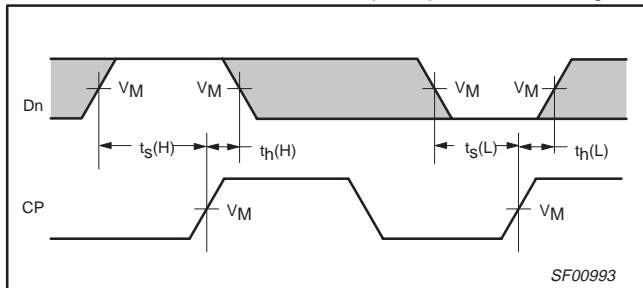
# Octal D flip-flop (3-State)

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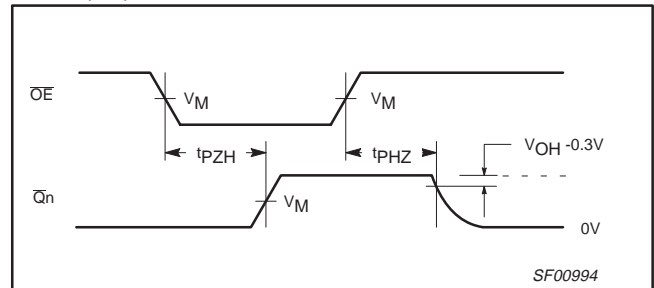
## AC WAVEFORMS (Continued)

For all waveforms,  $V_M = 1.5V$

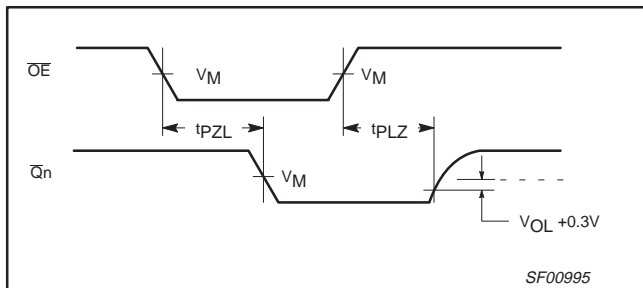
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 3. Data Setup and Hold Times



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

## TEST CIRCUIT AND WAVEFORM

**Test Circuit for 3-State Outputs**

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

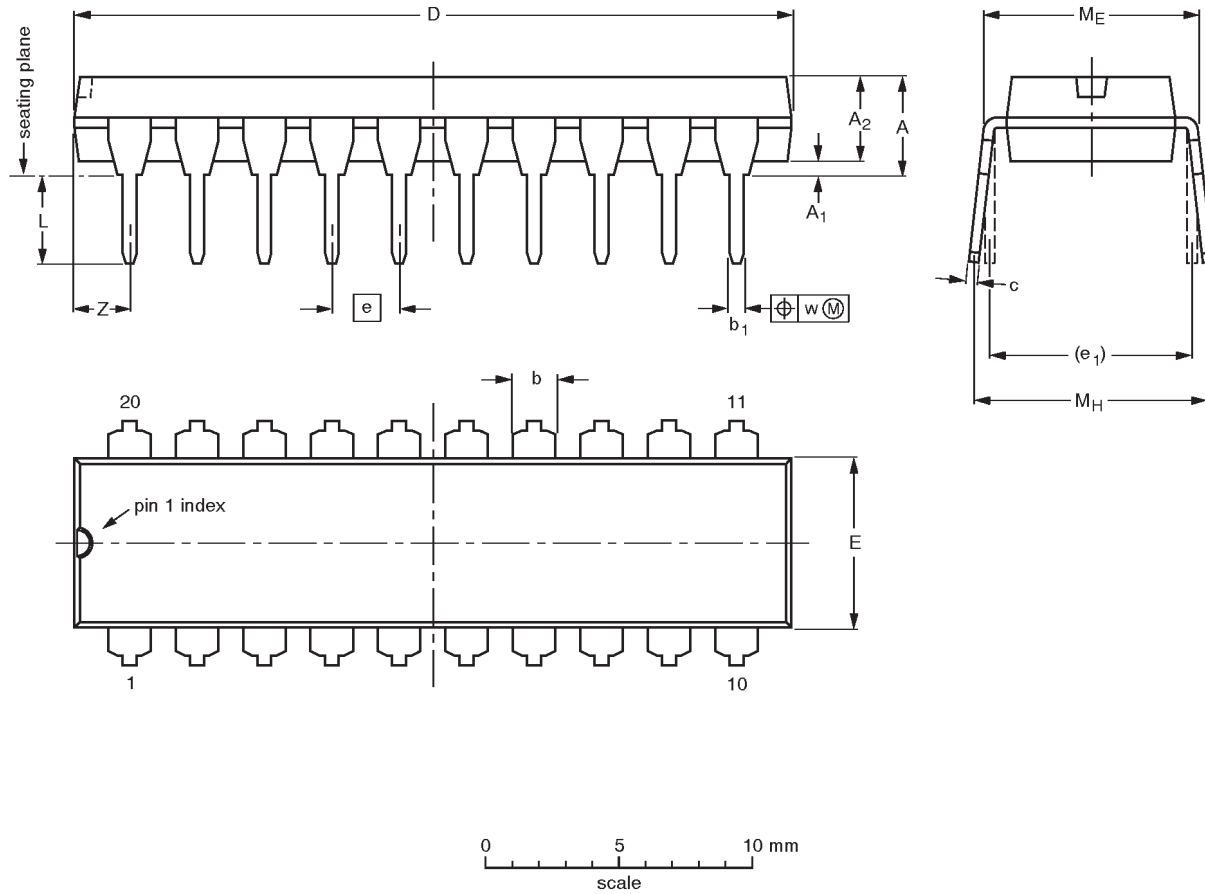
SF00777

# Octal D flip-flop (3-State)

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

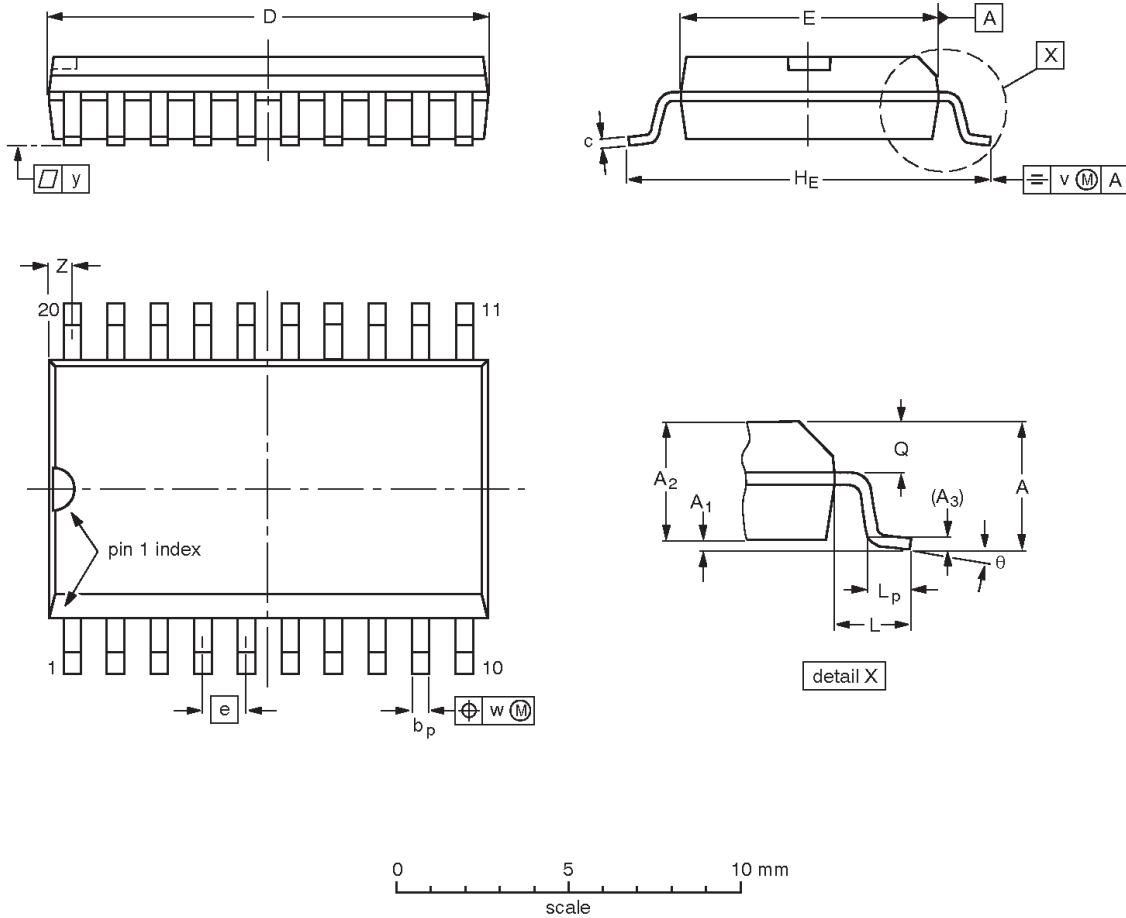
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Octal D flip-flop (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22



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**NOTES**

## Octal D flip-flop (3-State)

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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