

# DATA SHEET

**74F299**

8-bit universal shift/storage register  
(3-State)

Product specification

1990 Mar 01

IC15 Data Handbook

## 8-bit universal shift/storage register (3-State)

74F299

## FEATURES

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: Shift left, shift right, load and store
- 3-State outputs for bus-oriented applications

## DESCRIPTION

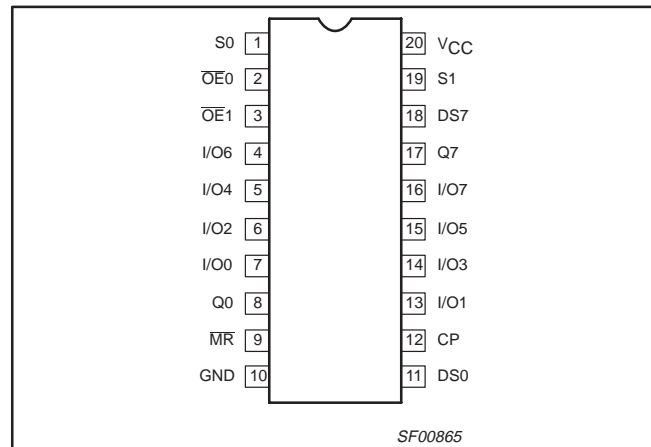
The 74F299 is an 8-bit universal shift/storage register with 3-State outputs. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

The 74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S0 and S1, as shown in the Function Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on  $\overline{MR}$  overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of clock are observed.

A High signal on either  $\overline{OE}0$  or  $\overline{OE}1$  disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S0 and S1 in preparation for a parallel load operation.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	115MHz	58mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
20-pin plastic DIP	N74F299N	SOT146-1
20-pin plastic SOL	N74F299D	SOT163-1
20-pin plastic SSOP II	N74F299DB	SOT339-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

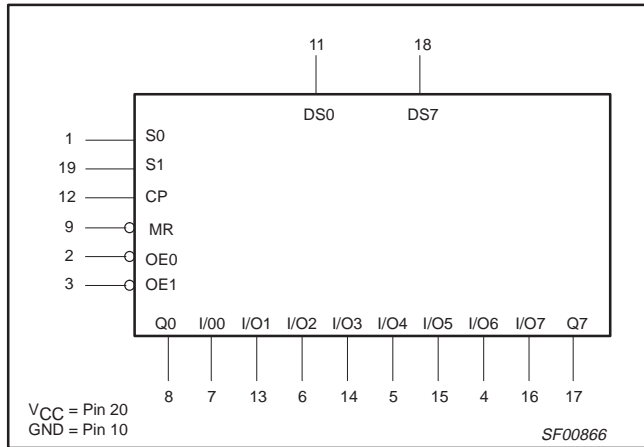
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS0	Serial data input for right shift	1.0/1.0	20 $\mu$ A/0.6mA
DS7	Serial data input for left shift	1.0/1.0	20 $\mu$ A/0.6mA
S0, S1	Mode select inputs	1.0/2.0	20 $\mu$ A/1.2mA
CP	Clock pulse input (Active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (Active Low)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{OE}0, \overline{OE}1$	Output Enable input (Active Low)	1.0/1.0	20 $\mu$ A/0.6mA
Q0, Q7	Serial outputs	50/33	1.0mA/20mA
I/On	Multiplexed parallel data inputs or	3.5/1.0	70 $\mu$ A/0.6mA
	3-State parallel outputs	150/40	3.0mA/24mA

**NOTE:** One (1.0) FAST Unit Load (U.L.) is defined as: 20 $\mu$ A in the High State and 0.6mA in the Low state.

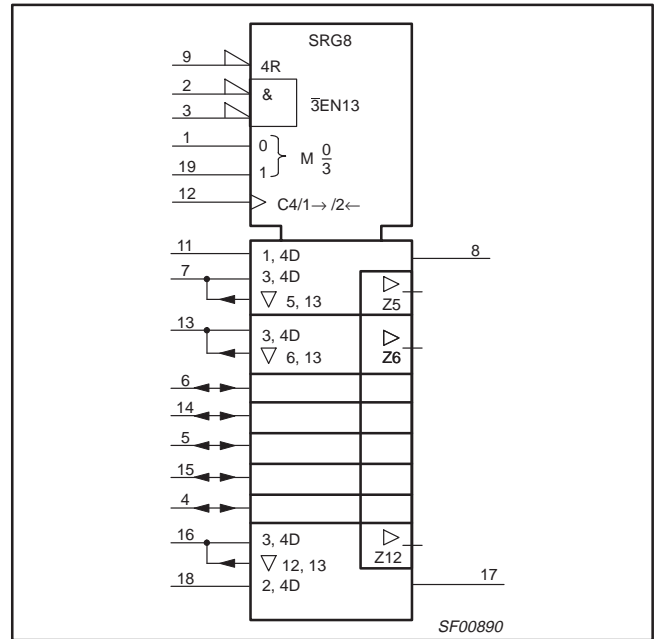
# 8-bit universal shift/storage register (3-State)

74F299

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## FUNCTION TABLE

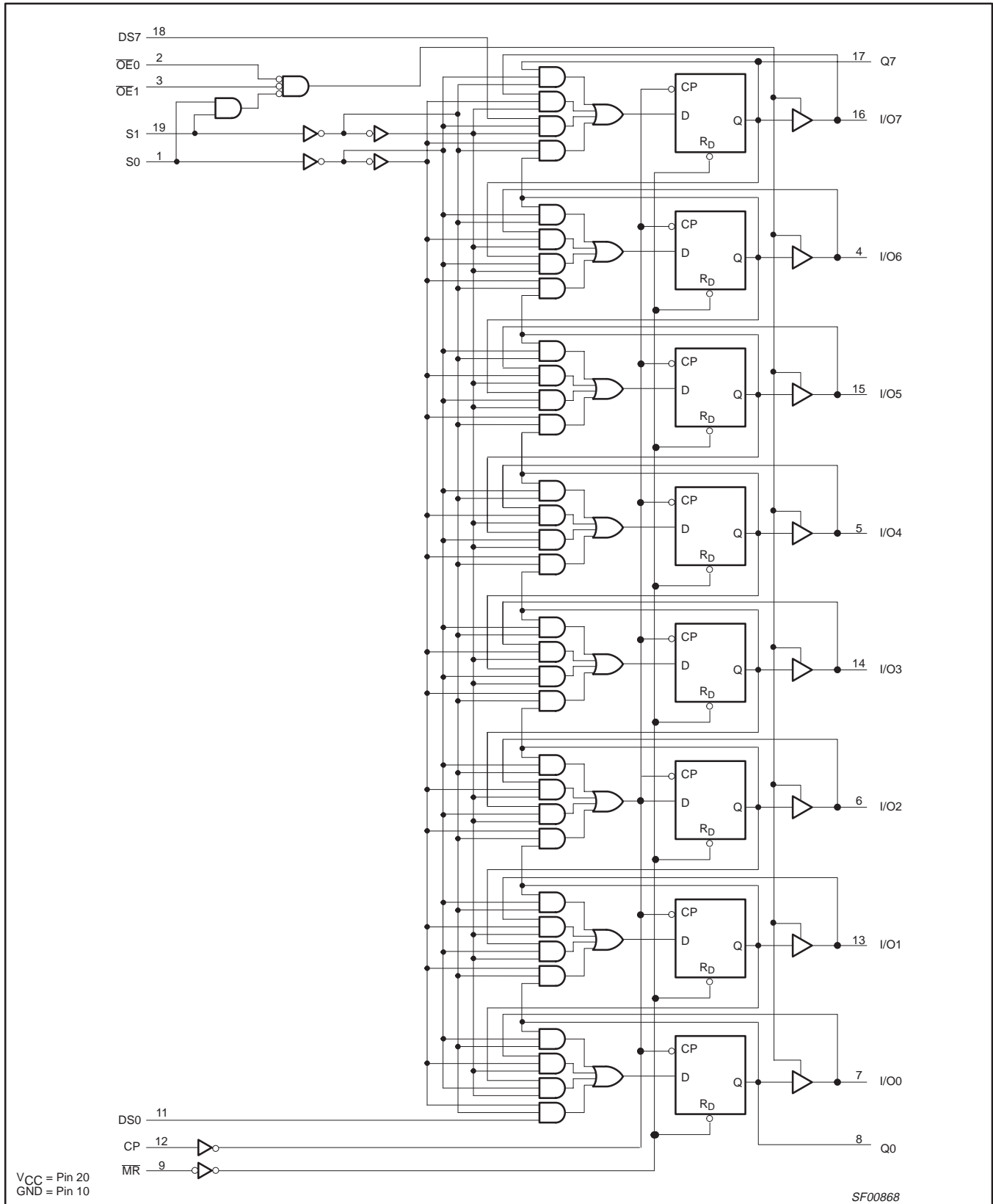
INPUTS		INPUTS			OPERATING MODE
$\overline{OEn}$	MR	S1	S0	CP	
L	L	X	X	X	Asynchronous Reset; Q0 - Q7 = Low
L	H	H	H	↑	Parallel load; I/On → Qn (I/On outputs disabled)
L	H	L	H	↑	Shift right; DS0 → Q0, Q0 → Q1, etc.
L	H	H	L	↑	Shift left; DS7 → Q7, Q7 → Q6, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs in High Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 ↑ = Low-to-High clock transition

# 8-bit universal shift/storage register (3-State)

74F299

## LOGIC DIAGRAM



## 8-bit universal shift/storage register (3-State)

74F299

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT	
$V_{CC}$	Supply voltage	-0.5 to +7.0	V	
$V_{IN}$	Input voltage	-0.5 to +7.0	V	
$I_{IN}$	Input current	-30 to +5	mA	
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to + $V_{CC}$	V	
$I_{OUT}$	Current applied to output in Low output state	Q0, Q7	40	mA
		I/On	48	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C	
$T_{stg}$	Storage temperature	-65 to +150	°C	

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current	Q0, Q7		-1	mA
		I/On		-3	mA
$I_{OL}$	Low-level output current	Q0, Q7		20	mA
		I/On		24	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

## 8-bit universal shift/storage register (3-State)

74F299

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>NO TAG</sup>			LIMITS			UNIT
						MIN	TYP NO TAG	MAX	
V <sub>OH</sub>	High-level output voltage	Q0, Q7	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -1mA	±10%V <sub>CC</sub>	2.5			V
					±5%V <sub>CC</sub>	2.7	3.4		V
		I/On		I <sub>OH</sub> = -3mA	±10%V <sub>CC</sub>	2.4			V
					±5%V <sub>CC</sub>	2.7	3.3		V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.35	0.50	V
					±5%V <sub>CC</sub>		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage	others	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V					100	μA
		I/On	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 5.5V					1	mA
I <sub>IH</sub>	High-level input current	except I/On	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA
I <sub>IL</sub>	Low-level input current	S0, S1	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-1.2	mA
		others						-0.6	mA
I <sub>IH</sub> + I <sub>OZH</sub>	Off-state output current, High-level voltage applied	I/On only	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					70	μA
I <sub>IL</sub> + I <sub>OZL</sub>	Off-state output current Low-level voltage applied		V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V					-0.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>		V <sub>CC</sub> = MAX			-60		-150	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				55	60	mA
		I <sub>CCL</sub>					70	90	mA
		I <sub>CCZ</sub>					65	95	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## 8-bit universal shift/storage register (3-State)

74F299

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Qn		85	115		85		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q0 or Q7		Waveform 1	4.0 4.5	5.0 6.0	7.5 8.0	3.5 4.5	8.5 8.5	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to I/On		Waveform 1	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns ns
t <sub>PHL</sub>	Propagation delay MR to Q0 or Q7		Waveform 2	5.5	7.5	9.5	5.5	10.5	ns
t <sub>PHL</sub>	Propagation delay MR to I/On		Waveform 2	5.5	7.5	10.0	5.5	10.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time Sn, OE to I/On		Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	9.0 11.0	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time Sn, OE to I/On		Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	8.0 6.5	ns ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low S0 or S1 to CP		Waveform 3	6.5 6.5			7.5 7.5		ns ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low S0 or S1 to CP		Waveform 3	0 0			0 0		ns ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Set-up time, High or Low I/On, DS <sub>L</sub> or DS <sub>R</sub> to CP		Waveform 3	3.5 3.5			4.0 4.0		ns ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low I/On, DS <sub>L</sub> or DS <sub>R</sub> to CP		Waveform 3	0 0			0 0		ns ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse width, High or Low		Waveform 1	5.0 4.5			5.0 4.5		ns
t <sub>w</sub> (L)	$\overline{\text{MR}}$ Pulse width, Low		Waveform 2	4.5			4.5		ns
t <sub>rec</sub>	Recovery time, $\overline{\text{MR}}$ to CP		Waveform 2	4.0			4.0		ns

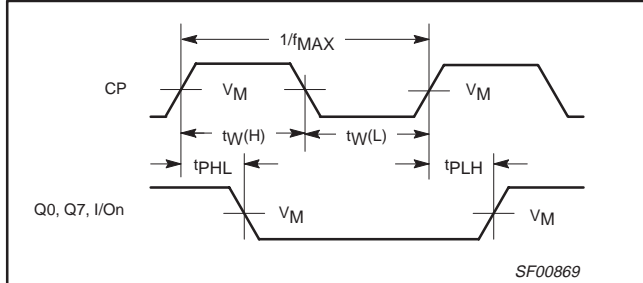
# 8-bit universal shift/storage register (3-State)

74F299

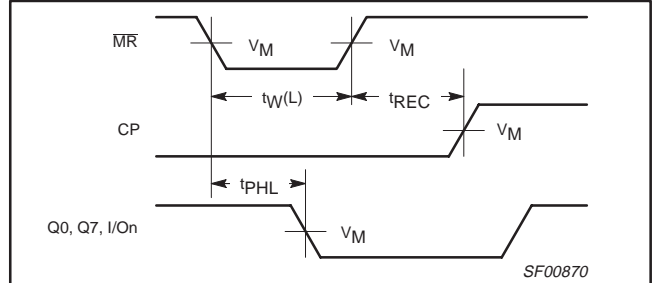
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$

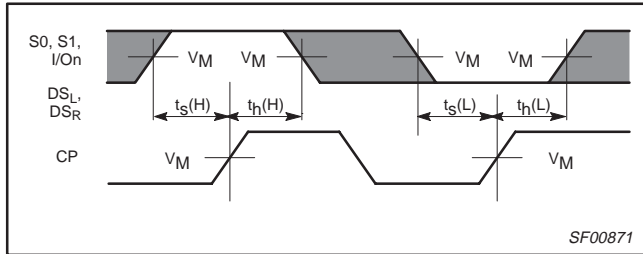
The shaded areas indicate when the input is permitted to change for predictable output performance.



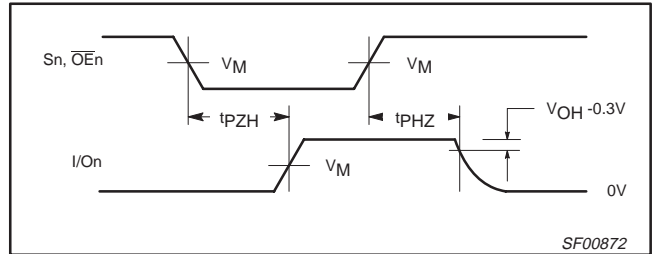
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Width, and Maximum Clock Frequency**



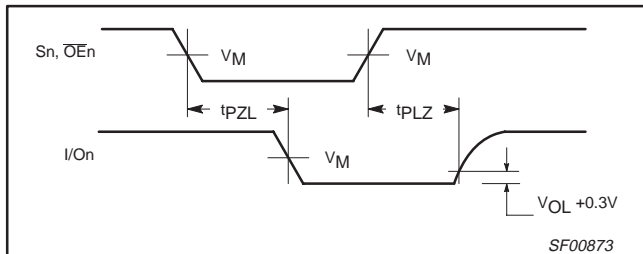
**Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time**



**Waveform 3. Setup and Hold Times**



**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**



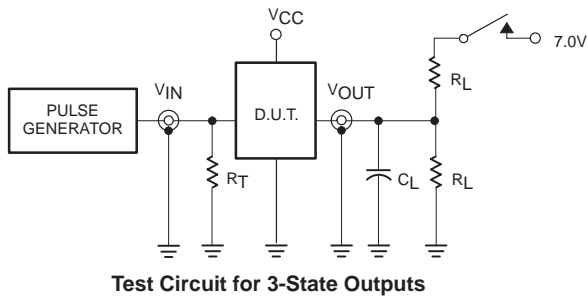
**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**



# 8-bit universal shift/storage register (3-State)

74F299

## TEST CIRCUIT AND WAVEFORM



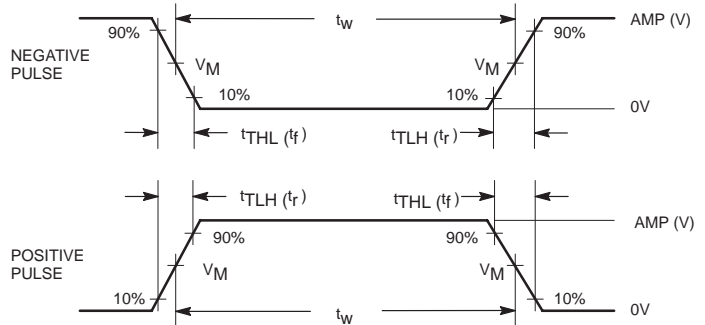
Test Circuit for 3-State Outputs

### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

### DEFINITIONS:

$R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

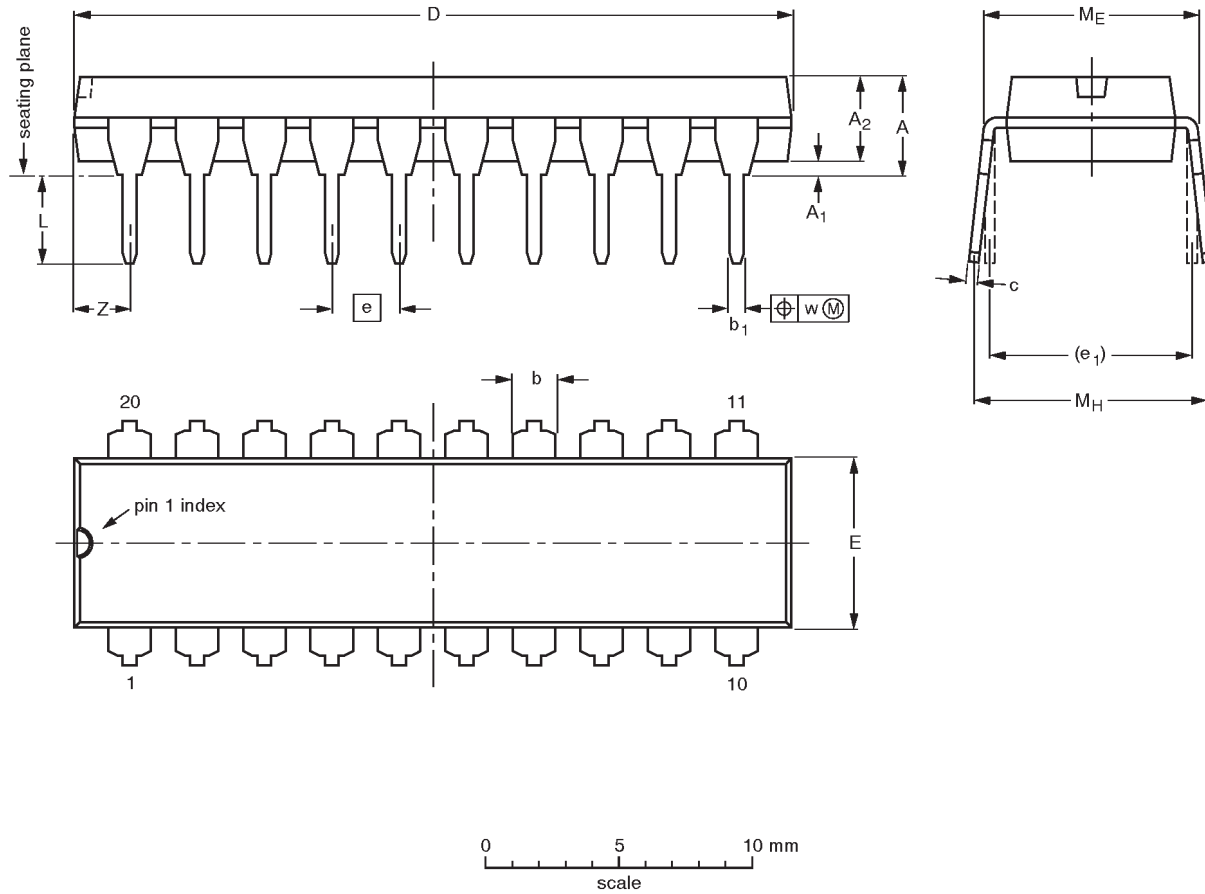
SF00777

# 8-bit universal shift/storage register (3-State)

74F299

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

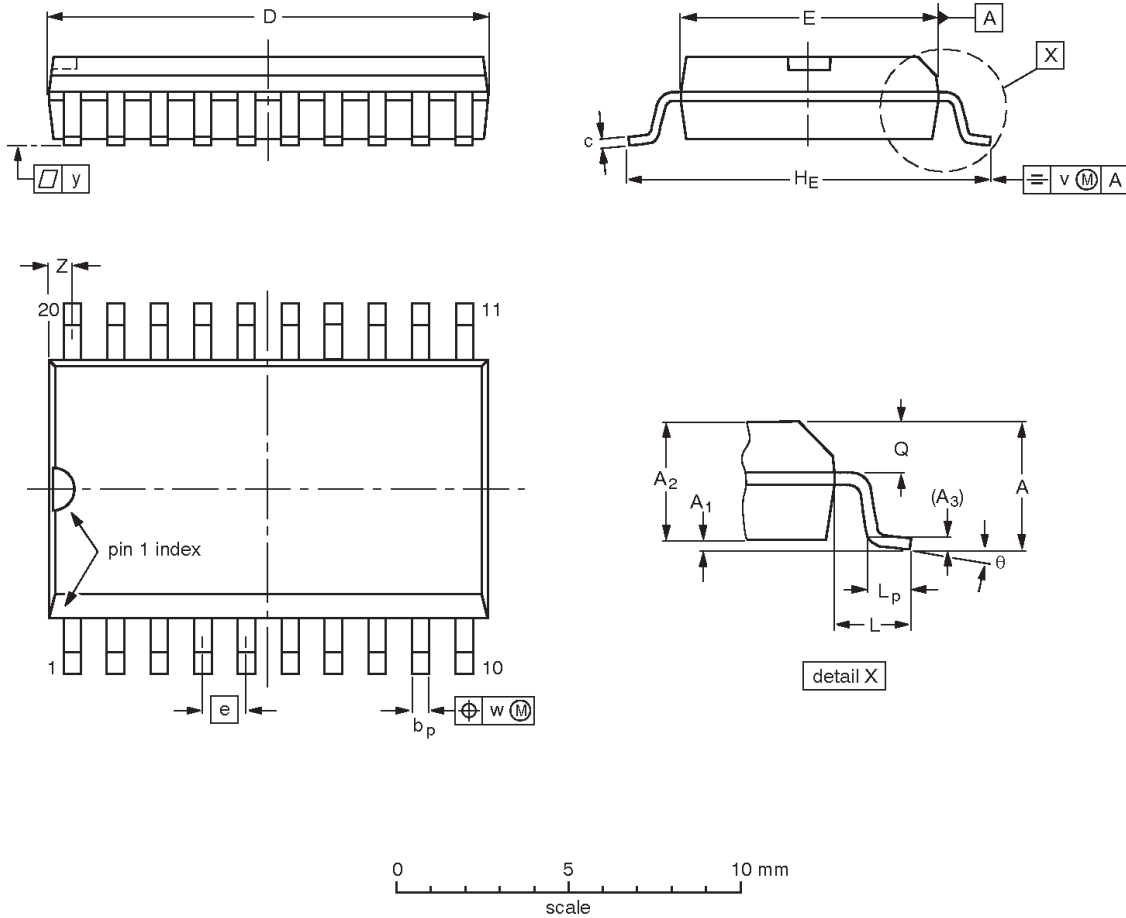
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# 8-bit universal shift/storage register (3-State)

## 74F299

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

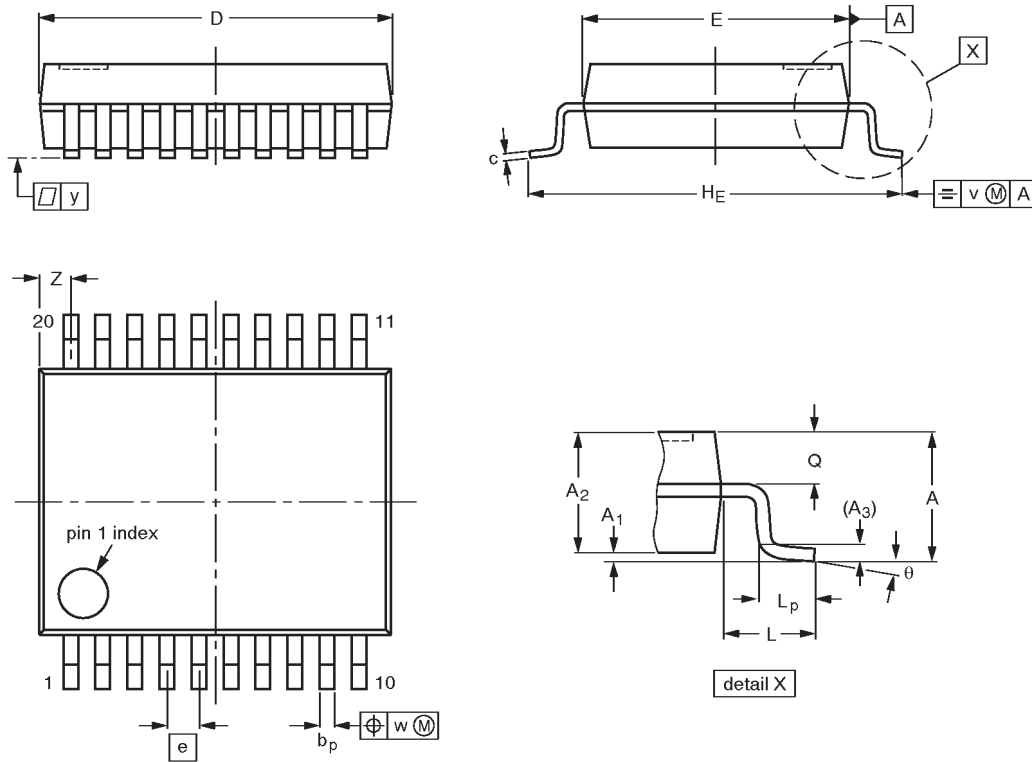
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

# 8-bit universal shift/storage register (3-State)

74F299

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm**

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

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8-bit universal shift/storage register (3-State)

74F299

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**NOTES**

## 8-bit universal shift/storage register (3-State)

74F299

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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