MX•COM, INC. MiXed Signal ICs

DATABULLETIN

MX812

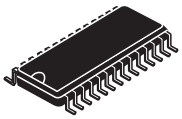
VSR CODEC WITH DRAM CONTROL

C-BUS COMPATIBLE

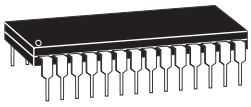
PRELIMINARY INFORMATION

Features and Applications

- **Half-Duplex Voice Storage and Retrieval**
- **Serial Bus µProcessor Control**
- **On-Chip DRAM Controller**
- **Up To 2 Minutes of High-Quality Recorded Audio**
- **Answering Functions and Voice-Notepad**
- **Low-Power 5-Volt CMOS**
- **Selectable Sample Rates and "Memory Size"**



MX812DW
28-pin SOIC



MX812J
28-pin CDIP

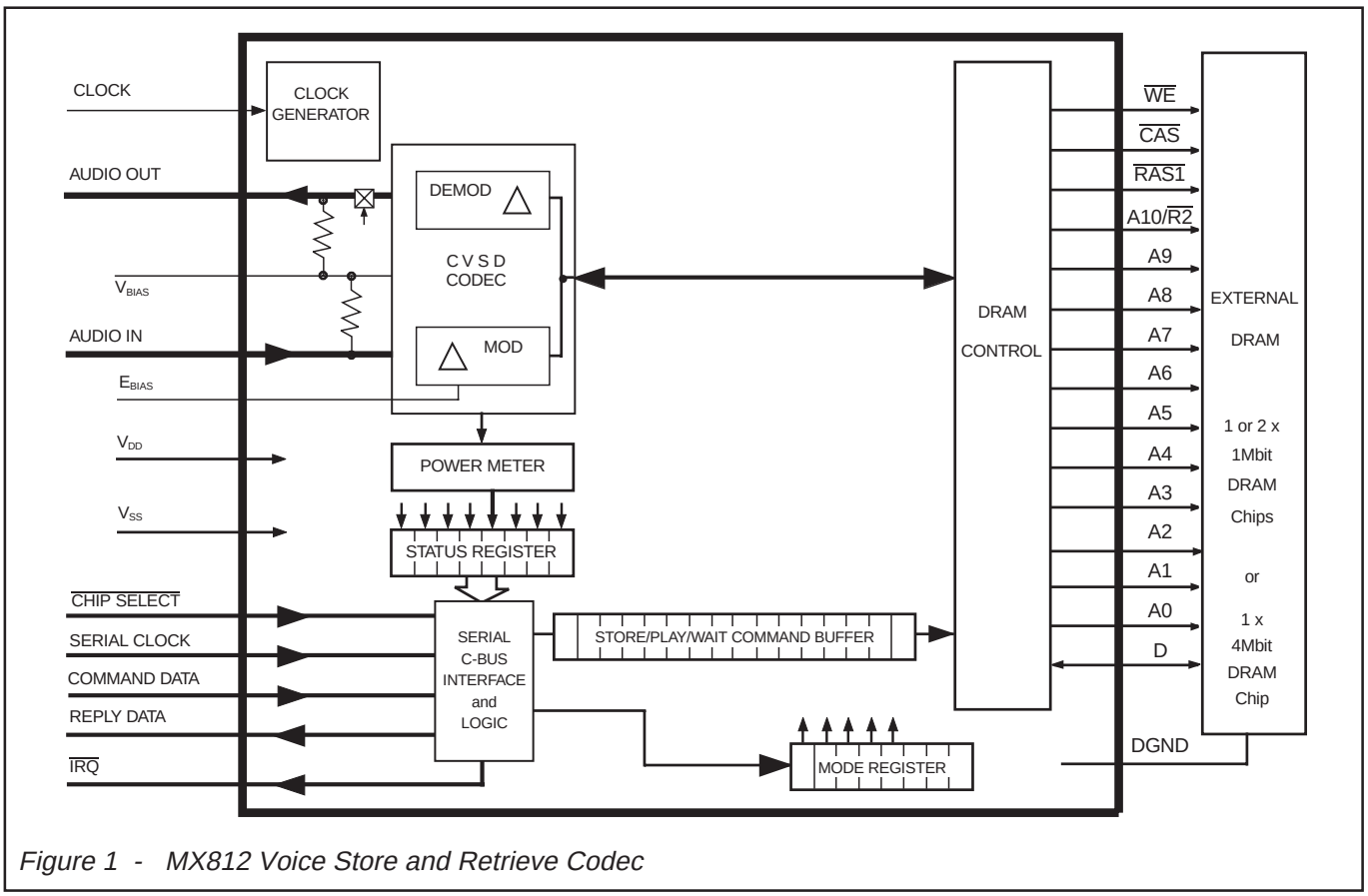


Figure 1 - MX812 Voice Store and Retrieve Codec

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Doc. # 20480076.003

DESCRIPTION

The MX812 is a half-duplex VSR Codec, which when connected to an audio processing microcircuit (such as the MX816, 826 or 836), provides the storage and recovery of speechband audio in attached Dynamic RAM. The addition of this device will enhance the communications system by providing cellular radios with Answering Functions, “Message-Notepad” and general announcement cabapilities.

The MX812 will enable:

- Storage of a speech message for transmission (replay) at a later time.
- Storage of a received speech message when the operator is not attending.
- The storage and subsequent replay of speech.

All VSR operating functions are controlled by a simple serial µProcessor interface which may operate from the radio’s own µProcessor/Controller.

Input audio from the “Store” output of the audio processor is digitized by delta modulation and stored via the DRAM controller, in attached memory.

Audio for replay is recovered from the assigned memory locations and after demodulation made available for supply to the “Play” input of the audio processor. For use with other audio systems, the input/output audio can be connected to relevant points in circuit.

The MX812 has no on-chip input or output audio filtering; this capability must therefore be provided by the host system. Sampling rates and memory capacity are selectable to 32kb/s or 63kb/s and 1 x 4Mbit or 2 x 1Mbit respectively, which when used in conjunction allow control of audio-quality and storage-time.

This low-power CMOS device is available 28-pin plastic SOIC and 28-pin Cerdip packages.

Pin	Function
1	**$\overline{\text{CAS}}$:** This output should be connected to the “Column Address Strobe” input pin(s) of all DRAM devices installed.
2	**$\overline{\text{WE}}$:** This output should be connected to the “Write Enable” input pin(s) of all DRAM devices installed.
3	**D:** Digital (speech) data into and out of the VSR Codec. This pin should be connected to the “Data In” and “Data Out” pins (“D” and “Q”) of DRAM devices.
4	**Xtal:** The nominal 4.0MHz clock input to the VSR Codec. The signal applied to this device may be derived from the attached Audio Processor on-chip Xtal Oscillator circuits (see Figures 2 and 3). **Note** that the VSR Codec will be able to function and maintain correct DRAM refresh, with Xtal input frequencies down to 2.0MHz. Compand and Local Decoder time constants will change accordingly and minimum “C-BUS” timings (Figures 6 and 7) would have to be increased pro-rata.
5	**Interrupt Request ($\overline{\text{IRQ}}$):** This Interrupt Request output from the MX812 is ‘wire-OR able’ allowing the Interrupt Outputs of other peripherals to be commoned and connected to the Interrupt input of the µProcessor (see the C-BUS Interface and System Applications document). This input has a low-impedance pulldown to V_{SS} when active, and a high-impedance when inactive.
6	**Serial Clock:** The C-BUS serial clock input. This clock produced by the µController, is used for transfer timing of commands and data to and from the VSR Codec. See Timing Diagrams.
7	**Command Data:** The C-BUS serial (command) data input from the µController. Data is loaded to this device in 8-bit bytes MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock.
8	**Chip Select ($\overline{\text{CS}}$):** The C-BUS data transfer control function. This input is provided by the µController. Transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
9	**Reply Data:** The C-BUS serial data output to the µController. The transmission of reply bytes is synchronized to the Serial Clock under the control of the Chip Select input. This is a 3-state output which is held at a high-impedance when not sending data to the µController.
10	**V_{BIAS}:** The output of the internal analog circuitry bias line, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_2 (see Figure 2).

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Pin	Function
11	**Audio Out:** The analog output to the Audio Processor "Play" input when the VSR Codec is configured as a Decoder. When configured as an active Decoder but with no Play Page commands (62_H) active, the VSR Codec will play-out an idle pattern of "101010.....10^s". When not configured as a Decoder, or Powersaved (Mode Register), this output will be held at V_{BIAS} via an internal 500kΩ resistor. The output at this pin is unfiltered; an external speechband filter – such as that included on the MX816/826/836 Audio Processors – will be required. Since this output is centered around $V_{DD}/2$ a coupling capacitor is required.
12	**E_{BIAS}:** The Encoder d.c. internal balancing circuitry line. This pin should be decoupled to V_{SS} by capacitor C_4 (see Figure 2). **Note** that in the 'Encode' mode (Mode Register DE and PS both "0") the Codec drives this pin to approximately $V_{DD}/2$ through a very high impedance; it can take more than one second for the E_{BIAS} voltage to stabilize when power is first applied to this device. A faster start-up can be achieved by setting Bit DE or PS to "1" for 250mS (approx) during power-up. This will cause the E_{BIAS} pin to be connected to V_{BIAS} through a resistance of approximately 100kΩ.
13	**Audio In:** The analog input to the VSR Codec in the Encode mode. When not configured as an Encoder, or Powersaved (Mode Register), this input will be held at V_{BIAS} via an internal 500kΩ resistor. This pin should be coupled via a capacitor, see Figure 2. As this input does not contain an internal audio filter, the audio to this pin should be limited to a 3400Hz "speechband" by an external audio filter – such as included in the MX816/826/836 Audio Processors.
14	**V_{SS}:** The "analog" ground connection. See D_{GND} description.
15	**A0:**
16	**A1:**
17	**A2:**
18	**A3:**
19	**A4:** — DRAM address line outputs from the MX812. These pins should be connected to the corresponding address inputs of the associated DRAM.
20	**A5:**
21	**A6:**
22	**A7:**
23	**A8:**
24	**A9:**
25	**A10/$\overline{R2}$:** A dual function output pin selected by the memory size (MS) bit (Mode Register), as detailed in the table below:

MS bit	DRAMs	Connected To	This Output
"0"	1Mbits'	DRAM No 2 $\overline{RAS}$	RAS2
"1"	4Mbit	DRAM A10	A10 Signal

26	**$\overline{RAS}$:** An output from the VSR Codec which should be connected to the "Row Address Strobe" pin of the 4Mbit DRAM or the first 1Mbit DRAM, see Figure 4, Example DRAM connections.
27	**D_{GND}:** The digital signal ground connection to the VSR Codec. Both D_{GND} and V_{SS} pins should be connected to the negative side of the d.c. power supply. However, a printed circuit board should be laid out so that D_{GND} is connected as closely as possible to the DRAM section ground pins.
28	**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the VSR Codec are dependent upon this supply. This pin should be decoupled to V_{SS} via capacitor C_5, located close to the MX812 pins.

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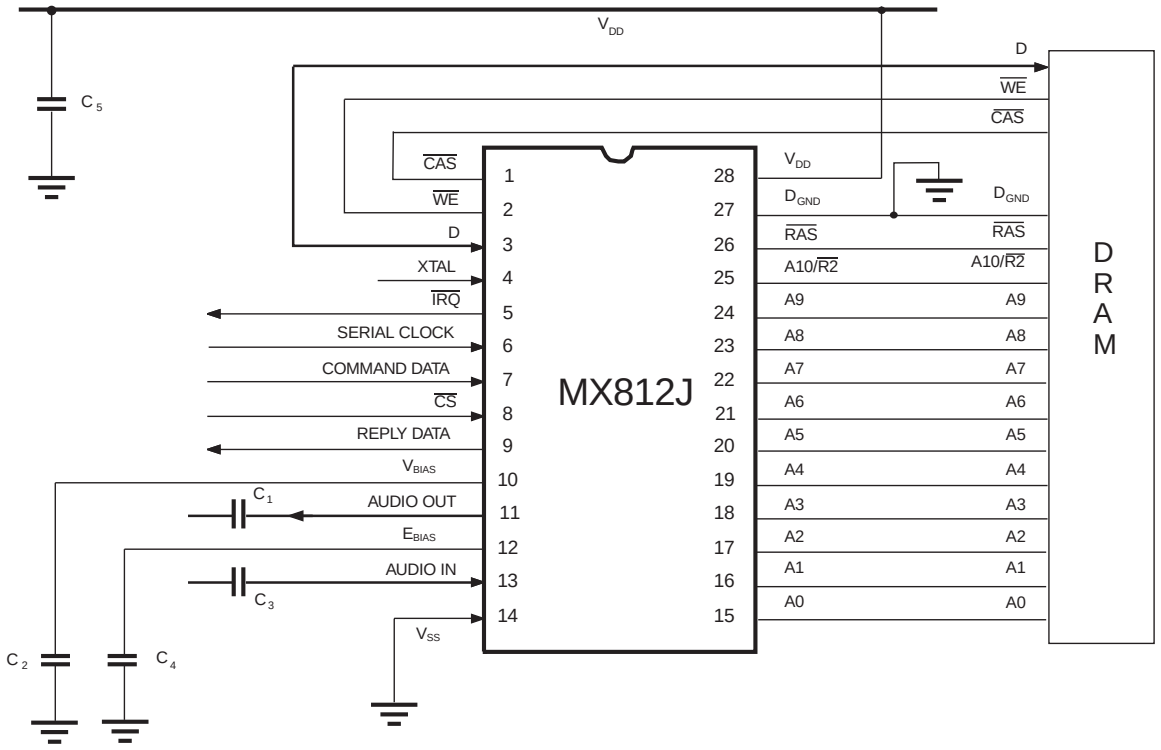
Application Information



Component	Value
C_1	Dependent upon the input impedance of the driven stage
C_2	1.0µF
C_3	0.1µF
C_4	1.0µF non-electrolytic
	Tolerance: Capacitors = -50/+100%

Figure 2 - Recommended External Components

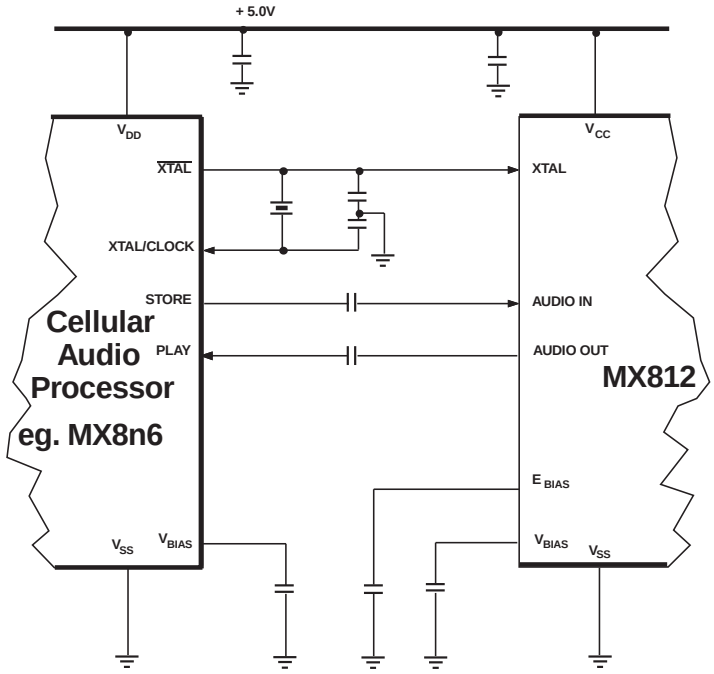


Figure 3 - Interfacing to an Audio Processor

Application Information .....

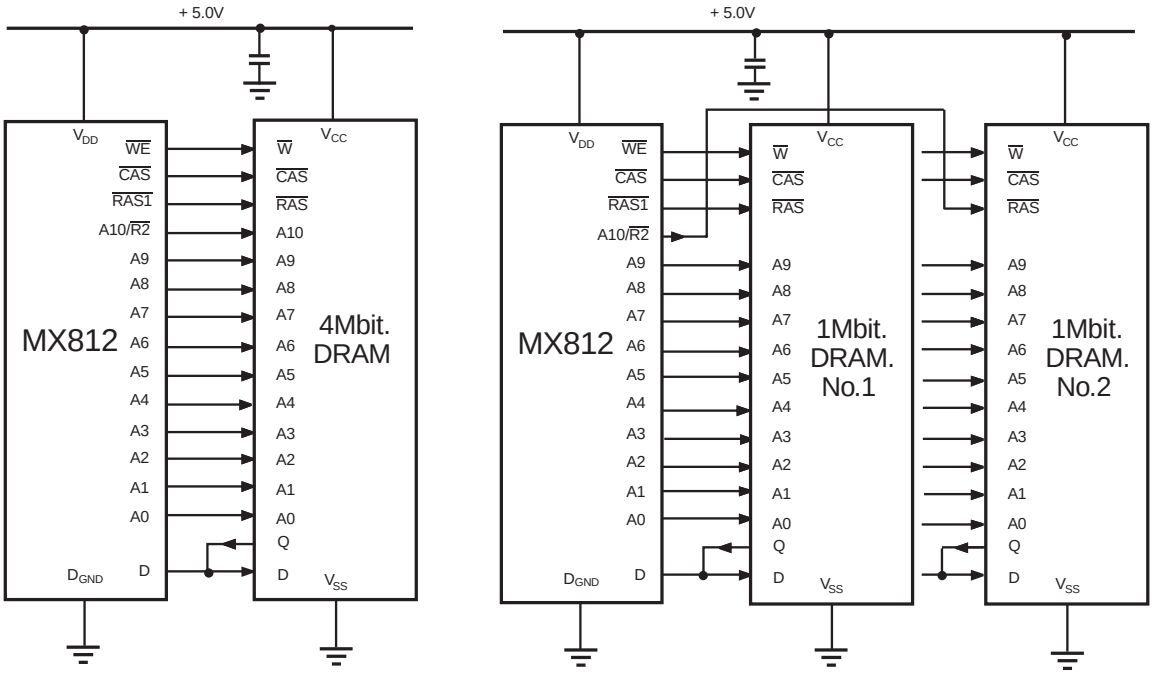


Figure 4 - Example DRAM Connections

Choice of DRAM Devices

DRAM devices chosen should be standard 1,048,576 x 1 or 4,194,304 x 1 Dynamic Random Access memories, with 'CAS before RAS' refresh, and a Row Address access time of 200 nano-seconds or less.

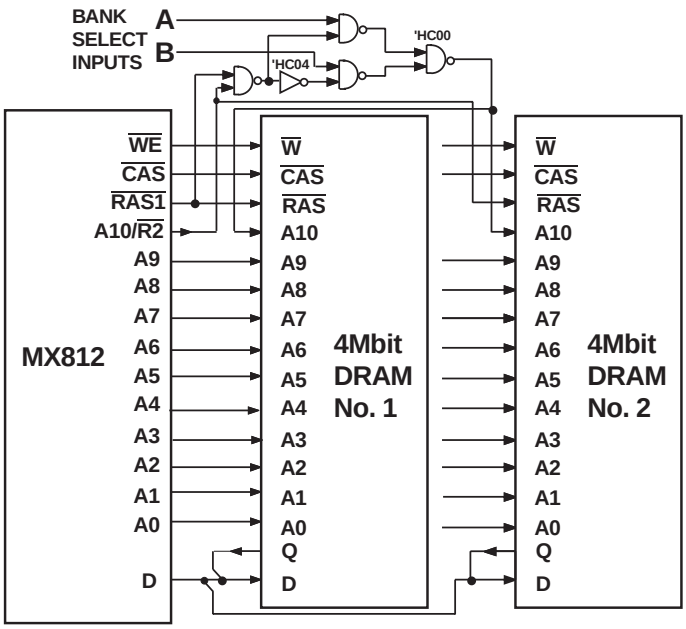


Figure 5 - Use of External Elements to Drive Two 4-MBit DRAM Chips

Driving Two 4-MBit DRAM Sections

By adding external logic circuitry, the MX812 can be configured to drive two 4-MBit DRAM sections. This will have the effect of doubling the available storage time. i.e. 4 minutes at 32kbps.

With reference to the circuitry shown in Figure 5: With the Mode Register **MS** Bit set to "0" the MX812 treats the DRAM sections as two 1-Mbit devices. The external logic makes each 4-MBit DRAM appear as four 1-MBit banks selected by the Bank Select lines '**A**' and '**B**.'

Bank Select Inputs A	B	DRAM No 1 Pages 0 – 1023	DRAM No 2 Pages 1024 – 2047
0	0	■	■
1	0	■	■
0	1	■	■
1	1	■	■

The Controlling System: C-BUS Hardware Interface

C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and MX-COM's New Generation integrated circuits. C-BUS is designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer can choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the MX812 VSR Codec is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the MX812. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	+	Data Byte/s
General Reset	01	0 0 0 0 0 0 0 1		
Write to Mode Register	60	0 1 1 0 0 0 0 0	+	1 byte Instruction to Mode Register
Read Status Register	61	0 1 1 0 0 0 0 1	+	1 byte Reply from Status Register
Store/Play Page	62	0 1 1 0 0 0 1 0	+	2 bytes Command
Wait	63	0 1 1 0 0 0 1 1		

Table 1 – C-BUS Address/Commands

"Write to Mode Register"

– A/C 60_H, followed by 1 byte of Command Data.

Interrupt Output – IE

Controls the MX812 IRQ output driver.

Sampling Rates – SR

The CVSD Codec sampling rates. Accurate rates depend upon the applied Xtal/clock frequency (see Table 5).

Memory Size – MS

The MX812 can operate with 1 x 1Mbit, 2 x 1Mbit or 1 x 4Mbit of DRAM (see Figure 4).

Powersave – PS

Powersaves the CVSD Codec only. Logic functions and DRAM refresh are maintained.

Decode/Encode – DE

The Codec and DRAM operational mode."
"Play" or "Store"

Setting	*Mode Bits*
MSB	***Transmitted to 812 First***
7	**Interrupt Output**
1	Enable
0	Disable
6	**Sampling Rate**
1	63kb/s
0	32kb/s
5	**Memory (DRAM) Size**
1	Single 4Mbit
0	1 or 2 x 1Mbit
4	**Powersave**
1	CVSD Codec Powersaved
0	CVSD Codec Powered
3	**Decode/Encode**
1	Decode – Play Mode
0	Encode – Store Mode
2 ***1*** ***0***	**Not Used**
0 0 0	Set to 'zeros'

Table 2 - Control Register

Interrupts

The MX812's Interrupt Output is driven by the Status Bit 7 (IF) when the Mode Register Bit7 (IE) is set to a "1."

The IF bit and the Interrupt Output (If enabled) are set when the Store/Play/Wait command Buffer is emptied (MT bit) by transferring from the buffer to the DRAM control circuits.

and/or

The IF bit and the Interrupt Output (if enabled) are set when a Store, Play or Wait command has finished **and** the Command Buffer is empty.

The notes below illustrate the $\overline{IRQ}$ pin conditions:

IF Bit	IE Bit	$\overline{IRQ}$
"0" cleared	"0" disable	High Z
"0" cleared	"1" enable	High Z
"1" Interrupt	"0" disable	High Z
"1" Interrupt	"1" enable	V_{SS} (logic "0")

"General Reset" – A/C 01_H

Upon Power-Up the "bits" in the MX812 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the C-BUS, and has the following effect upon the MX812.

Clear all Mode Register bits to "0"

Status Register Bit 7 (IF) to "0"

Bits 5 and 6 (MT and I) to "1"

Halt any current Store, Play or Wait execution

Clear the Store/Play/Wait Command Buffer

The Controlling System .....

"Read Status Register" – A/C 61_H, followed by 1 byte of Reply Data.

Reading	*Status Bits*
MSB	***Received from 812 First***
7	**Interrupt Condition (Flag)**
1	Bit 6 or 5 set to a "1"
0	Cleared condition
6	**Command Buffer**
1	Buffer Empty
0	Cleared condition
5	**Device Condition**
1	Idle
0	Storing, Playing or Waiting
4 3 2 1 0	**Input Power Level**

Table 3 Status Register

Interrupt Condition (Flag) – IF

Set to a logic "1" whenever Bit 6 or Bit 5 goes from "0" to "1" (unless the transition is caused by a General Reset command 01_H). This indication allows monitoring by 'poll' while Interrupts are disabled.

Cleared to a logic "0" by a General Reset command or immediately following a read of the Status Register.

Command Buffer Status – MT

Set to a logic "1" when the Command Buffer is empty or by a General Reset command.

Cleared to a logic "0" by loading a new Store, Play, Wait commands.

Device Condition – I

Set to a logic "1" when **NO** Store, Play or Wait command is being executed or by a General Reset command.

Set to a logic "0" while a Store, Play or Wait command is being executed.

Encode Input Power Level – POWER

Available in the Encode mode, a 5-bit representation of the analog signal input level, updated at the end of every Store or Wait command.

Store/Play/Wait Command Buffer

A buffer used to accept and hold the latest Store, Play or Wait command received over the C-BUS while the MX812 is executing the previous command. The Status Register, bit 6, indicates the condition of this buffer.

When a command is received it is first loaded into this buffer. If the MX812 is already executing a previously loaded Store, Play or Wait command the new command will be stored temporarily in the Command Buffer, from where it will be taken on completion of the previous command.

This permits the MX812 to perform a continuous sequence of Store, Play or Wait commands, without gaps and without requiring an unduly fast response from the mController.

Note that this Command Buffer can only hold one Store, Play or Wait instruction, each new command received into this buffer will overwrite any previously loaded contents.

To Store or Play a sequence of pages the relevant commands should be loaded with sequential page numbers while observing the Status Register – Bit 6.

"Store/Play Page" – A/C 62_H, followed by 2 bytes of Command Data.

For the purposes of storage and replay, the attatched DRAM is divided into 'data-pages' of 1024 bits (1kbit).

One Store/Play command (loaded MSB first) will instruct the MX812 to store or play (depending upon the setting of the Mode Register, Bit-3) to or from 1 x 1024 "page" of DRAM. The Store/Play/Wait command buffer will allow continuity of operation.

The particular page selected is identified by the 12 lowest bits of the 2 x Store/Play bytes as shown below.

If a Store command is loaded and executed whilst the Codec is "Powersaved" in the Encode mode, the selected DRAM page will be filled with an idle pattern ("101010.....").

	Bit Number																
	MSB – Loaded to MX812 First														***Loaded Last – LSB***		
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bit**
Value	**x**	**x**	**x**	**x**	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	**Value**
Page	"0"	"0"	"0"	"0"	——— DRAM Page Number ———												**Page**

DRAM Size	Valid Page Nos	Bit Nos
4Mbit	0 – 4095	0 – 11
1 + 1Mbit	0 – 2047	0 – 10
1Mbit	0 – 1023	0 – 9

"Wait" – A/C 63_H, — Wait for 1024 bit periods

Causes the MX812 to wait for 1024 bit periods (approximately 16 or 32ms).

If the Codec is set to the Encode mode, a new "Power" reading that is relevant to the input audio level, will be loaded into the Status Register at the end of the Wait period.

If the Codec is set to the Decode mode it will 'Play' a perfect idle pattern ("101010.....") during the Wait period.

Control Timing Information

Figure 6 shows the timing parameters for two-way communication between the µController and Cellular peripherals on the "C-BUS." Figure 7 shows the timing relationships between the Serial Clock and Data.

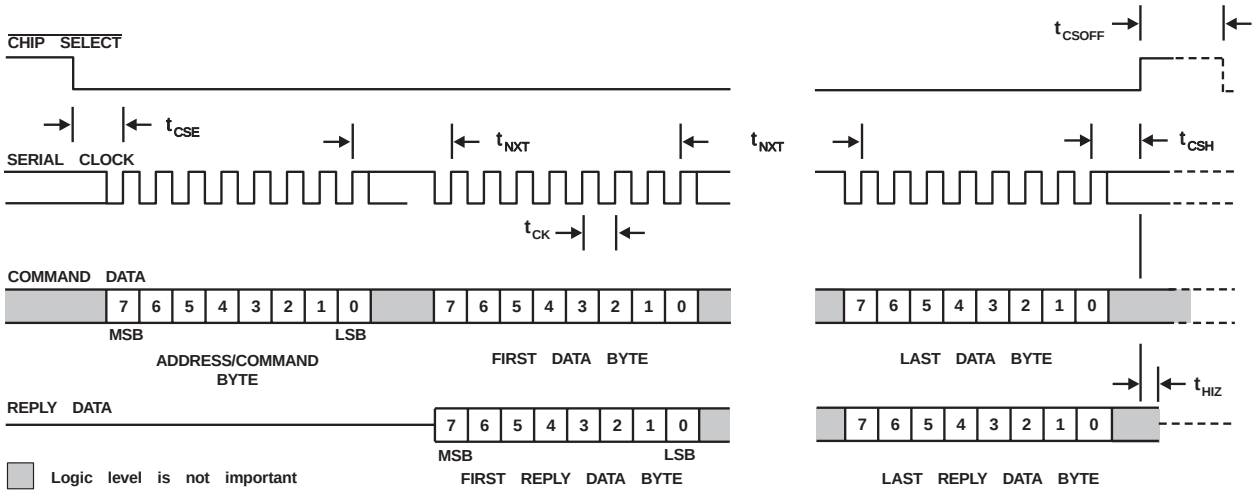


Figure 6 - Control Timing Information

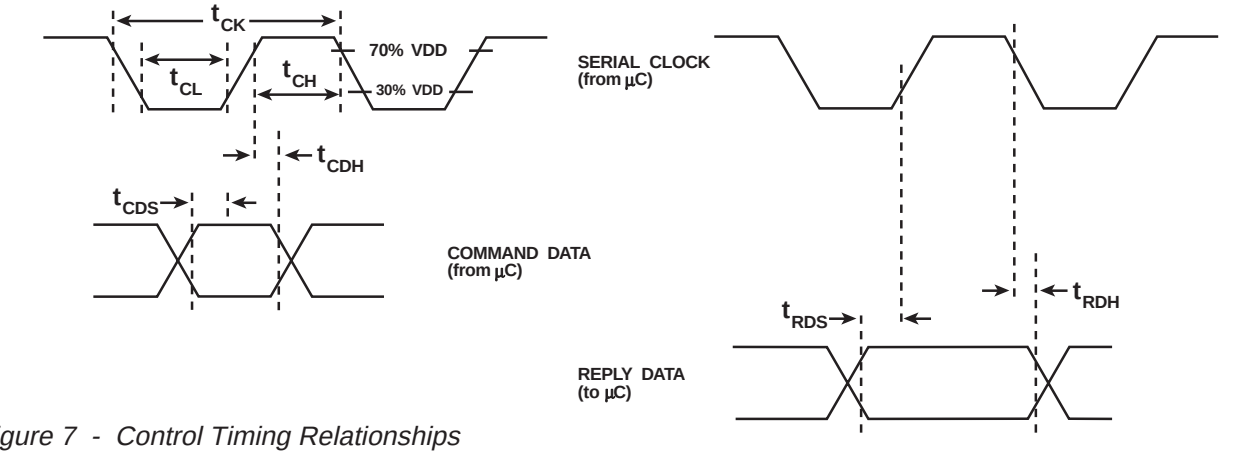


Figure 7 - Control Timing Relationships

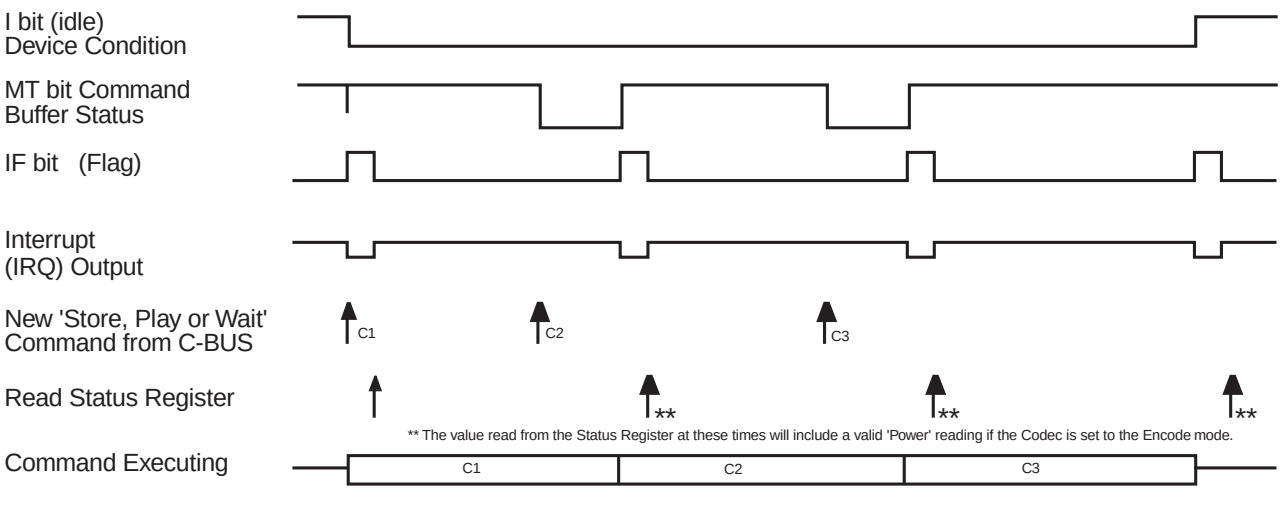


Figure 8 - Typical Command Sequences

Control Timing Information .....

Timing Specification – Figures 6 and 7

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"		2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"		4.0	–	–	µs
t_{HIZ}	"CS-High to Reply Output Tri-state"		–	–	2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time		2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time		4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns
t_{RDS}	"Reply Data Set-Up" Time		250	–	–	ns
t_{RDH}	"Repy Data Hold" Time		50.0	–	–	ns

Address Line Decoding

MA0 to MA21 are the outputs of the internal 22-bit DRAM address counter, which are time multiplexed as 'Row' and 'Column' addresses onto the DRAM address lines A0 to A10 etc., as shown below.

Memory Size (MS) Bit = "1" – 4Mbit DRAM

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10/R2
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18	MA20
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19	MA21

Memory Size (MS) Bit = "0" – 1Mbit DRAM(s)

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19

MA20	MA21	RAS1	A10/R2	DRAM Selected
0	x	active		"first"
1	x		active	"second"

x = don't care

Table 4 Address Line Decoding

Sample Rate (SR) Bit	Division Ratio	Xtal/clock Frequency (MHz) 4.0	4.032	4.096
SR = "1"	64 kbps	62.5 kbps	63 kbps	64 kbps
SR = "0"	128 kbps	31.25 kbps	31.5 kbps	32 kbps
		Internal Clock Rate		
Local Decoder Clock		125 kHz	126 kHz	128 kHz

Table 5 Sampling Clock Rates Available

Performance

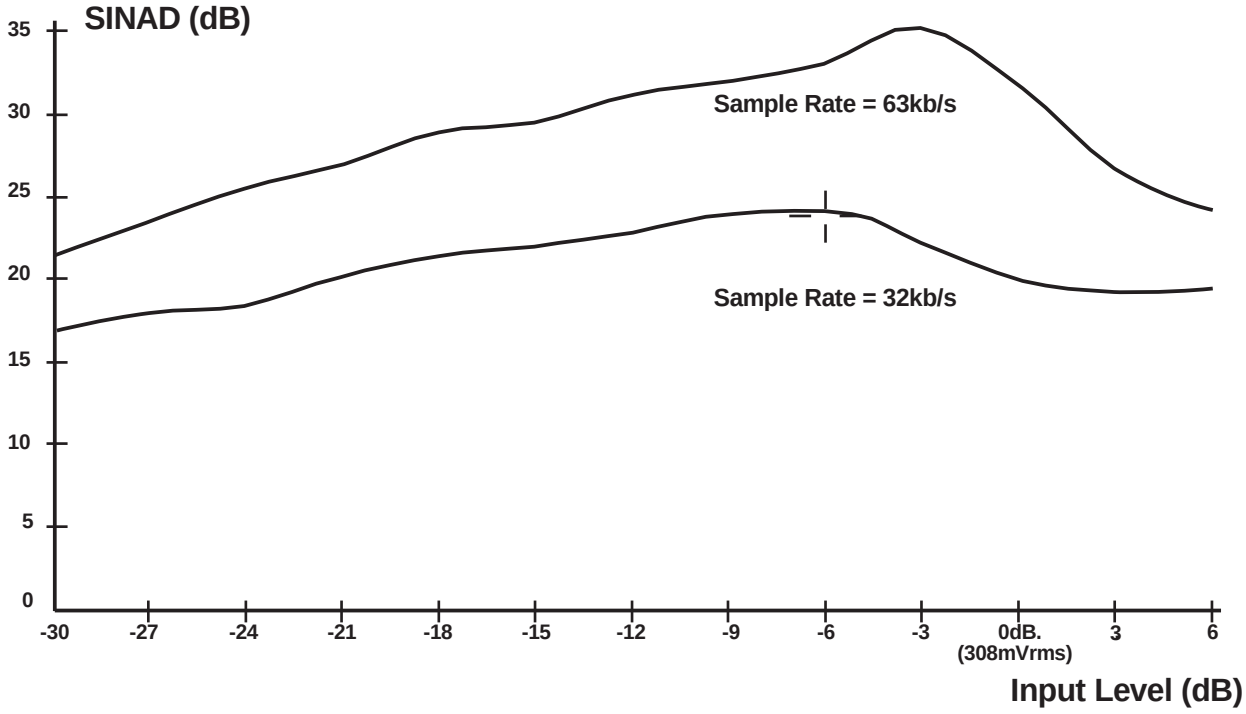


Figure 9 - Typical "SINAD vs Input Level" Plot

Performance

Figure 9 Shows a typical graph of SINAD vs Input Level produced for both 32kbps and 63kbps sample rates at an input frequency of 1.0kHz.

Figure 10 shows a typical graph of the "Power" reading for increasing input signal levels. The "Power" figure (0 to 31) is the binary figure obtained from the 5-bit representation in the Status Register - Bits 0, 1, 2, 3 and 4 while the Codec is selected to the Encode mode.

This reading is updated at the end of every Store or Wait command; Excessive input signal levels will record "11111_2" (31_{10}).

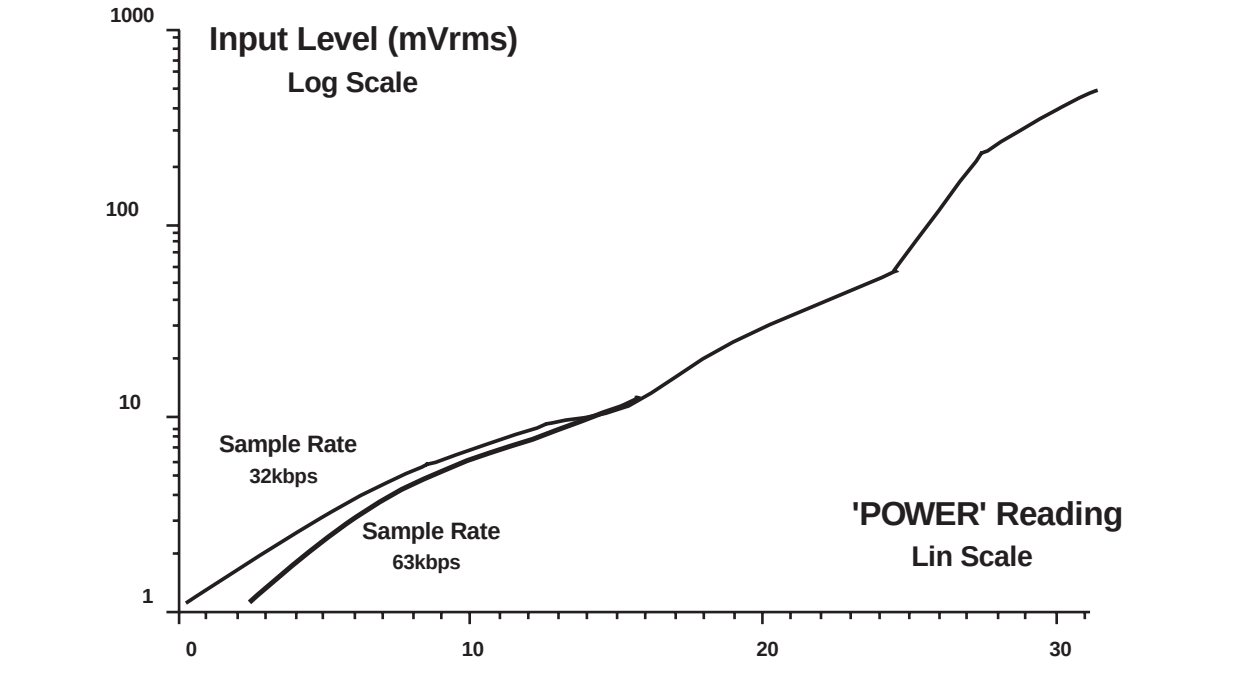


Figure 10 - Typical "Power Reading vs Input Level" Plot

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD}+0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.00MHz

Audio Level 0dB ref = 308mVrms @ 1kHz

Reply Data Line loaded with 50pF/200kΩ to V_{SS}

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Enabled	1	–	3.0	–	mA
Powersaved	1	–	1.0	–	mA
Analog Input Impedance		–	100	–	kΩ
Analog Output Impedance (Decode)		–	1.0	–	kΩ
Analog Output Impedance (Encode or Powersave)		–	500	–	kΩ
DRAM Interface					
Input Logic “1”	2	3.5	–	–	V
Input Logic “0”	2	–	–	1.5	V
Output Logic “1” (at I_o = -120µA)	3	2.7	–	–	V
Output Logic “0” (at I_o = 120µA)	3	–	–	0.4	V
Input Leakage Current (at V_{IN} = 0 to V_{DD})	4	-1.0	–	1.0	µA
Input Capacitance	2	–	10.0	–	pF
Digital Interface					
Input Logic “1”	5	3.5	–	–	V
Input Logic “0”	5	–	–	1.5	V
I_{IN} (logic “1” or “0”)	5	-1.0	–	1.0	µA
Output Logic Levels					
Output Logic “1” (-120µA)	6	4.6	–	–	V
Output Logic “0” (360µA)	7	–	–	0.4	V
I_{Out} Tri-state (logic “1” or “0”)	6	-4.0	–	4.0	µA
Input Capacitance	5	–	–	7.5	pF
IOX (V_{Out} = 5V)	8	–	–	4.0	µA

Characteristics	See Note	Min.	Typ.	Max.	Unit
Dynamic Values					
"Xtal" Pin Input Frequency Range	12	4.0		4.1	MHz
Store Mode					
Analog Input Signal Levels	9	-24.0	–	4.0	dB
Analog Input Signal Frequency Range	9, 10	300		3400	Hz
Recommended Signal Source Impedance	9	–	–	2.0	kΩ
Play Mode					
Analog Output Signal Levels	13	-7.0	–	-5.0	dB
Output Noise (idle)	11	–	-55.0	–	dBp
Overall 'Store to Play' Performance					
Output Noise (Input Short Circuit)	11	–	-50.0	–	dBp
SINAD (**SR** = 32kb/s)					
(Input = 1.0kHz @ -6.0dB)	11	–	23.0	–	dB

Notes

1. Not including DRAM current.
2. D input from DRAM
3. Outputs to DRAM.
4. All digital inputs.
5. Serial Clock, Command Data and Chip Select inputs.
6. Reply Data output.
7. Reply Data and Interrupt ($\overline{IRQ}$) outputs.
8. Leakage current into the "Off" Interrupt ($\overline{IRQ}$) output.
9. For optimum performance.
10. Input filtering must be performed at the source.
11. Measured in conjunction with the FX836 R2000 system Audio Processor.
12. For full C-BUS compatibility.
13. Playback of a stored "-6.0dB 1.0kHz Test Signal."

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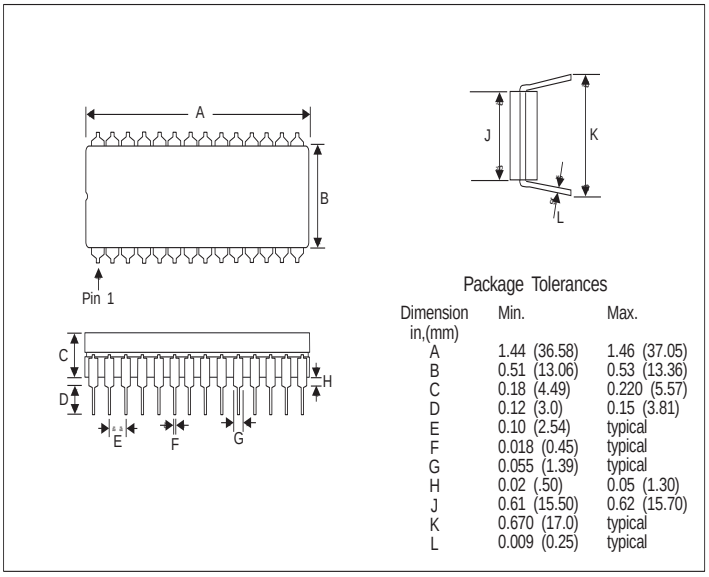
Package Outline

Figure 11 shows the MX812J Ceramic Dual In-Line, or Cerdip, Package. The MX812DW is shown in Figure 12. Pin 1 is marked with an indent spot on each chip. Pins number counter-clockwise when viewed from the top side.

Handling Precautions

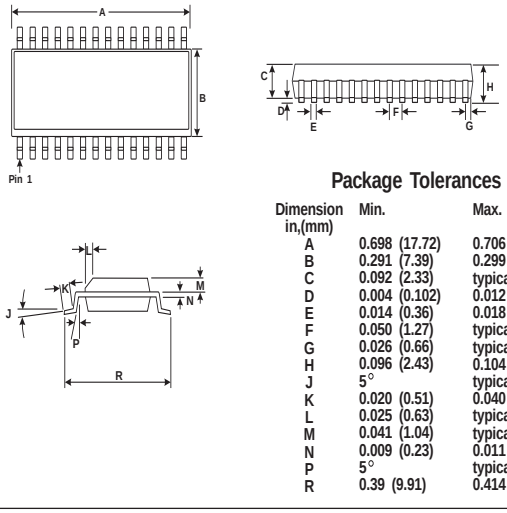
The MX812 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.



Package Tolerances

Dimension in,(mm)	Min.	Max.
A	1.44 (36.58)	1.46 (37.05)
B	0.51 (13.06)	0.53 (13.36)
C	0.18 (4.49)	0.220 (5.57)
D	0.12 (3.0)	0.15 (3.81)
E	0.10 (2.54)	typical
F	0.018 (0.45)	typical
G	0.055 (1.39)	typical
H	0.02 (.50)	0.05 (1.30)
J	0.61 (15.50)	0.62 (15.70)
K	0.670 (17.0)	typical
L	0.009 (0.25)	typical

Figure 11 - MX812J 28-pin Cerdip



Package Tolerances

Dimension in,(mm)	Min.	Max.
A	0.698 (17.72)	0.706 (17.97)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	5°	typical
R	0.39 (9.91)	0.414 (10.51)

Figure 12 - MX812DW SOIC-28 Package

