19-0110; Rev 0; 2/93

MAXIM

Quad, 12-Bit, µP-Compatible DAC

General Description

The MX390 contains four 12-bit, voltage-output digital-to-analog converters (DACs) in a compact 28-pin package. The design is based on a double-buffered, 12-bit DAC that reduces chip count and provides high reliability. The MX390 is ideal for systems requiring digital control of many analog voltages where board space is critical.

The monolithic voltage-output DACs inside the MX390 are laser-trimmed to ±1/2LSB max nonlinearity (MX390KD/TD) and absolute accuracy of ±0.05% of full scale. The internal buried-zener voltage reference provides excellent temperature drift characteristics (20ppm/°C max) and 5mV accuracy. The internal reference buffer provides a high input impedance (>1000MΩ) so that multiple MX390 devices can be driven by a single reference voltage.

The individual DACs are accessed by four chip-select inputs and the A0 and A1 lines. These control signals allow the registers of the four DACs to be loaded individually and the outputs to be updated simultaneously.

Applications

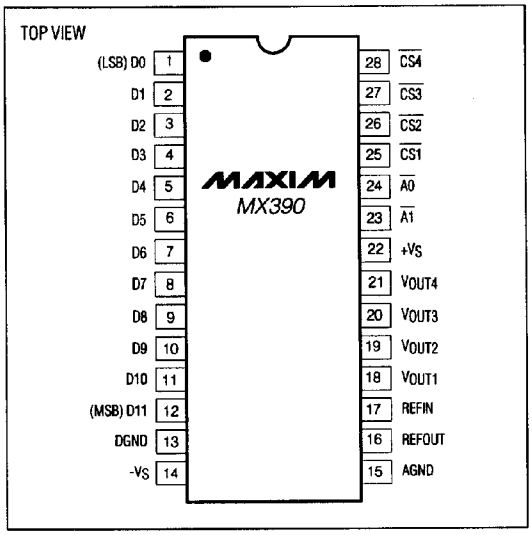
Military Products

Minimum Component Count Analog Systems

Control Systems

Test Equipment

Pin Configuration



Features

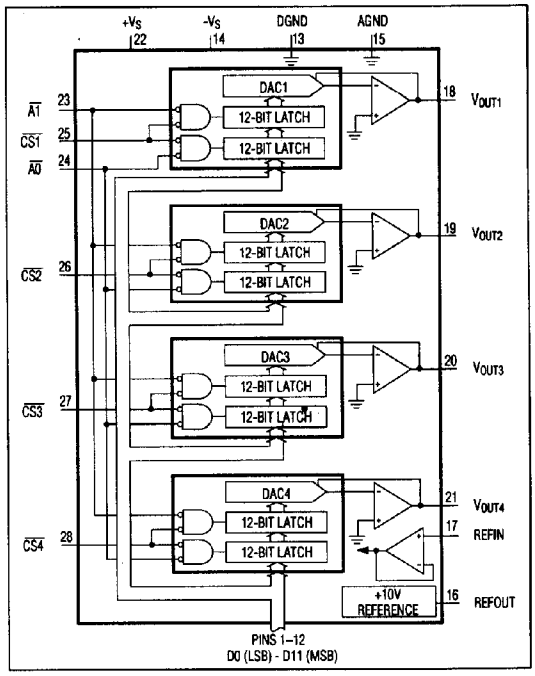
- **Pin-Compatible Upgrade to AD390**
  Lower Power: 1W
  MIL-STD-883B Qualified*
- **INL ±1/2LSB Max over Military Temperature**
- **Monotonicity Guaranteed Over Temperature**
- **Double-Buffered Data Latches**
- **Includes Precision Reference and Buffer**
- **Fast Settling: 8µs Max to 1/2LSB**

** Contact factory for availability.*

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MX390JD	0°C to +70°C	28 Ceramic SB	±3/4
MX390KD	0°C to +70°C	28 Ceramic SB	±1/2
MX390SD	-55°C to +125°C	28 Ceramic SB	±3/4
MX390TD	-55°C to +125°C	28 Ceramic SB	±1/2

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

+V_S to DGND ..... 0V DC to +18V DC
-V_S to DGND ..... 0V DC to -18V DC
Digital Inputs (pins 1-12 and 23-28) to DGND ..... -0.3V to (+V_S + 0.3V DC)
REFIN to AGND ..... ±V_S
AGND to DGND ..... ±0.6V
Outputs (pins 16, 18-21)
  Shorted to AGND or DGND ..... Continuous
  Shorted to ±V_S ..... Momentary

Continuous Power Dissipation (T_A = +70°C)
  28-Pin Ceramic SB (derate 33mW/°C above +70°C) ... 3.5W
Operating Temperature Ranges:
  MX390JD/KD ..... 0°C to +70°C
  MX390SD/TD ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature Range (Tj) ..... +175°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MX390JD/SD			MX390KD/TD			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Pins 1-12 and 23-28)									
Input Voltage High	V_{IH}		2.0			2.0			V
Input Voltage Low	V_{IL}				0.8			0.8	V
Input Current High	I_{IH}	V_{IN} = 5V		10	1200		10	1200	µA
Input Current Low	I_{IL}	V_{IN} = 0V		10	400		10	400	µA
Resolution					12			12	Bits
OUTPUT (Note 1)									
Voltage Range (Note 2)	V_{OUT}	External 10.000V reference			±10			±10	V
Current			±5			±5			mA
Settling Time	t_{SETT}	To ±1/2LSB		4	8		4	8	µs
ACCURACY									
Gain Error (Note 3)	A_e	External 10.000V reference, all bits high		±0.05	±0.1		±0.025	±0.05	% FSR
Offset Error	V_{OS}	External 10.000V reference, all bits low		±0.025	±0.05		±0.012	±0.025	% FSR
Integral Linearity Error	LE			±0.25	±0.75		±0.125	±0.5	LSB
Differential Linearity Error	DLE			±0.5	±0.75		±0.25	±0.5	LSB
TEMPERATURE DRIFT									
Gain	T_C/A_E	Internal reference			±40			±20	ppm/°C
		External 10.000V reference			±10			±5	
Bipolar Zero	$T_{C/PBZ}$				±10			±5	ppm/°C
Integral Linearity Error	LE	T_A = T_{MIN} to T_{MAX}		±0.5	±0.75		±0.25	±0.5	LSB
Differential Linearity Error	DLE	Monotonicity guaranteed over full temperature range							
CROSSTALK (Note 4)				0.1			0.1		LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MX390JD/SD			MX390KD/TD			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE OUTPUT									
Voltage		No load	9.995	10.000	10.005	9.995	10.000	10.005	V
Current		Available externally	2.5	3.5		2.5	3.5		mA
REFERENCE INPUT									
Input Resistance				10^{10}			10^{10}		Ω
Voltage Range			5		11	5		11	V
POWER REQUIREMENTS									
Voltages	±V_S	10V reference	±13.5	±15	±16.5	±13.5	±15	±16.5	V
		External 8.192V reference	±11.4		±16.5	±11.4		±16.5	
Currents +V_S	I_{CC}			38	50		38	50	mA
-V_S	I_{EE}			-26	-40		-26	-40	mA
Power Dissipation		V_S = ±15V		0.96	1.35		0.96	1.35	W
POWER-SUPPLY GAIN SENSITIVITY									
+V_S	PSRR+	+V_S = +15ç ±10%, -V_S = -15V		±0.002	±0.006		±0.002	±0.006	%FSR/%
-V_S	PSRR-	-V_S = −15V ±10%, +V_S = 15V		±0.002	±0.006		±0.002	±0.006	%FSR/%
TIMING SPECIFICATIONS									
$\overline{CS1}$-$\overline{CS4}$ Valid Before A0 Rising Edge	t_{AW}		100			100			ns
$\overline{A0}$, $\overline{A1}$ Low Time	t_{WP}		100			100			ns
Data Valid Before A0 Rising Edge	t_{DW}		50			50			ns
Data Valid After $\overline{A0}$ Rising Edge	t_{DH}		10			10			ns
$\overline{CS1}$-$\overline{CS4}$ Valid Before $\overline{A1}$ Low	t_{AS}		0			0			ns

Note 1: The MX390 outputs are guaranteed stable for load capacitances up to 500pF.
Note 2: ±10V range is standard. Contact factory for 0V to +10V range.
Note 3: Full-scale range (FSR) = 20V for the ±10V bipolar range.
Note 4: Crosstalk is defined as the change in any one output as a result of any other output being driven from -10V to +10V, 2kΩ load.

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MX390 Digital Circuit Details

Data and Control Signal Format

The MX390 data input format is 12-bit parallel. The DAC register is selected by control signals $\overline{CS1}$-$\overline{CS4}$, while the latches are controlled by the signals $\overline{A0}$ and $\overline{A1}$. The input registers are double-buffered, allowing any register to be updated independently of the others. As detailed in Table 1, the four chip-select lines address the DAC register of interest. More than one chip select may be active at any time. The first-rank register of a given DAC is loaded by bringing the appropriate chip select and A0 both low. The second-rank register of any DAC is then loaded by bringing the appropriate chip select and $\overline{A1}$ both low. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident with $\overline{A1}$ low, all four DAC outputs will be updated to the value in the corresponding first-rank registers. All control inputs are level-sensitive and may be hard-wired low to render any register (or group of registers) transparent.

Timing

The MX390 control-signal timing is fairly straightforward. The desired control signals from $\overline{A0}$, $\overline{A1}$, and $\overline{CS1}$-$\overline{CS4}$ must be concurrently valid for at least 100ns for an operation to occur. Data is latched on the rising edge of $\overline{A0}$ and $\overline{A1}$. When loading data from a bus into the first-rank register, the data setup time is 50ns and the data hold time is zero. When loading the second-rank registers, it is possible to excerise the chip-select inputs simultaneously with $\overline{A1}$. DAC settling time is measured from the falling edge of the last control signal to be asserted.

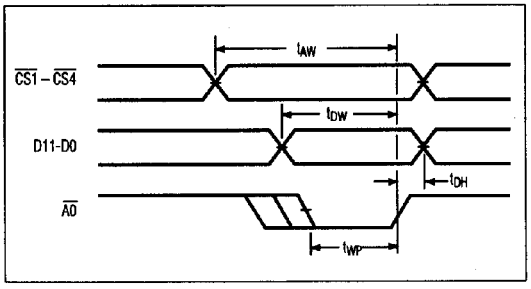

Figure 1a. Write-Cycle Timing Diagram

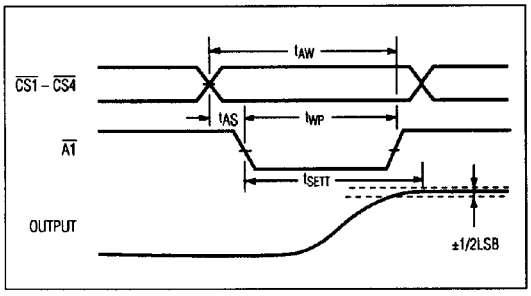

Figure 1b. Write-Cycle Timing Diagram

Reference Connections

The MX390 is equipped with an internal reference of 10V ±5mV. This reference is available for external use and can typically source up to 3.5mA. In normal operation, this reference is connected to REFIN, which establishes the ±10V output scale. If higher accuracy or a range other than ±10V is desired, an external reference such as the MAX671 (1ppm/°C) may be used.

Power-Supply Decoupling

Decouple +V_S and -V_S to AGND using a 10µF capacitor in parallel with a 0.1µF ceramic capacitor with short leads. AGND and DGND should be returned separately to the system ground.

Table 1. MX390 Truth Table

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{A1}$	$\overline{A0}$	OPERATION
1	1	1	1	X	X	No operation
X	X	X	X	1	1	No operation
0	1	1	1	1	0	Enable first rank of DAC1
1	0	1	1	1	0	Enable first rank of DAC2
1	1	0	1	1	0	Enable first rank of DAC3
1	1	1	0	1	0	Enable first rank of DAC4
0	1	1	1	0	1	Load DAC1 second rank from first rank
1	0	1	1	0	1	Load DAC2 second rank from first rank
1	1	0	1	0	1	Load DAC3 second rank from first rank
1	1	1	0	0	1	Load DAC4 second rank from first rank
0	0	0	0	0	0	All latches transparent

Table 2. MX390 Analog Output vs. Digital Input (±10V Scale)

Digital Input Code			Analog Output Voltage	
0000	0000	0000	-10.00V	- Full Scale
0100	0000	0000	-5.000V	- 1/2 Scale
1000	0000	0000	0.000V	Zero
1000	0000	0001	+4.88mV	+ 1LSB
1100	0000	0000	+5.000V	+ 1/2 Scale
1111	1111	1111	+9.9951V	+ Full Scale - 1LSB