MX23L8100

8M-BIT MASK ROM(8/16 BIT OUTPUT)

FEATURES

- Bit organization
  - 1M x 8 (byte mode)
  - 512K x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
- Current
  - Operating: 20mA
  - Standby: 5uA
- Supply voltage
  - 3.3V±10%
- Package
  - 44 pin SOP (500mil)
  - 42 pin PDIP (600mil)
  - 48 pin TSOP (type 1)
  - 44 pin TSOP (type 2)

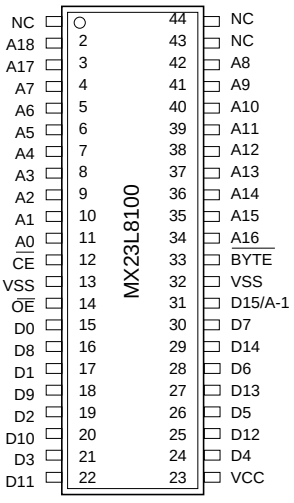
ORDER INFORMATION

Part No.	Access Time	Package
MX23L8100MC-10	100ns	44 pin SOP
MX23L8100MC-12	120ns	44 pin SOP
MX23L8100MC-15	150ns	44 pin SOP
MX23L8100PC-10	100ns	42 pin PDIP
MX23L8100PC-12	120ns	42 pin PDIP
MX23L8100PC-15	150ns	42 pin PDIP
MX23L8100TC-10	100ns	48 pin TSOP*
MX23L8100TC-12	120ns	48 pin TSOP
MX23L8100TC-15	150ns	48 pin TSOP
MX23L8100RC-10	100ns	48 pin RTSOP*
MX23L8100RC-12	120ns	48 pin RTSOP
MX23L8100RC-15	150ns	48 pin RTSOP
MX23L8100YC-10	100ns	44 pin TSOP
MX23L8100YC-12	120ns	44 pin TSOP
MX23L8100TI-10	100ns	48 pin TSOP*

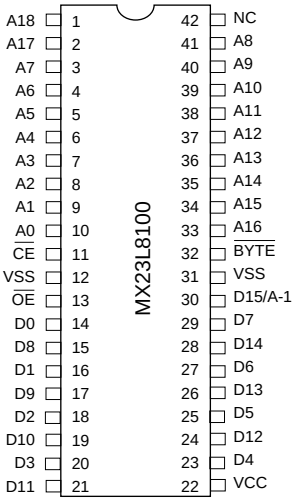
Note: 1.48-TSOP and 48-RTSOP support word mode only, not for byte mode.
2.MX23L8100TI-10 is for industrial grade, temperature -40~85℃

PIN CONFIGURATION

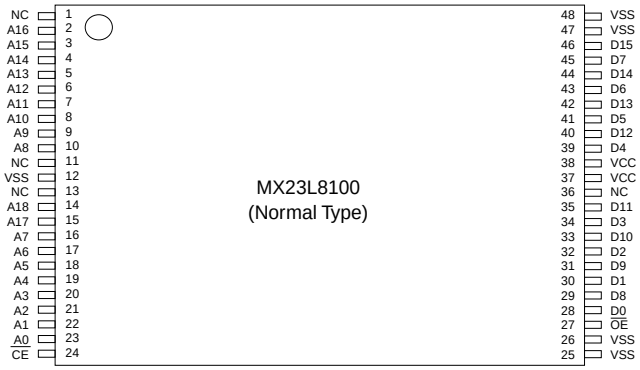
44 SOP/44TSOP



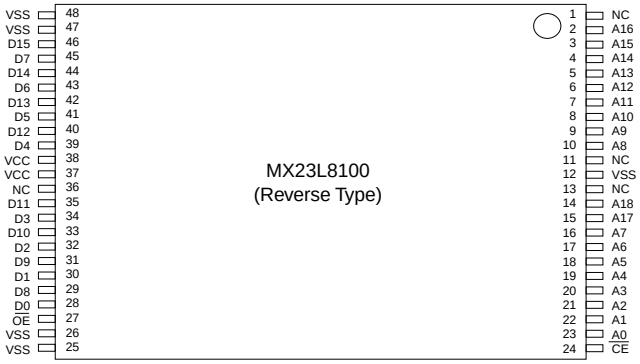
42 PDIP



48 TSOP (for word mode only)



48 Reverse TSOP (for word mode only)



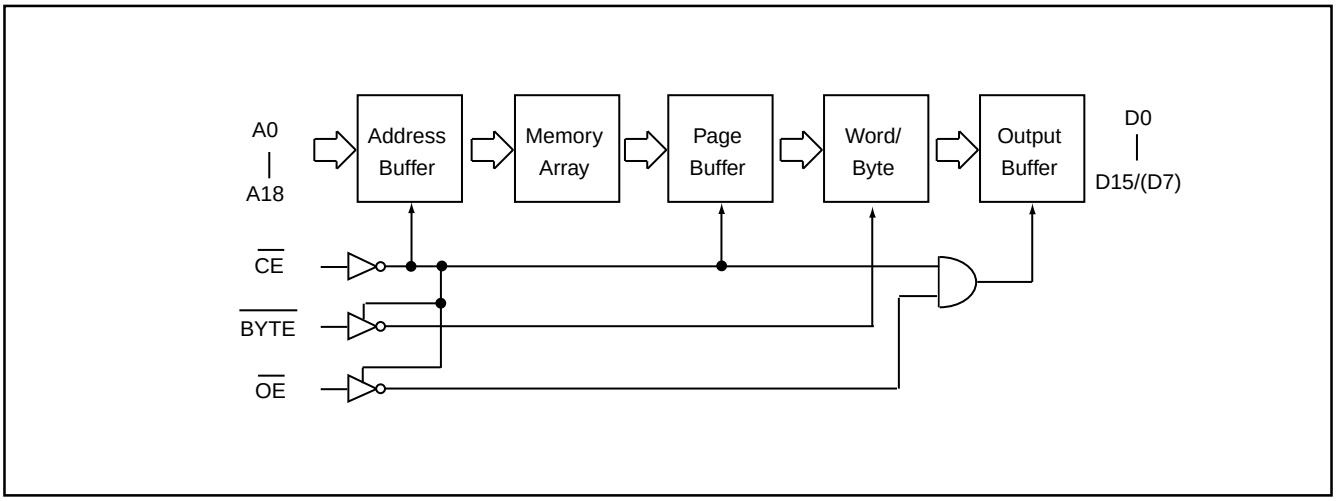
PIN DESCRIPTION

Symbol	Pin Function
A0~A18	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15(Word Mode)/LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{Byte}$	Word/Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{Byte}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	Topr	0℃ to 70℃
Storage Temperature	Tstg	-65℃ to 125℃

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	24V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	20mA	f=10MHz, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$=VIH
Standby Current (CMOS)	ISTB2	-	5uA	$\overline{CE}$> VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25℃, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25℃, f = 1MHZ

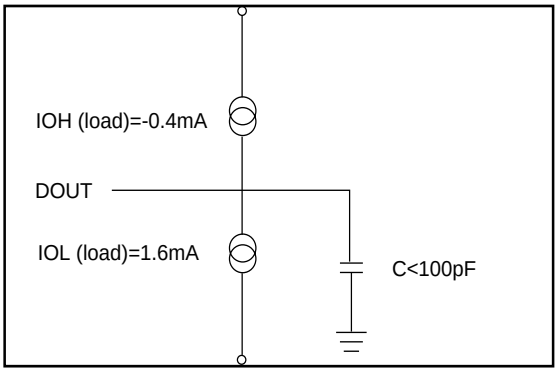
AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.3V±10%)

Item	Symbol	23L8100-10		23L8100-12		23L8100-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note:Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

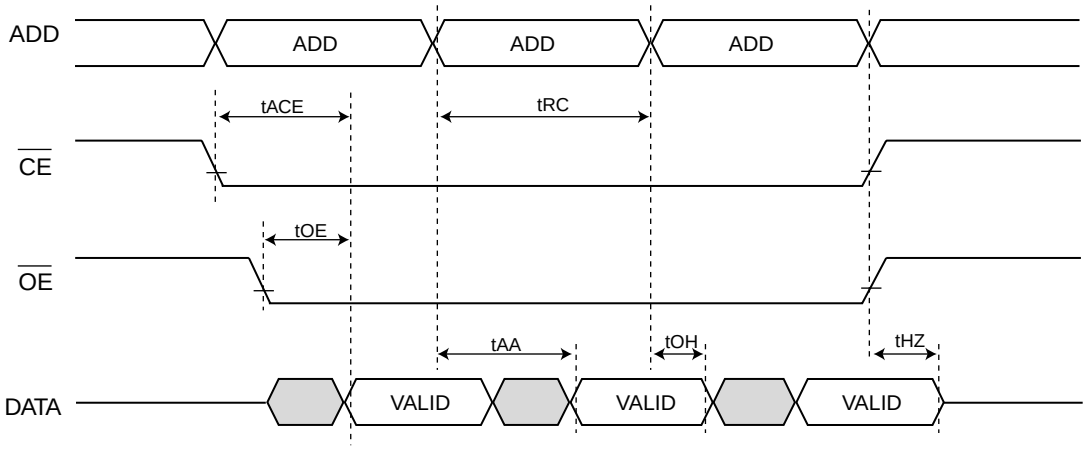
Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

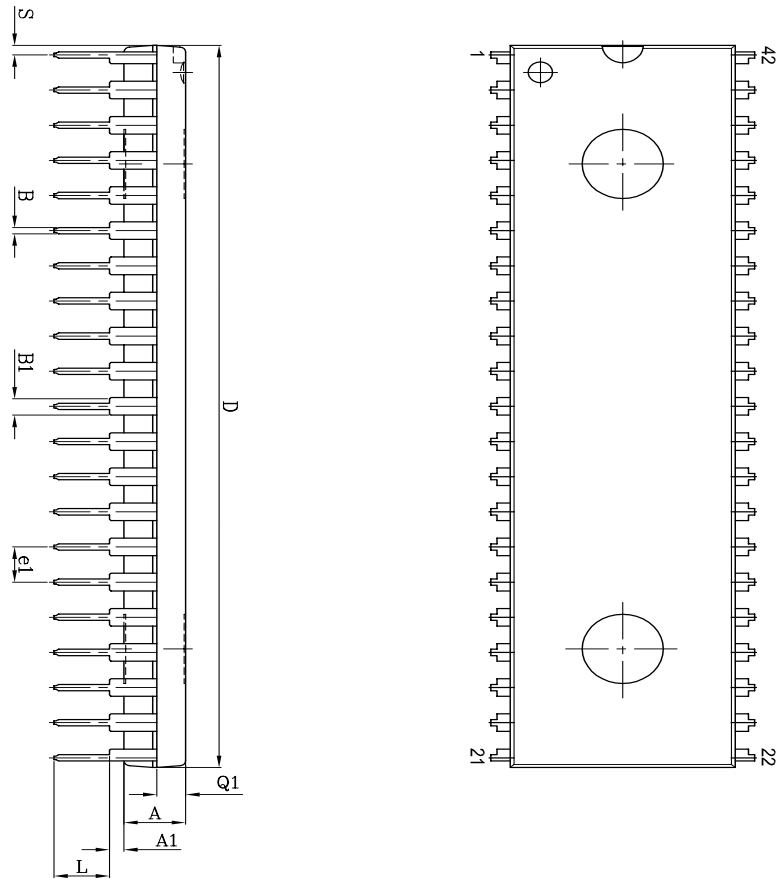
RANDOM READ



Note:$\overline{CE}$, $\overline{OE}$ are enable

PACKAGE INFORMATION

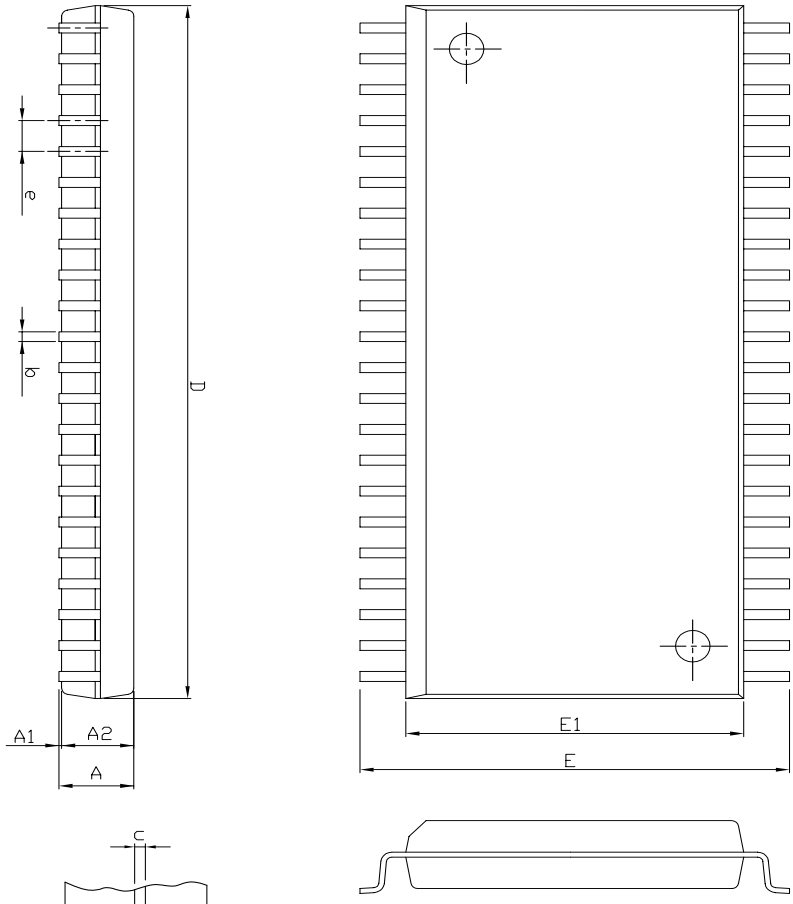
42-PIN PLASTIC DIP(600 mil)



SYMBOL / UNIT	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	2.05±0.005	52.07±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.025±0.005	0.635±0.127

MXIC 旺宏電子股份有限公司				DWG. NO.
Macronix International Co., Ltd.				6110-0202.5
TITLE				TOLERANCE
PACKAGE OUTLINE FOR PDIP 42L (600 MIL)			UNIT	.X ± .1 ANGLE .XX ±.01 .XXX±.002
DRAWN	APPROVED	DATE		REVISION
C.L.Chiang	Leo Lee	05-02-01		4

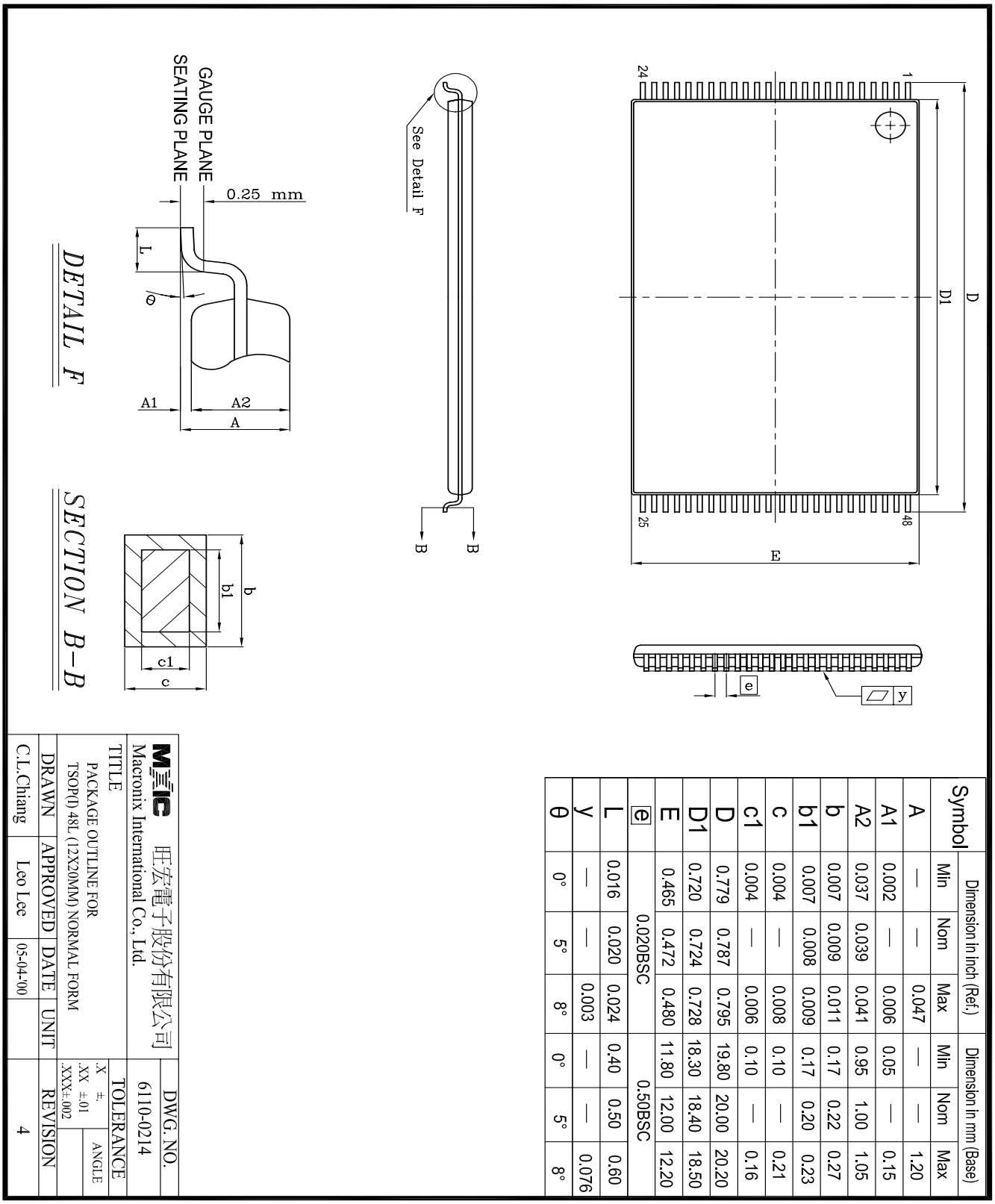
44-PIN PLASTIC SOP



Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b		0.41REF			0.016 REF	
c		0.20 REF			0.008 REF	
D	28.37	28.50	28.63	1.117	1.122	1.127
E	15.77	16.03	16.28	0.621	0.631	0.641
E1	12.47	12.60	12.73	0.491	0.496	0.501
e		1.27 REF			0.050 REF	
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—	5°	—	—	5°	—
JEDEC						

MIC 旺宏電子股份有限公司			DWG. NO.
Macronix International Co., Ltd.			6110-0207
TITLE			TOLERANCE
PACKAGE OUTLINE FOR SOP 44L (500 MIL)			X ±. / .XX ±.01 / .XXX±.002 / ANGLE / ROUGHNESS
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Dennis Chang	05-03-'01	INCH
			REVISION
			2

48-PIN PLASTIC TSOP



Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A1	0.002	—	0.006	0.05	—	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
c	0.004	—	0.008	0.10	—	0.21
c1	0.004	—	0.006	0.10	—	0.16
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	0.465	0.472	0.480	11.80	12.00	12.20
e		0.020BSC			0.50BSC	
L	0.016	0.020	0.024	0.40	0.50	0.60
y	—	—	0.003	—	—	0.076
θ	0°	5°	8°	0°	5°	8°

MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd.			DWG. NO. 6110-0214
TITLE PACKAGE OUTLINE FOR TSOP(I) 48L (12X20MM) NORMAL FORM			TOLERANCE .X ± ANGLE .XX ±.01 .XXX±.002
DRAWN	APPROVED	DATE	UNIT
C.L.Chiang	Leo Lee	05-04-'00	
			REVISION 4

REVISION HISTORY

Revision	Description	Page	Date
1.4	Add new 44pin TSOP (type 2)		Jul/17/1998
1.5	AC CHARACTERISTICS tOH 10ns-->0ns	P3	FEB/01/1999
1.6	Correct Typing error	P1	JUL/16/2001
	Modify Package Information	P5~7	
1.7	Added MX23L8100TI-10 in Order Information	P1	AUG/20/2001

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