

74VCX162245

Low Voltage 16-Bit Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in A Port Outputs

General Description

The VCX162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The OE inputs disable both the A and B ports by placing them in a high impedance state.

The 74VCX162245 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V. The 74VCX162245 is also designed with 26Ω series resistance in the A Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74VCX162245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.4V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in A port outputs
- t_{PD} (B to A)
 - 3.4 ns max for 3.0V to 3.6V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL} A outputs)
 - ±12 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Note 1: To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX162245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

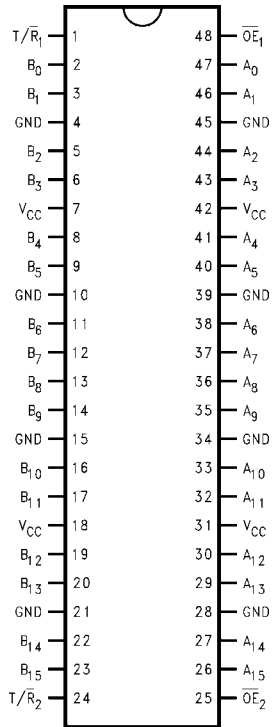
Logic Symbol



Pin Descriptions

Pin Names	Description
OE _n	Output Enable Input
T/R _n	Transmit/Receive Input
A ₀ -A ₁₅	Side A Inputs or 3-STATE Outputs
B ₀ -B ₁₅	Side B Inputs or 3-STATE Outputs

Connection Diagram



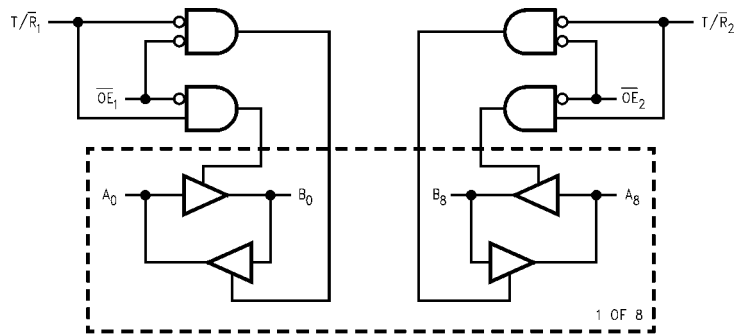
Truth Tables

Inputs		Outputs
\overline{OE}_1	T/\overline{R}_1	
L	L	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇
L	H	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇
H	X	HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇

Inputs		Outputs
\overline{OE}_2	T/\overline{R}_2	
L	L	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅
L	H	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅
H	X	HIGH Z State on A ₈ -A ₁₅ , B ₈ -B ₁₅

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
 Z = High Impedance

Logic Diagram



Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-State	-0.5V to +4.6V
Outputs Active (Note 3)	-0.5 to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.4V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	-0.3V to 3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL} -A Outputs	
$V_{CC} = 3.0V$ to 3.6V	± 12 mA
$V_{CC} = 2.3V$ to 2.7V	± 8 mA
$V_{CC} = 1.65V$ to 1.95V	± 3 mA
Output Current in $\pm I_{OH}/I_{OL}$ -B Outputs	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused pins (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
V_{OH}	HIGH Level Output Voltage A Outputs	$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -8$ mA $I_{OH} = -12$ mA	2.7 - 3.6	$V_{CC} - 0.2$		V
			2.7	2.2		
			3.0	2.4		
			3.0	2.2		
		$I_{OH} = -100 \mu A$ $I_{OH} = -4$ mA $I_{OH} = -6$ mA $I_{OH} = -8$ mA	2.3 - 2.7	$V_{CC} - 0.2$		
			2.3	2.0		
			2.3	1.8		
			2.3	1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -3$ mA $I_{OH} = -100 \mu A$ $I_{OH} = -1$ mA	1.65 - 2.3	$V_{CC} - 0.2$		
			.65	1.4		
			1.4 - 1.6	$V_{CC} - 0.2$		
			1.4	1.05		

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{OH}	HIGH Level Output Voltage B Outputs	I _{OH} = -100 μA	2.7 - 3.6	V _{CC} - 0.2		V
		I _{OH} = -12 mA	2.7	2.2		
		I _{OH} = -18 mA	3.0	2.4		
		I _{OH} = -24 mA	3.0	2.2		
		I _{OH} = -100 μA	2.7 - 3.6	V _{CC} - 0.2		
		I _{OH} = -6 mA	2.3	2.0		
		I _{OH} = -12 mA	2.3	1.8		
		I _{OH} = -18 mA	2.3	1.7		
		I _{OH} = -100 μA	1.65 - 2.3	V _{CC} - 0.2		
		I _{OH} = -6 mA	1.65	1.25		
V _{OL}	LOW Level Output Voltage A Outputs	I _{OL} = 100 μA	2.7 - 3.6		0.2	V
		I _{OL} = 6 mA	2.7		0.4	
		I _{OL} = 8 mA	3.0		0.55	
		I _{OL} = 12 mA	3.0		0.8	
		I _{OL} = 100 μA	2.3 - 2.7		0.2	
		I _{OL} = 6 mA	2.3		0.4	
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 100 μA	1.65 - 2.3		0.2	
		I _{OL} = 3 mA	1.65		0.3	
		I _{OL} = 100 μA	1.4 - 1.6		0.2	
I _{OL} = 2 mA	1.4		0.35			
V _{OL}	LOW Level Output Voltage B Outputs	I _{OL} = 100 μA	2.7 - 3.6		0.2	V
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 18 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
		I _{OL} = 100 μA	2.3 - 2.7		0.2	
		I _{OL} = 12 mA	2.3		0.4	
		I _{OL} = 18 mA	2.3		0.6	
		I _{OL} = 100 μA	1.65 - 2.3		0.2	
		I _{OL} = 6 mA	1.65		0.3	
		I _{OL} = 100 μA	1.4 - 1.6		0.2	
I _{OL} = 2 mA	1.4		0.35			
I _I	Input Leakage Current	0V ≤ V _I ≤ 3.6V	2.7 - 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0V ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	2.7 - 3.6		±10	μA
I _{OFF}	Power Off Leakage Current	0V ≤ (V _I , V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 5)	2.7 - 3.6		20	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		750	μA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 6)							
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PHL} , t _{PLH}	Propagation Delay B to A	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.4	ns	Figures 1, 2
			2.5 ± 0.2	1.0	4.3		
			1.8 ± 0.15	1.5	8.6		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	17.2		Figures 5, 6
t _{PZL} , t _{PZH}	Output Enable Time B to A	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	4.2	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	5.7		
			1.8 ± 0.15	1.5	9.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 7, 8
t _{PLZ} , t _{PHZ}	Output Disable Time B to A	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	4.1	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.8		
			1.8 ± 0.15	1.5	8.6		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	17.2		Figures 5, 7, 8
t _{PHL} , t _{PLH}	Propagation Delay A to B	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	2.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.0		
			1.8 ± 0.15	1.5	6.0		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	12.0		Figures 5, 6
t _{PZL} , t _{PZH}	Output Enable Time A to B	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.1		
			1.8 ± 0.15	1.5	8.2		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	16.4		Figures 5, 7, 8
t _{PLZ} , t _{PHZ}	Output Disable Time A to B	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	3.8		
			1.8 ± 0.15	1.5	6.8		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1	1.0	13.6		Figures 5, 7, 8
t _{OSHL} , t _{OSLH}	Output-to-Output Skew (Note 7)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C _L = 15 pF, R _L = 2kΩ	1.5 ± 0.1		1.5		

Note 6: For C_L = 50pF, add approximately 300ps to the AC maximum specification.

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics						
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units	
				Typical		
V _{OLP}	Quiet Output Dynamic Peak V _{OL} , A to B	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.25	V	
			2.5	0.6		
			3.3	0.8		
V _{OLP}	Quiet Output Dynamic Peak V _{OL} , B to A	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.15	V	
			2.5	0.25		
			3.3	0.35		
V _{OLV}	Quiet Output Dynamic Valley V _{OL} , A to B	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.25	V	
			2.5	-0.6		
			3.3	-0.8		
V _{OLV}	Quiet Output Dynamic Valley V _{OL} , B to A	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.15	V	
			2.5	-0.25		
			3.3	-0.35		
V _{OHV}	Quiet Output Dynamic Valley V _{OH} , A to B	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.5	V	
			2.5	1.9		
			3.3	2.2		
V _{OHV}	Quiet Output Dynamic Valley V _{OH} , B to A	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.55	V	
			2.5	2.05		
			3.3	2.65		
Capacitance						
Symbol	Parameter	Conditions	T _A = +25°C	Units		
C _{IN}	Input Capacitance	V _{CC} = 1.8V, 2.5V, or 3.3V, V _I = 0V or V _{CC}	6	pF		
C _{I/O}	Output Capacitance	V _I = 0V, or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7	pF		
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz V _{CC} = 1.8V, 2.5V or 3.3V	20	pF		

AC Loading and Waveforms (V_{CC} 3.3V ± 0.3V to 1.8V ± 0.15V)

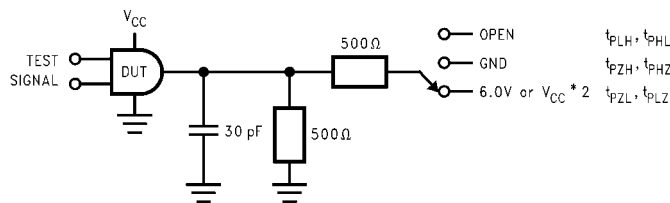


FIGURE 1. AC Test Circuit

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$; $1.8V \pm 0.15V$
t_{PZH} , t_{PHZ}	GND

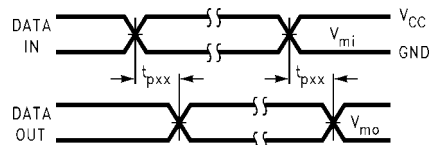


FIGURE 2. Waveform for Inverting and Non-inverting Functions

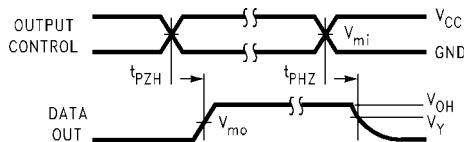


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for LOW Voltage Logic

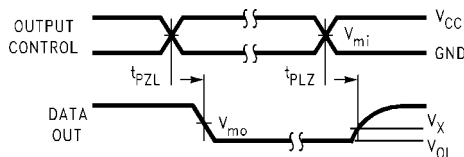


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for LOW Voltage Logic

Symbol	V_{CC}		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

AC Loading and Waveforms ($V_{CC} 1.5V \pm 0.1V$)

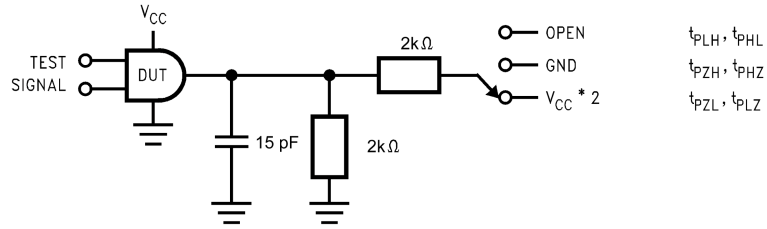


FIGURE 5. AC Test Circuit

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	$V_{CC} \times 2$ at $V_{CC} = 1.5V \pm 0.1V$
t_{PZH}, t_{PHZ}	GND

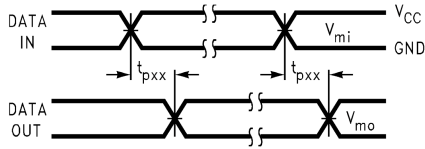


FIGURE 6. Waveform for Inverting and Non-inverting Functions

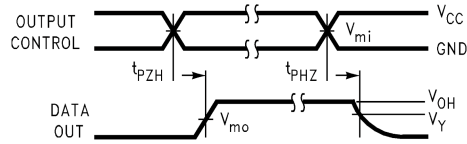


FIGURE 7. 3-STATE Output HIGH Enable and Disable Times for LOW Voltage Logic

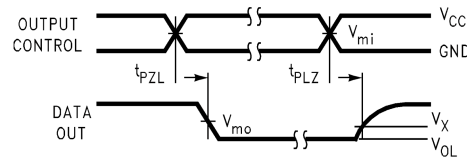
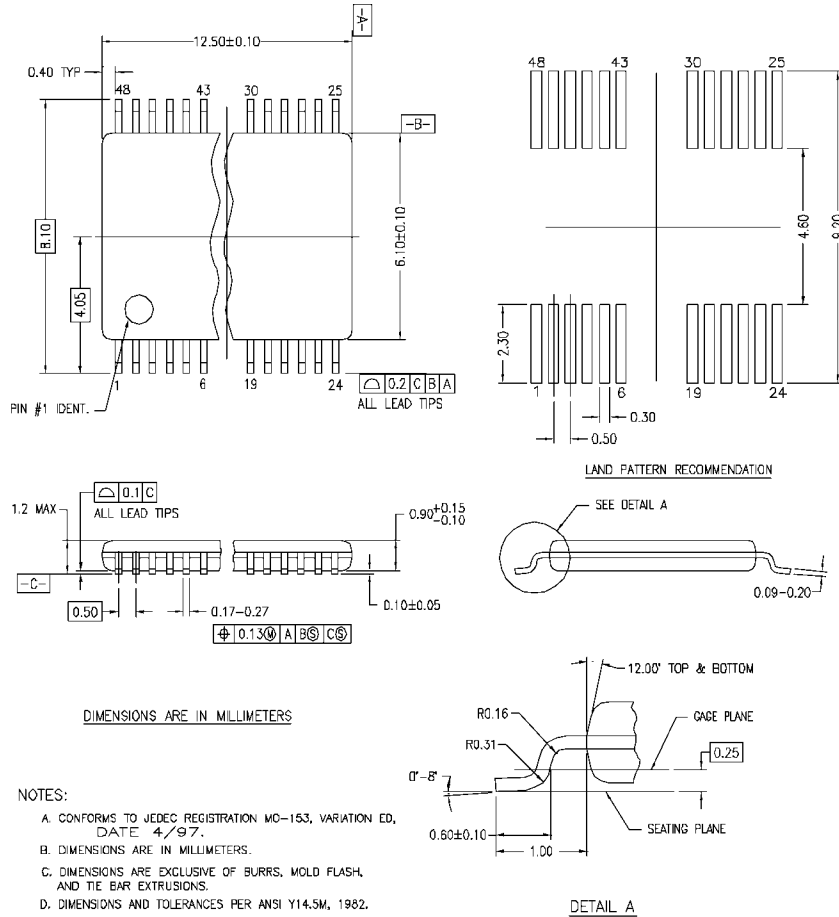


FIGURE 8. 3-STATE Output LOW Enable and Disable Times for LOW Voltage Logic

Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_X	$V_{OL} + 0.1V$
V_Y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted



MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com