

# DRAM MODULE

## 2 MEG x 32 DRAM FAST PAGE MODE

DRAM MODULE

### FEATURES

- Industry standard pinout in a 72-pin single-in-line package
- High-performance, CMOS silicon gate process.
- Single 5V ±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 48mW standby; 3600mW active, typical
- Refresh modes:  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  and HIDDEN
- 1,024-cycle refresh distributed across 16ms
- Optional FAST PAGE MODE access cycle

### OPTIONS

- Timing
  - 70ns access
  - 80ns access
  - 100ns access

### Packages

- Leadless 72-pin SIMM M
- Leadless 72-pin SIMM (Gold) G
- Leaded 72-pin ZIP Z

### MARKING

- 7
- 8
- 10

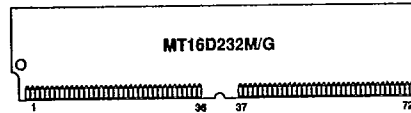
### GENERAL DESCRIPTION

The MT16D232 is a randomly accessed solid-state memory containing 2,097,152 words organized in a x32 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time.  $\overline{\text{RAS}}$  is used to latch the first 10 bits and  $\overline{\text{CAS}}$  the latter 10 bits. A READ or WRITE cycle is selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. EARLY-WRITE occurs when  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, the output pin(s) remain open (High-Z) until the next  $\overline{\text{CAS}}$  cycle.

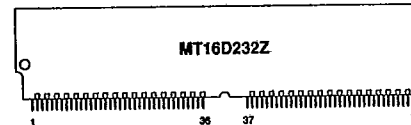
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address (A0-A9) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by  $\overline{\text{RAS}}$  followed by a column address strobed-in by  $\overline{\text{CAS}}$ .  $\overline{\text{CAS}}$  may

### PIN ASSIGNMENT (Top View)

72-Pin SIMM (I-6)



72-Pin ZIP (J-5)



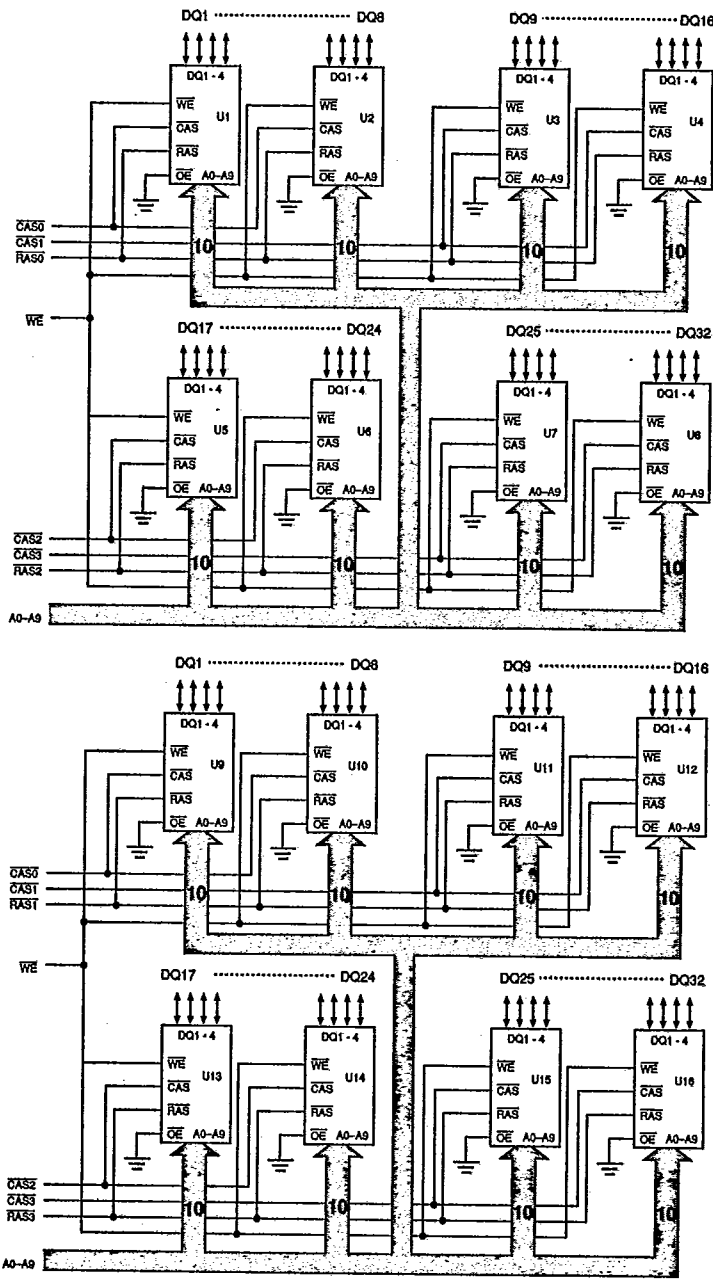
PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	CAS0	58	DQ29
5	DQ18	23	DQ22	41	CAS2	59	Vcc
6	DQ3	24	DQ7	42	CAS3	60	DQ30
7	DQ19	25	DQ23	43	CAS1	61	DQ14
8	DQ4	26	DQ8	44	RAS0	62	DQ31
9	DQ20	27	DQ24	45	RAS1	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ32
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	A9	50	DQ25	68	PRD2
15	A3	33	RAS3	51	DQ10	69	PRD3
16	A4	34	RAS2	52	DQ26	70	PRD4
17	A5	35	NC	53	DQ11	71	NC
18	A6	36	NC	54	DQ27	72	Vss

be toggled-in by holding  $\overline{\text{RAS}}$  LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning  $\overline{\text{RAS}}$  HIGH terminates the FAST PAGE MODE operation.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ , or HIDDEN REFRESH) so that all 1,024 combination of  $\overline{\text{RAS}}$  addresses (A0-A9) are executed at least every 16ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM

DRAM MODULE



U1-U16 = MT4C4001DJ

TRUTH TABLE

Function	RAS	CAS	WE	Addresses		DQ1-32	
				'R	'C		
Standby	H	X	X	X	X	High Impedance	
READ	L	L	H	ROW	COL	Valid Data Out	
EARLY-WRITE	L	L	L	ROW	COL	Valid Data In	
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Valid Data Out
	2nd Cycle	L	H→L	H	n/a	COL	Valid Data Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Valid Data In
	2nd Cycle	L	H→L	L	n/a	COL	Valid Data In
RAS-ONLY REFRESH	L	H	X	ROW	n/a	High Impedance	
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Valid Data Out
	WRITE	L→H→L	L	L	ROW	COL	Valid Data In
CAS-BEFORE-RAS REFRESH	H→L	L	X	X	X	High Impedance	

DRAM MODULE

PRESENCE DETECT

SYMBOL	-7	-8	-10
PRD1	NC	VSS	NC
PRD2	NC	VSS	NC
PRD3	VSS	VSS	NC
PRD4	NC	NC	NC

ABSOLUTE MAXIMUM RATINGS\*

Voltage on Vcc supply relative to Vss .....-1.0V to +7.0V  
 Operating Temperature, TA(Ambient) .....0°C to +70°C  
 Storage Temperature (Plastic) .....-55°C to +150°C  
 Power Dissipation ..... 16W  
 Short Circuit Output Current .....50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 3, 4, 6, 7) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ )

DRAM MODULE

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	$V_{CC}$	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	$V_{IH}$	2.4	$V_{CC}+1$	V	1
Input Low (Logic 0) Voltage, All Inputs	$V_{IL}$	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input $0\text{V} \leq V_{IN} \leq V_{CC}$ (All other pins not under test = 0V) For each package input	A0-A9, WE $I_i$	-32	32	$\mu\text{A}$	
OUTPUT LEAKAGE CURRENT (Q is disabled, $0\text{V} \leq V_{OUT} \leq V_{CC}$ ) For each package input	DQ1-DQ32 $I_{OZ}$	-24	24	$\mu\text{A}$	
OUTPUT LEVELS Output High Voltage ( $I_{OH} = -5\text{mA}$ ) Output Low Voltage ( $I_{OL} = 5\text{mA}$ )	$V_{OH}$ $V_{OL}$	2.4	0.4	V	1

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-7	-8	-10		
OPERATING CURRENT ( $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling; $t_{RC} = t_{RC}(\text{MIN})$ )	$I_{CC1}$	816	736	656	mA	2
OPERATING CURRENT: FAST PAGE MODE ( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ = Cycling; $t_{PC} = t_{PC}(\text{MIN})$ )	$I_{CC2}$	576	496	416	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ after 8 $\overline{\text{RAS}}$ cycles (MIN))	$I_{CC3}$	32	32	32	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ after 8 $\overline{\text{RAS}}$ cycles (MIN)). (All other inputs at $V_{CC} - 0.2\text{V}$ or $V_{SS} + 0.2\text{V}$ )	$I_{CC4}$	16	16	16	mA	
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY ( $\overline{\text{RAS}}$ = Cycling; $\overline{\text{CAS}} = V_{IH}$ )	$I_{CC5}$	816	736	656	mA	2
REFRESH CURRENT: $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ ( $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = Cycling)	$I_{CC6}$	816	736	656	mA	2

**CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	$C_{I1}$		80	pF	17
Input Capacitance: WE	$C_{I2}$		112	pF	17
Input Capacitance: $\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$ , $\overline{\text{RAS0}}$ - $\overline{\text{RAS3}}$	$C_{I4}$		28	pF	17
Input/Output Capacitance: DQ1-DQ32	$C_{IO}$		14	pF	17

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 3, 4, 5, 10, 11, 16, 17) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$ )

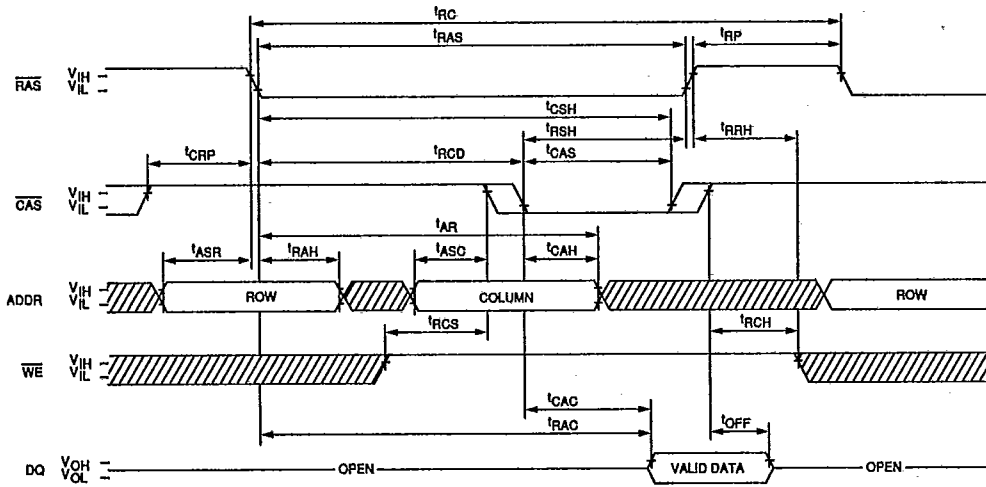
DRAM MODULE

A.C. CHARACTERISTICS PARAMETER	SYM	-7		-8		-10		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	<sup>t</sup> RC	130		150		180		ns	6, 7
FAST-PAGE-MODE cycle time	<sup>t</sup> PC	40		45		55		ns	6, 7
Access time from RAS	<sup>t</sup> RAC		70		80		100	ns	7, 8
Access time from $\overline{\text{CAS}}$	<sup>t</sup> CAC		20		20		25	ns	7, 9
RAS pulse width	<sup>t</sup> RAS	70	100,000	80	100,000	100	100,000	ns	
RAS hold time	<sup>t</sup> RSH	20		20		25		ns	
RAS precharge time	<sup>t</sup> RP	50		60		70		ns	
$\overline{\text{CAS}}$ pulse width	<sup>t</sup> CAS	20	100,000	20	100,000	25	100,000	ns	
$\overline{\text{CAS}}$ hold time	<sup>t</sup> CSH	70		80		100		ns	
$\overline{\text{CAS}}$ precharge time	<sup>t</sup> CPN	10		10		15		ns	18
$\overline{\text{CAS}}$ precharge time (FAST PAGE MODE)	<sup>t</sup> CP	10		10		10		ns	
RAS to $\overline{\text{CAS}}$ delay time	<sup>t</sup> RCD	20	50	20	60	25	75	ns	13
$\overline{\text{CAS}}$ to RAS setup time	<sup>t</sup> CRP	5		5		20		ns	
Row address setup time	<sup>t</sup> ASR	0		0		0		ns	
Row address hold time	<sup>t</sup> RAH	10		10		15		ns	
Column address setup time	<sup>t</sup> ASC	0		0		0		ns	
Column address hold time	<sup>t</sup> CAH	15		15		20		ns	
Column address hold time referenced to RAS	<sup>t</sup> AR	55		60		70		ns	
Read command setup time	<sup>t</sup> RCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	<sup>t</sup> RCH	0		0		0		ns	14
Read command hold time referenced to RAS	<sup>t</sup> RRH	0		0		0		ns	
Output buffer turn-off delay	<sup>t</sup> OFF	0	20	0	20	0	20	ns	12
$\overline{\text{WE}}$ command setup time	<sup>t</sup> WCS	0		0		0		ns	
Write command hold time	<sup>t</sup> WCH	15		15		20		ns	
Write command hold time referenced to RAS	<sup>t</sup> WCR	55		60		75		ns	
Write command pulse width	<sup>t</sup> WP	15		15		20		ns	
Write command to RAS lead time	<sup>t</sup> RWL	15		20		25		ns	
Write command to $\overline{\text{CAS}}$ lead time	<sup>t</sup> CWL	15		20		25		ns	
Data-in setup time	<sup>t</sup> DS	0		0		0		ns	15
Data-in hold time	<sup>t</sup> DH	15		15		20		ns	15
Data-in hold time referenced to RAS	<sup>t</sup> DHR	55		60		75		ns	
Transition time (rise or fall)	<sup>t</sup> T	3	50	3	50	3	50	ns	16
Refresh period (256 cycles)	<sup>t</sup> REF		16		16		16	ms	20
$\overline{\text{CAS}}$ hold time (CAS-BEFORE-RAS REFRESH)	<sup>t</sup> CHR	15		15		15		ns	19
$\overline{\text{CAS}}$ set-up time (CAS-BEFORE-RAS REFRESH)	<sup>t</sup> CSR	10		10		10		ns	19
RAS to $\overline{\text{CAS}}$ precharge time	<sup>t</sup> RPC	0		0		0		ns	19

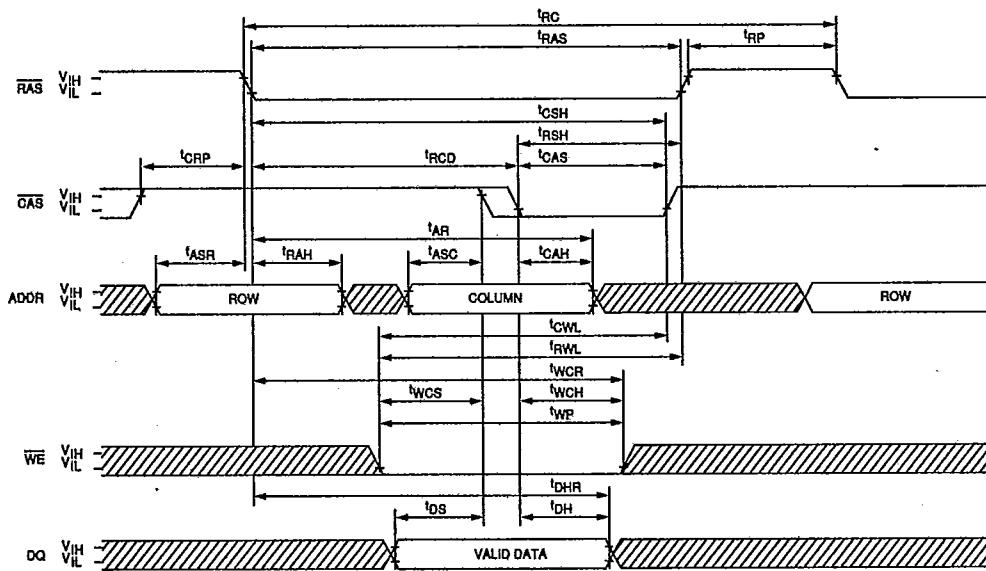
## NOTES

1. All voltages referenced to  $V_{SS}$ .
2.  $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100 $\mu$ s is required after power-up followed by eight  $\overline{RAS}$  REFRESH cycles ( $\overline{RAS}$ -ONLY or CBR with  $\overline{WE}$  HIGH) before proper device operation is assured. The eight  $\overline{RAS}$  cycle wake-up should be repeated any time the 16ms refresh requirement is exceeded.
4. AC characteristics assume  $t_T = 5$ ns.
5.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is assured.
7. Measured with a load equivalent to two TTL gates and 100pF.
8. Assumes that  $t_{RCD} < t_{RCD}(\text{MAX})$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
9. Assumes that  $t_{RCD} \geq t_{RCD}(\text{MAX})$ .
10. If  $\overline{CAS} = V_{IH}$ , data output is high impedance.
11. If  $\overline{CAS} = V_{IL}$ , data output may contain data from the last valid READ cycle.
12.  $t_{OFF}(\text{MAX})$  defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
13. Operation within the  $t_{RCD}(\text{MAX})$  limit ensures that  $t_{RAC}(\text{MAX})$  can be met.  $t_{RCD}(\text{MAX})$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{MAX})$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
14.  $t_{RCH}$  is referenced to the first rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ .
15. These parameters are referenced to  $\overline{CAS}$  leading edge in EARLY-WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
17. This parameter is sampled. Capacitance is calculated from the equation  $C = I^{di}/dv$  with  $dv = 3\text{V}$  and  $V_{CC} = 5\text{V}$ .
18. If  $\overline{CAS}$  is LOW at the falling edge of  $\overline{RAS}$ , data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer,  $\overline{CAS}$  must be pulsed HIGH for  $t_{CP}$ . Note 8 applies to determine valid data out.
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{WE} = \text{LOW}$ .
21. LATE-WRITE, READ-WRITE or READ-MODIFY-WRITE cycles are not available due to  $\overline{OE}$  being grounded on U1-U16.

READ CYCLE



EARLY-WRITE CYCLE



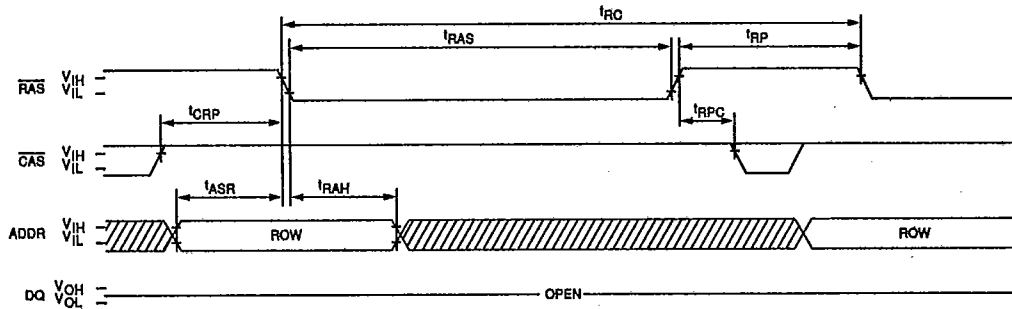
 DON'T CARE  
 UNDEFINED

DRAM MODULE

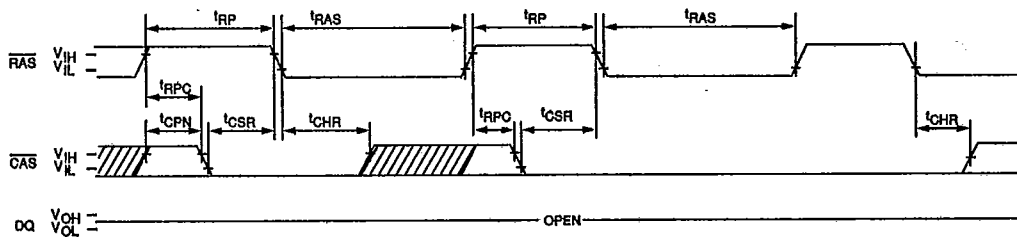




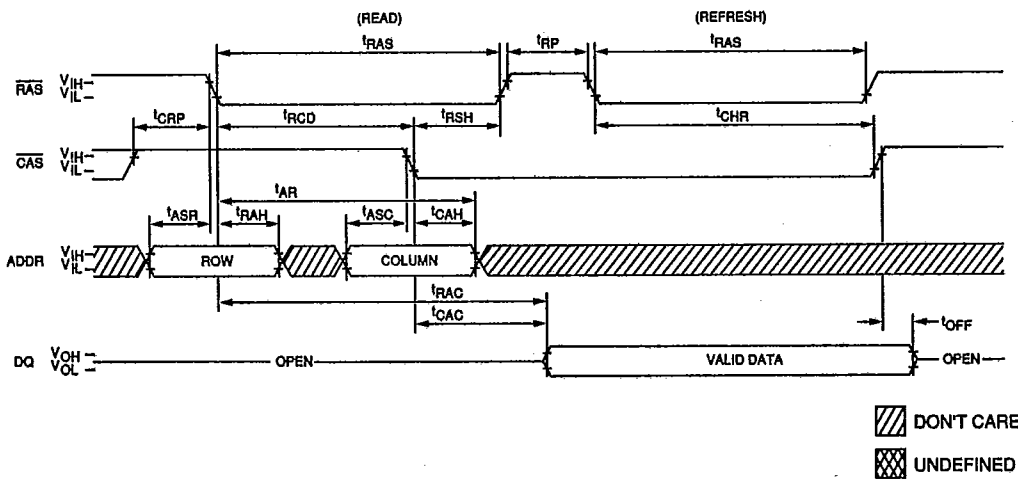
**RAS-ONLY REFRESH CYCLE**  
(ADDR = A<sub>0</sub> - A<sub>9</sub>; WE = DON'T CARE)



**CAS-BEFORE-RAS REFRESH CYCLE**  
(A<sub>0</sub> - A<sub>9</sub>; WE = DON'T CARE)



**HIDDEN REFRESH CYCLE**  
(WE = HIGH)<sup>20</sup>



DON'T CARE  
 UNDEFINED