

# OKI Semiconductor

## MSM7661B

### NTSC/PAL Digital Video Decoder

#### GENERAL DESCRIPTION

The MSM7661B is an LSI device which converts digitally sampled NTSC or PAL video signals to 8-bit format based on ITU-RBT601.

The input video signals available are composite video signals and S video signals.

The composite video signals are converted to YUV data via a 2-dimensional Y/C separation circuit.

The A-to-D converted data is data sampled at pixel clock frequency or double pixel clock frequency (the built-in decimation filter is used). Input signal synchronization can lock synchronization and color burst at high speed through internal digital processing.

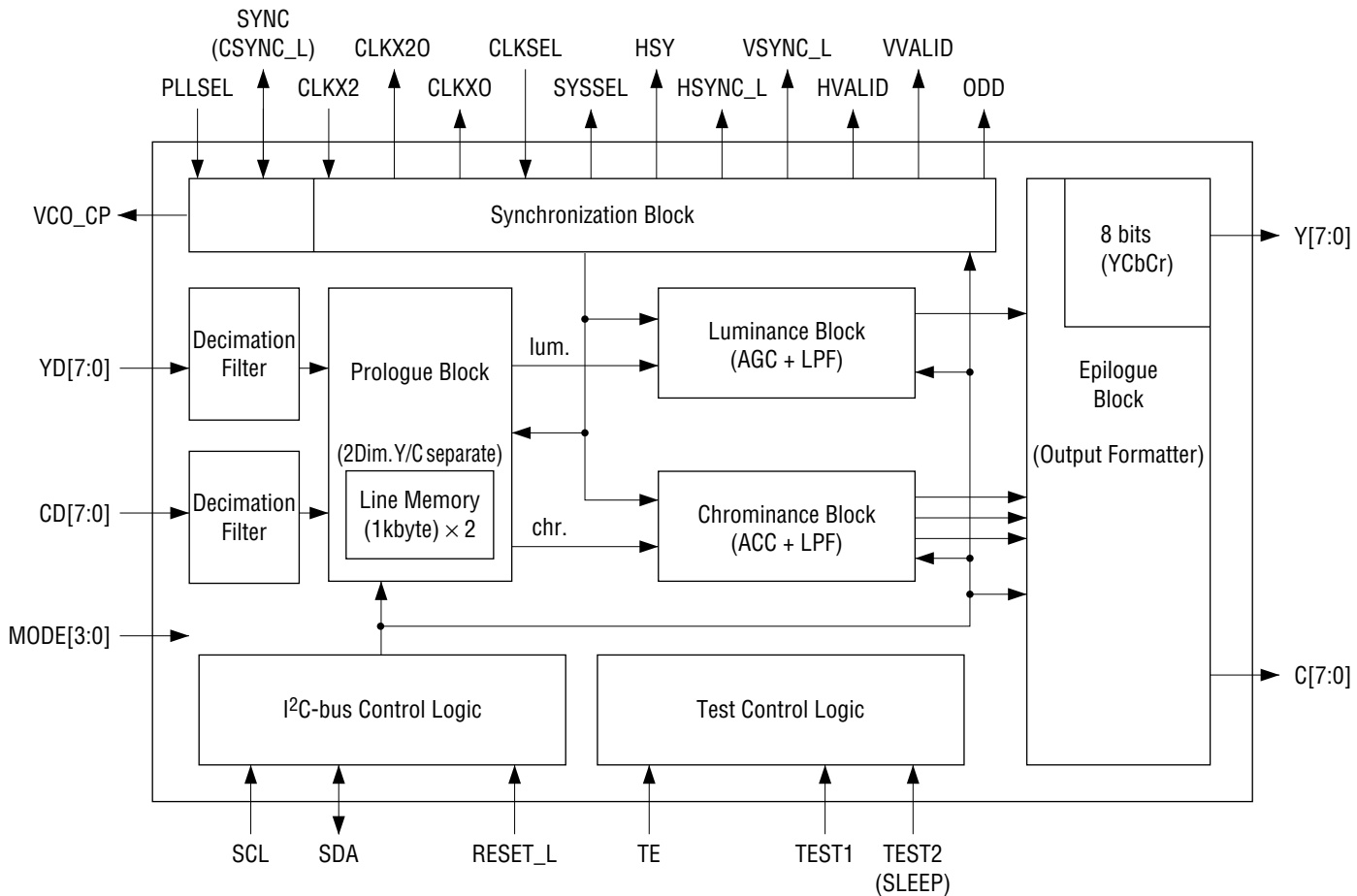
The MSM7661B is upward compatible with the MSM7661. It provides additional features which are added to the MSM7661 indicated by the mark ■ and is superior to the MSM7661 in picture quality and synchronization stability. The device, which includes an additional register added to the MSM7661, has electrical characteristics which are nearly equal to those of the MSM7661. The MSM7661B allows a pin-for-pin replacement with the MSM7661.

#### FEATURES (● indicates a new feature compared with MSM7660. ■ indicates a new feature compared with MSM7661.)

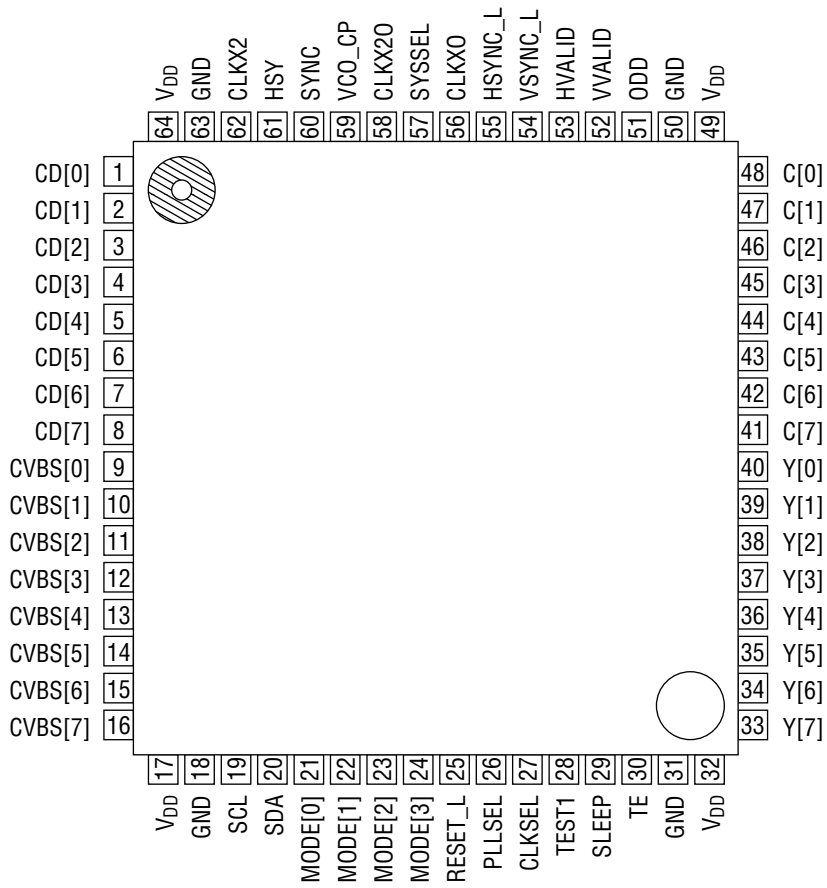
- Input video signals include the following two types of digital data that are A-to-D converted at pixel frequency or double pixel frequency :
  - NTSC/PAL composite video signal
  - NTSC/PAL S video signal
- 8-bit Y/8-bit C (CbCr) output (conforms to ITU-RBT601)
  - YCbCr            4 : 2 : 2
  - YCbC4 : 1 : 1
- YCbCr 8-bit multiplex output (27 MHz) (not including SAV and EAV)
- 2-dimensional Y/C separation using adaptive comb filter (this filter is bypassed for S video signal input)
  - NTSC: 3 lines/2 lines
  - PAL: 2 lines (3 virtual lines)
- Input signal synchronization can lock synchronization and color burst at high speed through internal digital processing.
- Sampling frequency
  - 13.5 MHz (ITU-R601)
  - 12.27 MHz (NTSC Square Pixel)
  - 14.31818 MHz (NTSC 4Fsc)
  - 14.75 MHz (PAL Square Pixel)
- Internal AGC/ACC circuit
  - Switchable between AGC and MGC (fixed gain)
- Switchable between ACC and MCC (fixed gain)
- Built-in decimation filter located in the input stage allows easy configuration of an external filter circuit (located ahead of A/D converter).
- Automatic NTSC/PAL recognition (only for ITU-RBT.601)
- Sleep mode

- Multiplex signal recognition (Teletext)  
Data during vertical blanking is output in 8 bits in Through mode.
- I<sup>2</sup>C-bus interface
- 3.3 V single power supply (each I/O pin is 5 V tolerable)
- Package:  
64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name: MSM7661B GS-BK)

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



**64-Pin Plastic QFP**



| Pin      | Symbol          | Type | Description   |
|----------|-----------------|------|---|
| 33 to 40 | Y[7 to 0]       | 0    | Chrominance signal output pins<br>YCbCr 8-bit multiplex output pins   |
| 41 to 48 | C[7 to 0]       | 0    | Luminance signal output pins  |
| 49       | V <sub>DD</sub> |      |   |
| 50       | GND             |      |   |
| 51       | ODD             | 0    | Field display output pin<br>Outputs "H" for odd field.  |
| 52       | VVALID          | 0    | Vertical valid line timing output pin   |
| 53       | HVALID          | 0    | Horizontal valid pixel timing output pin  |
| 54       | VSYNC_L         | 0    | V sync output pin   |
| 55       | HSYNC_L         | 0    | H sync output pin   |
| 56       | CLKXO           | 0    | Internal operation clock output pin   |
| 57       | SYSSEL          | 0    | Display select output pin for NTSC-PAL detect / multiplex signal detect / HLOCK sync detect.<br>Selection by register. (Default : NTSC-PAL detect)<br>NTSC mode : "L", PAL mode : "H"<br>Multiplex signal detect : "H"<br>HLOCK sync detect : "H" |
| 58       | CLKX2O          | 0    | Clock output pin  |
| 59       | VCO_CP          | 0    | Unused.<br>Open normally.   |
| 60       | SYNC            | I/O  | Composite sync output.<br>Unused as input pin.  |
| 61       | HSY             | 0    | Clamp signal timing output pin for A/D converter  |
| 62       | CLKX2           | I    | Clock input pin   |
| 63       | GND             |      |   |
| 64       | V <sub>DD</sub> |      |   |

**ABSOLUTE MAXIMUM RATINGS**

| Parameter            | Symbol    | Condition | Rating       | Unit |
|----------------------|-----------|-----------|--------------|------|
| Power Supply Voltage | $V_{DD}$  | —         | -0.3 to +4.5 | V    |
| Input Voltage        | $V_I$     | —         | -0.3 to +5.5 | V    |
| Power Consumption    | $P_W$     | —         | 800          | mW   |
| Storage Temperature  | $T_{STG}$ | —         | -55 to +150  | °C   |

**RECOMMENDED OPERATING CONDITIONS**

| Parameter               | Symbol   | Condition | Min. | Typ. | Max.     | Unit |
|-------------------------|----------|-----------|------|------|----------|------|
| Power Supply Voltage    | $V_{DD}$ | —         | 3.0  | 3.3  | 3.6      | V    |
| Power Supply Voltage    | GND      | —         | —    | 0    | —        | V    |
| "H" Level Input Voltage | $V_{IH}$ | —         | 2.2  | —    | $V_{DD}$ | V    |
| "L" Level Input Voltage | $V_{IL}$ | —         | 0    | —    | 0.8      | V    |
| Operating Temperature   | $T_a$    | —         | 0    | 25   | 70       | °C   |

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

(Ta = 0 to 70°C, VDD = 3.3 V ±0.3 V)

| Parameter                        | Symbol            | Condition                                 | Min.                | Typ. | Max. | Unit |
|----------------------------------|-------------------|---|---------------------|------|------|------|
| "H" Level Output Voltage         | VOH               | I <sub>OH</sub> = -4 mA (*1)              | 0.7 V <sub>DD</sub> | —    | —    | V    |
|                                  |                   | I <sub>OH</sub> = -6 mA (*2)              |                     |      |      |      |
|                                  |                   | I <sub>OH</sub> = -8 mA (*3)              |                     |      |      |      |
| "L" Level Output Voltage         | VOL               | I <sub>OL</sub> = 4 mA (*1)               | —                   | —    | 0.4  | V    |
|                                  |                   | I <sub>OL</sub> = 6 mA (*2)               |                     |      |      |      |
|                                  |                   | I <sub>OL</sub> = 8 mA (*3)               |                     |      |      |      |
| Input Leak Current               | II                | V <sub>I</sub> = GND to V <sub>DD</sub>   | -10                 | —    | +10  | μA   |
|                                  |                   | R <sub>pull-down</sub> = 50 kΩ (*4)       | 20                  | —    | 250  |      |
| Output Leak Current              | IO                | V <sub>I</sub> = GND to V <sub>DD</sub>   | -10                 | —    | +10  | μA   |
| Power Supply Current (operating) | IDDO              | CLK = 27 MHz<br>V <sub>DD</sub> = 3.3 V   | —                   | 155  | 190  | mA   |
| Power Supply Current (operating) | IDDO2             | CLK = 13.5 MHz<br>V <sub>DD</sub> = 3.3 V | —                   | 125  | 160  | mA   |
| Power Supply Current (SLEEP)     | IDDS              | SLEEP ON                                  | —                   | 1    | 5    | mA   |
| SDA Output Voltage               | SDAV <sub>L</sub> | —   | 0                   | —    | 0.4  | V    |
| SDA Output Current               | SDAI <sub>O</sub> | —   | 3                   | —    | —    | mA   |

\*1: HSYNC\_L, VSYNC\_L, SYSSEL

\*2: Y[7:0], C[7:0], HSY, HVALID, VVALID, ODD, CLKXO

\*3: CLKX2O

\*4: MODE[3:0], SLEEP, TEST1, TE



**AC Characteristics (Single Speed Mode)**

(Ta = 0 to 70°C, VDD = 3.3 V ±0.3 V)

| Parameter                              | Symbol             | Condition         | Min. | Typ.  | Max. | Unit |
|--|--------------------|-------------------|------|-------|------|------|
| CLKX2 Cycle Time                       | t <sub>CLKX1</sub> | ITU-R601          | —    | 74.07 | —    | ns   |
|  |                    | NTSC 4Fsc         | —    | 69.84 | —    | ns   |
|  |                    | NTSC Square Pixel | —    | 81.5  | —    | ns   |
|  |                    | PAL Square Pixel  | —    | 67.8  | —    | ns   |
| CLKX2 Duty                             | t <sub>D_D1</sub>  | —                 | 40   | —     | 60   | %    |
| Input Data Setup Time                  | t <sub>IS1</sub>   | CLKSEL : H        | 0    | —     | —    | ns   |
| Input Data Hold Time                   | t <sub>IH1</sub>   | CLKSEL : H        | 30   | —     | —    | ns   |
| Output Data Delay Time 1 (*)           | t <sub>ODX1</sub>  | CLKSEL : H        | 2    | —     | 8    | ns   |
| Output Data Delay Time 2 (*)           | t <sub>OD2X1</sub> | CLKSEL : H        | 2    | —     | 7    | ns   |
| Output Data Delay Time 3 (*)           | t <sub>OD1</sub>   | CLKSEL : H        | 9    | —     | 25   | ns   |
| Output Clock Delay Time (*) (External) | t <sub>CXD1</sub>  | CLKSEL : H        | 7    | —     | 17   | ns   |
| Output Clock Delay Time (*) (Internal) | t <sub>CD1</sub>   | CLKSEL : H        | 7    | —     | 18   | ns   |
| SCL Clock Cycle Time                   | t <sub>C_SCL</sub> | Rpull_up = 4.7 kΩ | 200  | —     | —    | ns   |
| Low Level Cycle                        | t <sub>L_SCL</sub> | Rpull_up = 4.7 kΩ | 100  | —     | —    | ns   |

(\*output load 40 pF)

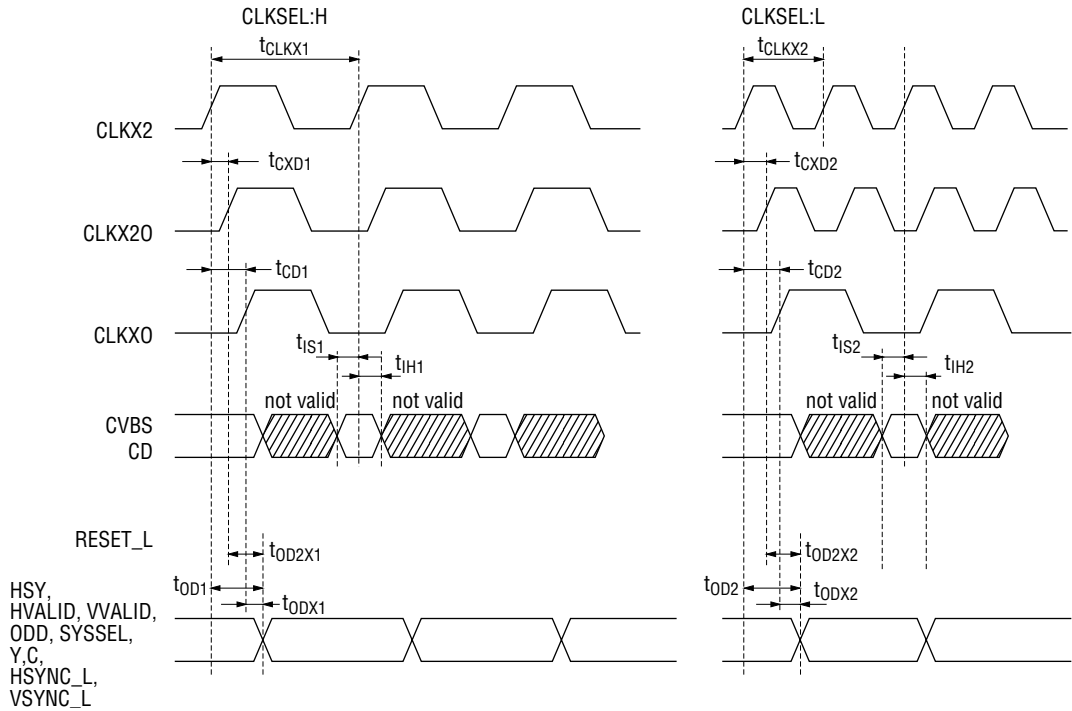
**AC Characteristics (Double Speed Mode)**

(Ta = 0 to 70°C, VDD = 3.3 V ±0.3 V)

| Parameter                              | Symbol             | Condition         | Min. | Typ.  | Max. | Unit |
|--|--------------------|-------------------|------|-------|------|------|
| CLKX2 Cycle Time                       | t <sub>CLKX2</sub> | ITU-R601          | —    | 37.05 | —    | ns   |
|  |                    | NTSC 4Fsc         | —    | 34.9  | —    | ns   |
|  |                    | NTSC Square Pixel | —    | 40.75 | —    | ns   |
|  |                    | PAL Square Pixel  | —    | 33.9  | —    | ns   |
| CLKX2 Duty                             | t <sub>D_D2</sub>  | —                 | 40   | —     | 60   | %    |
| Input Data Setup Time                  | t <sub>IS2</sub>   | CLKSEL : L        | 5    | —     | —    | ns   |
| Input Data Hold Time                   | t <sub>IH2</sub>   | CLKSEL : L        | 15   | —     | —    | ns   |
| Output Data Delay Time 1 (*)           | t <sub>ODX2</sub>  | CLKSEL : L        | 2    | —     | 7    | ns   |
| Output Data Delay Time 2 (*)           | t <sub>OD2X2</sub> | CLKSEL : L        | 2    | —     | 6    | ns   |
| Output Data Delay Time 3 (*)           | t <sub>OD2</sub>   | CLKSEL : L        | 9    | —     | 24   | ns   |
| Output Clock Delay Time (*) (External) | t <sub>CXD2</sub>  | CLKSEL : L        | 7    | —     | 17   | ns   |
| Output Clock Delay Time (*) (Internal) | t <sub>CD2</sub>   | CLKSEL : L        | 7    | —     | 18   | ns   |
| SCL Clock Cycle Time                   | t <sub>C_SCL</sub> | Rpull_up = 4.7 kΩ | 200  | —     | —    | ns   |
| Low Level Cycle                        | t <sub>L_SCL</sub> | Rpull_up = 4.7 kΩ | 100  | —     | —    | ns   |

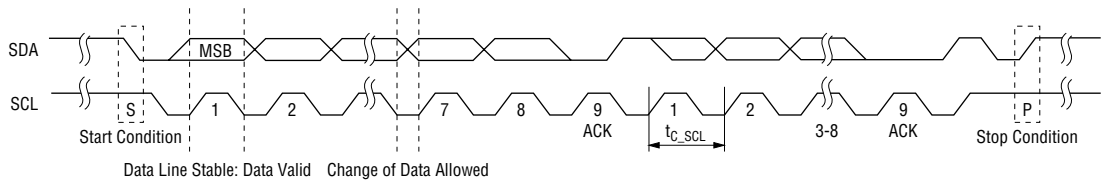
(\*output load 40 pF)

### Input and Output Timing



### I<sup>2</sup>C-bus Interface Input/Output Timing

The basic input/output timing of the I<sup>2</sup>C-bus interface is as follows.



### I<sup>2</sup>C-bus Basic Input/Output Timing

## BLOCK DESCRIPTION

### 1. Prologue Block

The prologue block performs Y/C separation by inputting data.

Data can be input either at ordinary pixel frequency (ITU-R : 13.5 MHz) or at double pixel frequency (ITU-R: 27 MHz).

When the double pixel frequency is used, data is processed after changing to the ordinary pixel frequency via a decimeter circuit.

By changing the register setting, the decimeter circuit can be bypassed irrespective of whether data is input at ordinary pixel frequency or at double pixel frequency.

The prologue block performs Y/C separation using a 2-dimensional adaptive comb filter when composite signals (CVBS) are input.

The following operation modes can be changed via the I<sup>2</sup>C-bus. The \* mark indicates a default. The default is a state that is selected when reset.

- 1) Video input mode select
  - Composite video input \*
  - S video input
  
- 2) Video input mode select
  - Auto NTSC/PAL select\* (Only for ITU-R601)
  - Dependent on Operation mode selected
  - When ITU-R601 is selected, the video input mode is automatically determined by the number of lines per field.
  
- 3) Operation mode select
 

|                   |              |
|-------------------|--------------|
| NTSC CCIR601      | 13.5 MHz*    |
| MTSC Square Pixel | 12.27 MHz    |
| NTSC 4Fsc         | 14.31818 MHz |
| PAL CCIR601       | 13.5 MHz     |
| PAL Square Pixel  | 14.75 MHz    |
  
- 4) Decimeter circuit pass/bypass select
  - Decimeter circuit is passed. \*
  - Decimeter circuit is bypassed.
  
- 5) Y/C separation mode select
  - Adaptive comb filter is used. \*
  - Unadaptive comb filter is used.
  - Trap filter is used.

The adaptive comb filter detects the correlation up to 3 lines between continuous lines. The Y/C is separated by the comb filter according to the way of correlation if these lines are correlated. The Y/C is separated by the trap filter if these lines are not correlated (only 2 lines in the case of PAL).

In the unadaptive comb filter, the Y/C is always separated by removing the luminance component based on the average of preceding and following lines (when there is the correlation between 3 lines).

If the comb filter is not used, the Y/C is separated by the trap filter.  
 The Y/C separation circuit is bypassed by S video signal input.  
 In addition, the functions of this block work only when lines are valid as image information.  
 The processing of CVBS signals is not made during V-blanking.

## 2. Luminance Block

The luminance block removes synchronous signals from the signals containing luminance components after Y/C separation. The signals are corrected and output as luminance signals. The luminance signal output level gain control functions include three selectable modes such as AGC (Auto Gain Control), MGC (manual Gain Control) + No Clamp, and MGC + Pedestal Clamp.

In the AGC mode, the luminance level amplification is determined by comparing the depth of SYNC with the reference value. The default is 40IRE which can be changed by the register. The input is a sync chip clamp type.

In the MGC + No Clamp mode, the luminance signal output level is not affected by the input, and the amplification and black level are controlled by setting the register.

In the MGC + Pedestal Clamp mode, the signal output level is clamped to the pedestal level of the input. The signal amplification and black level are controllable from the clamped point by setting the register.

This block can select the following operation modes.

- 1) Use of prefilter and sharp filter
  - Used\*
  - Not used

These filters are used for enhancing the edges of luminance component signals.
- 2) Selection of aperture bandpass filter coefficient
  - Middle range\*
  - High range
- 3) Coring range select
  - off\*
  - ±4LBS
  - ±5LBS
  - ±7LBS
- 4) Aperture weighting factor select
  - 0\*
  - 0.25
  - 0.75
  - 1.5

The profile of these signals can be corrected by coring and aperture correction.

- 5) Use of pixel position correction circuit
  - Used\*
  - Not used
- 6) AGC loop filter time constant select
  - Slow
  - Factor value 1/1024n

|        |        |
|--------|--------|
| Medium | 1/64n* |
| Fast   | 1/n    |
| Fixed  | 0      |

- 7) Parameter for AGC reference level fine adjustment
- 8) Parameter for sync separation level fine adjustment

The black level is controlled. When the default is specified, the pedestal position is output as a black level (=16).

- 9) Pedestal clamp selecton
  - Pedestal clamp is not used.\*
  - Pedestal clamp is used. (AGC will not operate)

### 3. Chrominance Block

This is a chroma signal processing block.  
The following modes can be selected.

- 1) Use of color bandpass filter
  - Used\*
  - Not used
- 2) ACC loop filter time constant select
 

|        |                      |
|--------|----------------------|
| Slow   | Factor value 1/1024n |
| Medium | 1/64n*               |
| Fast   | 1/n                  |
| Fixed  | 0                    |
- 3) ACC reference level fine adjustment
- 4) Parameter for burst level fine adjustment
 

The threshold level for valid chroma amplitude is selected based on a color burst ratio.

  - 0.5
  - 0.25\*
  - 0.125
  - off
- 5) Color killer mode select
  - Auto color killer mode\*
  - Forcible color killer
- 6) Parameter for color subcarrier phase fine adjustment
 

In this block, chroma signals pass through the chroma bandpass filter to cut an unnecessary band. To maintain a constant chroma level, UV demodulation is performed on these signals via the ACC correction circuit. (This filter can be bypassed.)  
If the demodulation result does not reach a specified level, color killer signals are generated to fix the ACC gain. This functions as an auto color killer control circuit.  
The UV demodulation result is output as chrominance signals via a low pass filter.

#### 4. Synchronization Block

This is a synchronizing signal processing block.

Chip output synchronizing signals and synchronizing signals for internal use are generated by this block. Various signals are output in this block and the following operation modes can be selected.

1) SYNC threshold level adjustment

2-1) Fine adjustment of HSY signal (start side)

2-2) Fine adjustment of HSY signal (stop side)

3) HSY signal enable select

High Level

Active\*

These signal are used to sync chip and clamp timing to the A/D converter

4) Fine adjustment of HSYNC\_L signal

5-1) Fine adjustment of HVALID signal (start side)

5-2) Fine adjustment of HVALID signal (stop side)

6-1) Fine adjustment of VVALID signal (start side)

6-2) Fine adjustment of VVALID signal (stop side)

The data signals are transmitted or received at the rising edge of the HVALID signal.

7) TV, VTR mode select

TV mode

VTR mode\*

The TV mode outputs a fixed pixel number per one line and absorbs a jitter that does not appear on the TV receiver normally.

The VTR mode outputs the results of decoding in accordance with the HSYNC signal regardless of whether a jitter exists or not.

## 5. Epilogue Block

The Epilogue Block outputs UV signals from the chrominance block and Y signals from the luminance block in the format based on the signal obtained by setting of the control register. In this block, the following modes can be selected.

- 1) Display of blue back when synchronization fails.  
OFF  
ON\*

- 2) Output modes

- 2.1) ITUR 601 mode

Output signal Y/CbCr format select

YCbCr 4 : 2 : 2\*

YCbCr 4 : 1 : 1

The chrominance signal (U, V component) outputs Cb and Cr data to the C pin in an output format described later.

- 2.2) YCbCr 8-bit multiplex output mode

This mode does not include SAV and EAV.

- 3) Selection of 8-bit chroma signal output format

Offset binary\*

2's Complement

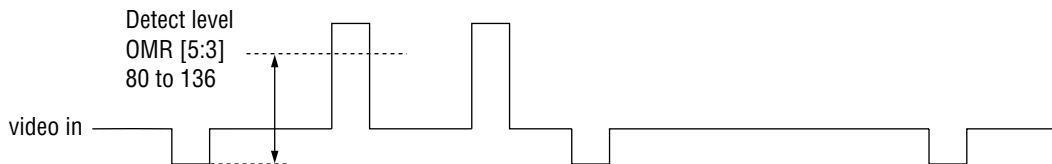
- 4) Output pin enable select

High impedance

Output enable\*

- 5) Multiplex signal detect level adjustment

The levels to detect multiplexed signals sent during the vertical blanking period are configured to be variable. The binary values after input signals are A-to-D converted are employed as the levels to detect multiplexed signals, and the levels are set in eight steps with respect to the SYNC tip level.



- 6) Various modes detection

NTSC/PAL detect mode\*

Multiplex signal detect mode

HSYNC synchronization detect mode

- 7) Output signal phase control

**6. I<sup>2</sup>C Control Block**

This is the serial interface block based on the I<sup>2</sup>C standard of Phillips Corporation.

This block functions only as a Slave-Receiver.

The external control can set the internal registers (MRA, MRB, HSYT, etc.).

**7. Test Control Block**

This block is used to test this LSI. Normally it is not used.



## Register Description

Registers controlled by I<sup>2</sup>C bus are shown below.  
 A register setting value with an "\*" indicates the default.  
 Enter "0" to the undefined register when setting registers.

### Mode Register A (MRA) <default: 0xC0>

|          |                      |       |                        |              |
|----------|----------------------|-------|------------------------|--------------|
| MRA[7]   | NTSC/PAL Auto select | 0:    | Fix                    |              |
|          |                      | *1:   | Auto                   |              |
| MRA[6]   | Synchronization mode | 0:    | TV mode                |              |
|          |                      | *1:   | VTR mode               |              |
| MRA[5]   | Chroma format        | *0:   | Offset binary          |              |
|          |                      | 1:    | 2's Complement         |              |
| MRA[4]   | Override             | *0:   | external terminal mode |              |
|          |                      | 1:    | register mode          |              |
| MRA[3]   | Video Input mode     | *0:   | composite video input  |              |
|          |                      | 1:    | S video input          |              |
| MRA[2:0] | Video Input mode     | *000: | NTSC CCIR601           | 13.5 MHz     |
|          |                      | 001:  | NTSC Square Pixel      | 12.27 MHz    |
|          |                      | 010:  | NTSC 4Fsc              | 14.31818 MHz |
|          |                      | 100:  | PAL CCIR601            | 13.5 MHz     |
|          |                      | 101:  | PAL Square Pixel       | 14.75 MHz    |

### Mode Register B (MRB) <default: 0x18>

|        |                      |     |   |            |
|--------|----------------------|-----|---|------------|
| MRB[7] | Sub Pixel Alignment  | *0: | Sub Pixel Alignment is used.  |            |
|        |                      | 1:  | Sub Pixel Alignment is not used.  |            |
| MRB[6] | Color killer mode    | *0: | Auto color killer (Chrominance signal level becomes "0" when color burst level is below specified value.) |            |
|        |                      | *1: | Forced color killer ON (Chrominance signal level is forced to be "0".)                                    |            |
| MRB[5] | Pixel Sampling Ratio | *0: | (4:2:2)   | 1: (4:1:1) |
| MRB[4] | Blue Back            | 0:  | OFF (Video signal is demodulated and output regardless of synchronization detection .)                    |            |
|        |                      | *1: | AUTO (Blue Back is output when synchronization is not detected.)  |            |

|        |                             |   |
|--------|-----------------------------|---|
| MRB[3] | Sync enable, clamping pulse | 0: HSY outputs "HIGH" level.<br>*1: HSY outputs active.           |
| MRB[2] | Data-pass control           | *0: DECIMETER is used at 2X sampling.<br>1: No DECIMETER is used. |

(Note) This register becomes valid at double-speed clock input(27 MHz).

|          |                     |  |
|----------|---------------------|--|
| MRB[1:0] | Y/C separation mode | *00: Adaptive comb filter (Operation mode is selected monitoring the correlation of 3 lines.)<br>01: Nonadaptive comb filter (Operation mode is always fixed.)<br>10: Comb filter is not used. (Trap filter is used.)<br>11: Undefined |
|----------|---------------------|--|

|                              |                                  |
|------------------------------|----------------------------------|
| (Note) Adaptive comb filter: | 2/3-line comb filter at NTSC     |
| Non-adaptive comb filter:    | Comb filter/trap filter at PAL   |
|                              | 3-line comb filter at NTSC       |
|                              | 2-line cosine comb filter at PAL |

Horizontal Sync Trimmer (HSYT) <default: 0x00>

|           |                             |                                 |
|-----------|-----------------------------|---------------------------------|
| HSYT[7:4] | HSY begin trimmer (8/pixel) | 0xC: -4 (-32) to 0xB: +11 (+88) |
| HSYT[3:0] | HSY stop trimmer (8/pixel)  | 0xC: -4 (-32) to 0xB: +11 (+88) |

Sync Threshold level adjust (STHR) <default: 0x00>

|           |            |                                 |
|-----------|------------|---------------------------------|
| STHR[7:0] | Sync depth | 0x0: -0 to *0x37:55 to 0xFF:255 |
|-----------|------------|---------------------------------|

(Note) The sync signal detect threshold level is adjusted.

Horizontal Sync Delay (HSDL) <default: 0x00>

|           |                                 |                                       |
|-----------|---------------------------------|---------------------------------------|
| HSDL[7:0] | HSYNC_L delay trimmer (4/pixel) | 0x80: -128 (-512) to 0x7F: +127 (508) |
|-----------|---------------------------------|---------------------------------------|

Horizontal Valid Trimmer (HVALT) <default: 0x00>

|            |                                |                    |
|------------|--------------------------------|--------------------|
| HVALT[7:0] | HVALID begin trimmer (1/pixel) | 0x8: -8 to 0x7: +7 |
| HVALT[3:0] | HVALID stop trimmer (1/pixel)  | 0x8: -8 to 0x7: +7 |

Vertical Valid Trimmer (VVALT) <default: 0x00>

VVALT[7:4] VVALID begin trimmer (1/line) 0x8: -8 to 0x7: +7

VVALT[3:0] VVALID stop trimmer (1/line) 0x8: -8 to 0x7: +7

Luminance Control (LUMC) <default: 0x40>

LUMC[7] Output level limiter \*0: OFF 1: ON

(Note) The limit range is from 16 to 235 at limiter ON.

LUMC[6] Use of Pre-filter 0: Prefilter is not used.  
\*1: Prefilter is used.

LUMC[5:4] Aperture bandpass select \*00: middle range  
01:  
10:  
11: high range

LUMC[3:2] Coring range select \*00: coring off  
01: +/-4LSB  
10: +/-5LSB  
11: +/-7LSB

LUMC[1:0] Aperture filter weighting factor  
\*00: 0  
01: 0.25  
10: 0.75  
11: 1.5

AGC/Pedestal Loop filter control (AGCLF) <default: 0x40>

AGCLF[7:6] AGC loop filter time constant  
00: slow  
\*01: medium  
10: fast  
11: fixed

AGCLF[5:0] AGC reference level 0x20: -32 to 0x1F: +31

## Sync separation level (SSEPL) &lt;default: 0x00&gt;

|          |                       |     |  |
|----------|-----------------------|-----|--|
| SSEPL[7] | Pedestal clamp on/off | *0: | Pedestal clamp is not used.                        |
|          |                       | 1:  | Pedestal clamp is used.<br>(AGC will not operate.) |

|            |                       |           |    |           |
|------------|-----------------------|-----------|----|-----------|
| SSEPL[6:0] | Sync separation level | 0x40: -64 | to | 0x3F: +63 |
|------------|-----------------------|-----------|----|-----------|

## Chrominance Control (CHRC) &lt;default: 0x5&gt;

|           |           |
|-----------|-----------|
| CHRC[7:4] | Undefined |
|-----------|-----------|

|           |                        |    |      |    |    |
|-----------|------------------------|----|------|----|----|
| CHRC[7:3] | C-Output level limiter | 0: | *OFF | 1: | ON |
|-----------|------------------------|----|------|----|----|

(Note) The limit range is from 16 to 224 at limiter ON.

|         |                        |    |     |     |    |
|---------|------------------------|----|-----|-----|----|
| CHRC[2] | Chroma bandpass filter | 0: | OFF | *1: | ON |
|---------|------------------------|----|-----|-----|----|

|           |                             |      |                         |
|-----------|-----------------------------|------|-------------------------|
| CHRC[1:0] | Color kill threshold factor | 00:  | 0.5 color burst level   |
|           |                             | *01: | 0.25 color burst level  |
|           |                             | 10:  | 0.125 color burst level |
|           |                             | 11:  | 0 (Color killer off)    |

## ACC Loop filter control (ACCLF) &lt;default: 0x20&gt;

|          |           |
|----------|-----------|
| ACCLF[7] | Undefined |
|----------|-----------|

|            |                               |      |        |
|------------|-------------------------------|------|--------|
| ACCLF[6:5] | ACC loop filter time constant | 00:  | slow   |
|            |                               | *01: | medium |
|            |                               | 10:  | fast   |
|            |                               | 11:  | fixed  |

|            |                     |           |    |           |
|------------|---------------------|-----------|----|-----------|
| ACCLF[4:0] | ACC reference level | 0x10: -16 | to | 0x0F: +15 |
|------------|---------------------|-----------|----|-----------|

## Hue control (HUE) &lt;default: 0x00&gt;

|          |             |                    |    |                     |
|----------|-------------|--------------------|----|---------------------|
| HUE[7:0] | Hue control | 0x80: -180 degrees | to | 0x7F: 178.6 degrees |
|----------|-------------|--------------------|----|---------------------|

Optional Mode Register (OMR) <default: 0x00>

|          |   |  |  |
|----------|---|--|--|
| OMR[7:6] | Undefined                                       |  |  |
| OMR[5:3] | Multiplex signal detection level<br>(VBID etc.) | 00: 80<br>01: 88<br>*10: 96<br>•<br>•<br>11: 136   |  |
| OMR[2]   | Hi-Z on Sleep for Out-pin                       | *0: Active<br>1: Hi-Z  |  |
| OMR[1:0] | Signal Indicate mode                            | *00: NTSC/PAL<br>01: SOUT (Multiplex signal detect)<br>10: HDET (H-Sync detect)<br>11: Undefined |  |

Output phase control for data Y (OPCY) <default: 0x00>

|           |                                 |  |  |
|-----------|---------------------------------|--|--|
| OPCY[7:3] | Undefined                       |  |  |
| OPCY[2]   | YCbCr 8-bit multiplex output    | *0: YCbCr 16-bit output<br>1: YCbCr 8-bit multiplex output           |  |
| OPCY[1:0] | Output phase control for data Y | *00: normal<br>01: forward 1 clock<br>10: Undefined<br>11: Undefined |  |

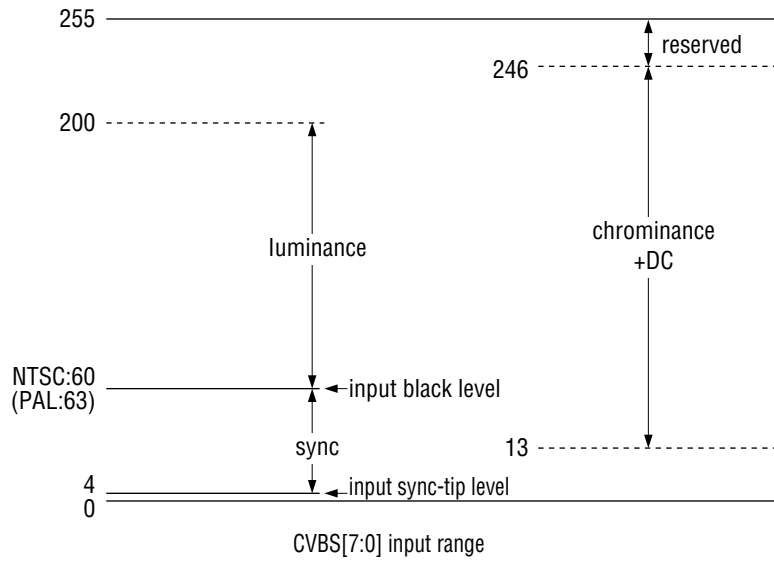
Output phase control for data C (OPCC) <default: 0x00>

|           |                                 |  |  |
|-----------|---------------------------------|--|--|
| OPCC[7:2] | Undefined                       |  |  |
| OPCC[1:0] | Output phase control for data C | *00: normal<br>01: forward 1 clock<br>10: Undefined<br>11: Undefined |  |

## FUNCTIONAL DESCRIPTION

### Input Signal Level

Input signal is 8 bits in a straight binary format.  
The recommended input range is shown below.



**Output format**

The YCbCr 4:2:2 format and 4:1:1 format are shown below.  
 The output format can be changed by register settings.

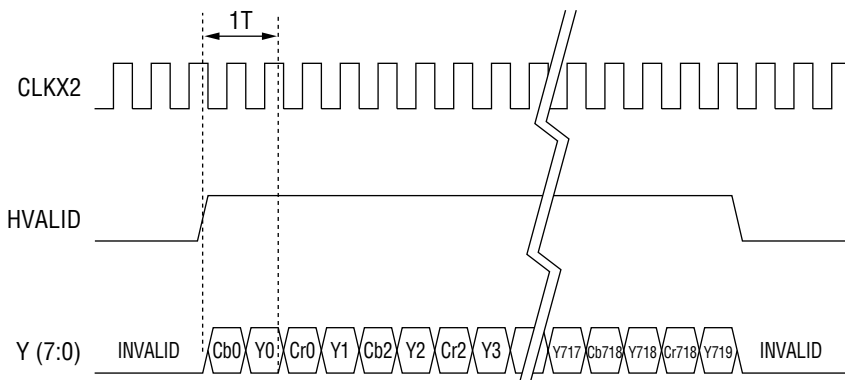
| OUTPUT  | PIXEL BYTE SEQUENCE |     |     |     |     |     |
|---------|---------------------|-----|-----|-----|-----|-----|
| Y7(MSB) | Y7                  | Y7  | Y7  | Y7  | Y7  | Y7  |
| Y6      | Y6                  | Y6  | Y6  | Y6  | Y6  | Y6  |
| Y5      | Y5                  | Y5  | Y5  | Y5  | Y5  | Y5  |
| Y4      | Y4                  | Y4  | Y4  | Y4  | Y4  | Y4  |
| Y3      | Y3                  | Y3  | Y3  | Y3  | Y3  | Y3  |
| Y2      | Y2                  | Y2  | Y2  | Y2  | Y2  | Y2  |
| Y1      | Y1                  | Y1  | Y1  | Y1  | Y1  | Y1  |
| Y0(LSB) | Y0                  | Y0  | Y0  | Y0  | Y0  | Y0  |
| C7(MSB) | Cb7                 | Cr7 | Cb7 | Cr7 | Cb7 | Cr7 |
| C6      | Cb6                 | Cr6 | Cb6 | Cr6 | Cb6 | Cr6 |
| C5      | Cb5                 | Cr5 | Cb5 | Cr5 | Cb5 | Cr5 |
| C4      | Cb4                 | Cr4 | Cb4 | Cr4 | Cb4 | Cr4 |
| C3      | Cb3                 | Cr3 | Cb3 | Cr3 | Cb3 | Cr3 |
| C2      | Cb2                 | Cr2 | Cb2 | Cr2 | Cb2 | Cr2 |
| C1      | Cb1                 | Cr1 | Cb1 | Cr1 | Cb1 | Cr1 |
| C0(LSB) | Cb0                 | Cr0 | Cb0 | Cr0 | Cb0 | Cr0 |
| Y point | 0                   | 1   | 2   | 3   | 4   | 5   |
| C point | 0                   |     | 2   |     | 4   |     |

YCbCr 4:2:2 format

| OUTPUT  | PIXEL BYTE SEQUENCE |     |     |     |     |     |     |     |
|---------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Y7(MSB) | Y7                  | Y7  | Y7  | Y7  | Y7  | Y7  | Y7  | Y7  |
| Y6      | Y6                  | Y6  | Y6  | Y6  | Y6  | Y6  | Y6  | Y6  |
| Y5      | Y5                  | Y5  | Y5  | Y5  | Y5  | Y5  | Y5  | Y5  |
| Y4      | Y4                  | Y4  | Y4  | Y4  | Y4  | Y4  | Y4  | Y4  |
| Y3      | Y3                  | Y3  | Y3  | Y3  | Y3  | Y3  | Y3  | Y3  |
| Y2      | Y2                  | Y2  | Y2  | Y2  | Y2  | Y2  | Y2  | Y2  |
| Y1      | Y1                  | Y1  | Y1  | Y1  | Y1  | Y1  | Y1  | Y1  |
| Y0(LSB) | Y0                  | Y0  | Y0  | Y0  | Y0  | Y0  | Y0  | Y0  |
| C7(MSB) | Cb7                 | Cb5 | Cb3 | Cb1 | Cb7 | Cb5 | Cb3 | Cb1 |
| C6      | Cb6                 | Cb4 | Cb2 | Cb0 | Cb6 | Cb4 | Cb2 | Cb0 |
| C5      | Cr7                 | Cr5 | Cr3 | Cr1 | Cr7 | Cr5 | Cr3 | Cr1 |
| C4      | Cr6                 | Cr4 | Cr2 | Cr0 | Cr6 | Cr4 | Cr2 | Cr0 |
| C3      | 0                   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| C2      | 0                   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| C1      | 0                   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| C0(LSB) | 0                   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Y point | 0                   | 1   | 2   | 3   | 4   | 5   | 6   | 7   |
| C point | 0                   |     |     |     | 4   |     |     |     |

YCbCr 4:1:1 format

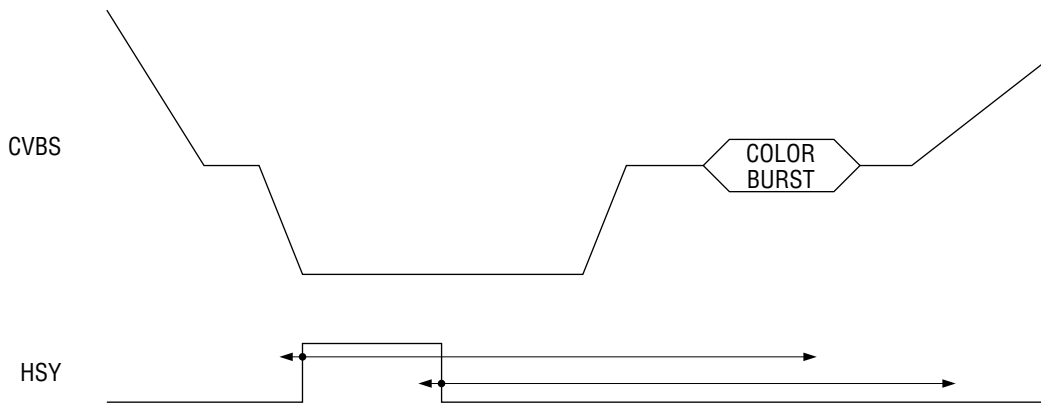
**YCbCr 8-bit multiplex output mode format**



## TIMING DESCRIPTION

### A/D Converter Support Signal

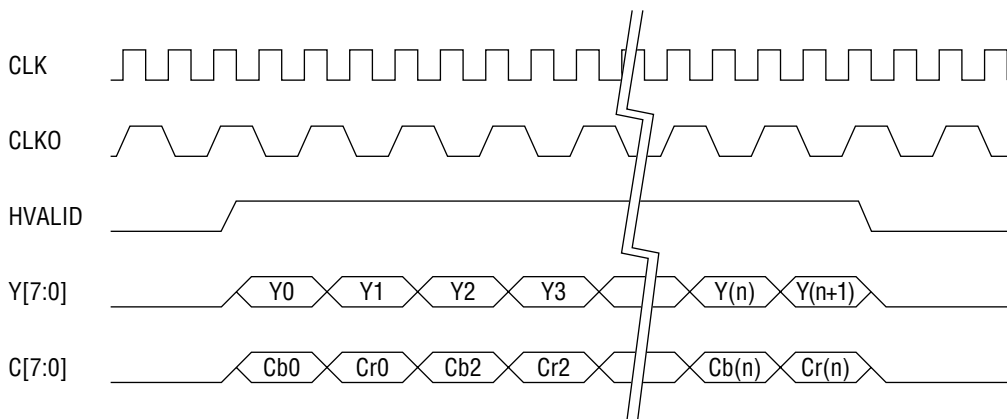
The timing wave form of HSY/HCL signals, which measure the sync chip and clamp timing for the A/D converter, is as follows.



**A/D Converter Support Signal**

### Line control signal

The line control signal timing is as follows.



**Line Control Timing**



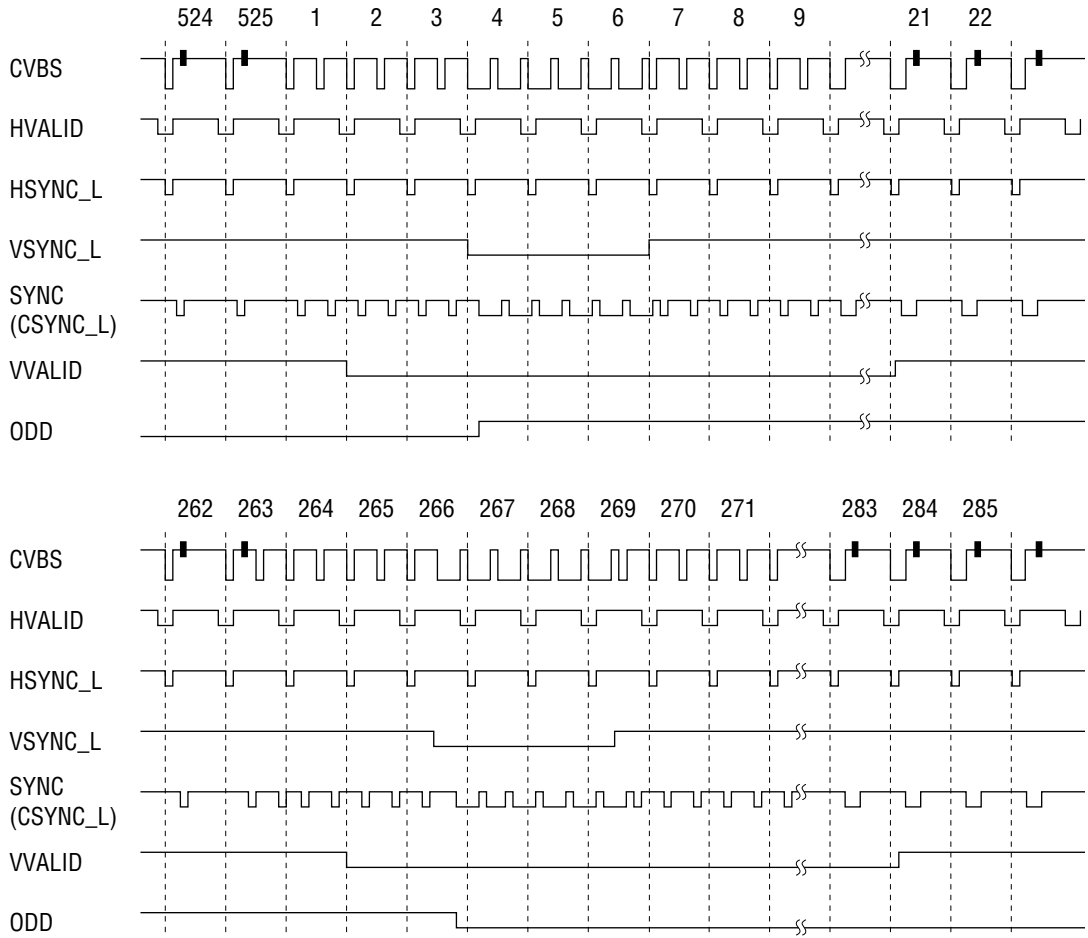
**Total Number of Pixels**

The total number of pixels vary depending on the mode and frequency used, as shown below (default values when typical signals are input).

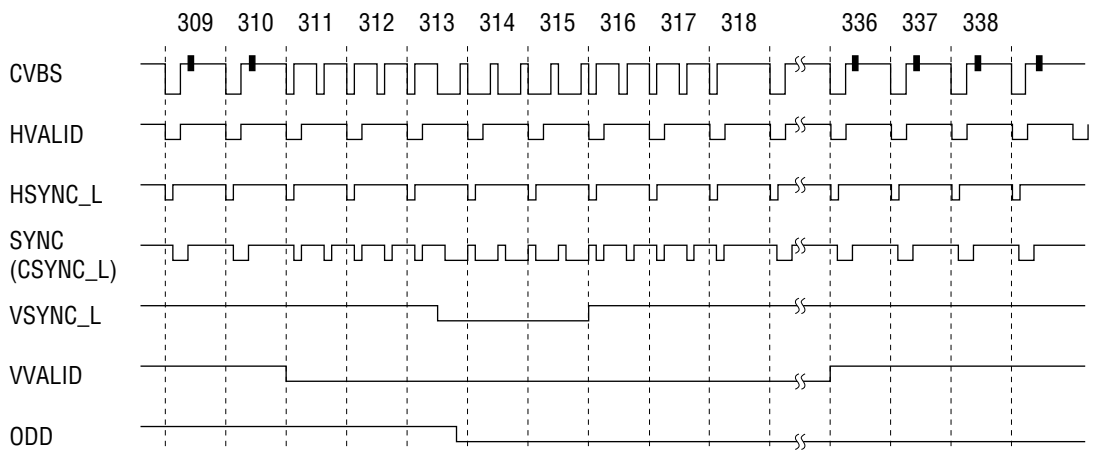
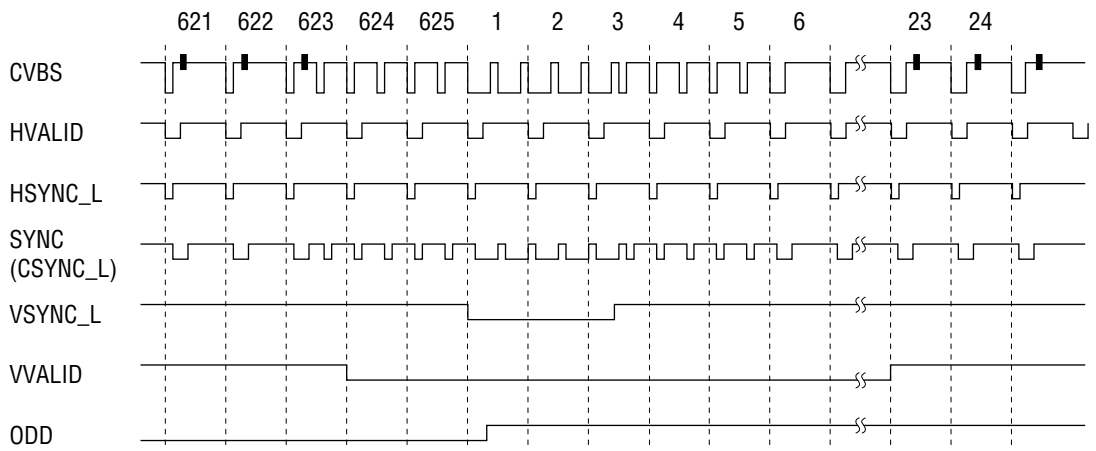
| Video and Sampling Mode |                  | Total<br>Pixels | Active<br>Pixels | HBLK Pixels |                  |       |
|-------------------------|------------------|-----------------|------------------|-------------|------------------|-------|
| Video Mode              | Sampling Rate    |                 |                  | Front-porch | Hsync.Back-porch | Total |
| NTSC                    | 13.5 MHz         | 858             | 720              | 16          | 122              | 138   |
|                         | 12.27 MHz (SQ)   | 780             | 640              | 28          | 112              | 140   |
|                         | 14.32 MHz (4FSC) | 910             | 768              | 8           | 134              | 142   |
|                         | —                |                 |                  |             |                  |       |
| PAL                     | 13.5 MHz         | 864             | 720              | 14          | 130              | 144   |
|                         | 14.75 MHz (SQ)   | 944             | 768              | 34          | 142              | 176   |
|                         | —                |                 |                  |             |                  |       |
|                         | —                |                 |                  |             |                  |       |

### Vertical Synchronizing Signal

The vertical synchronizing signal timing is as follows.



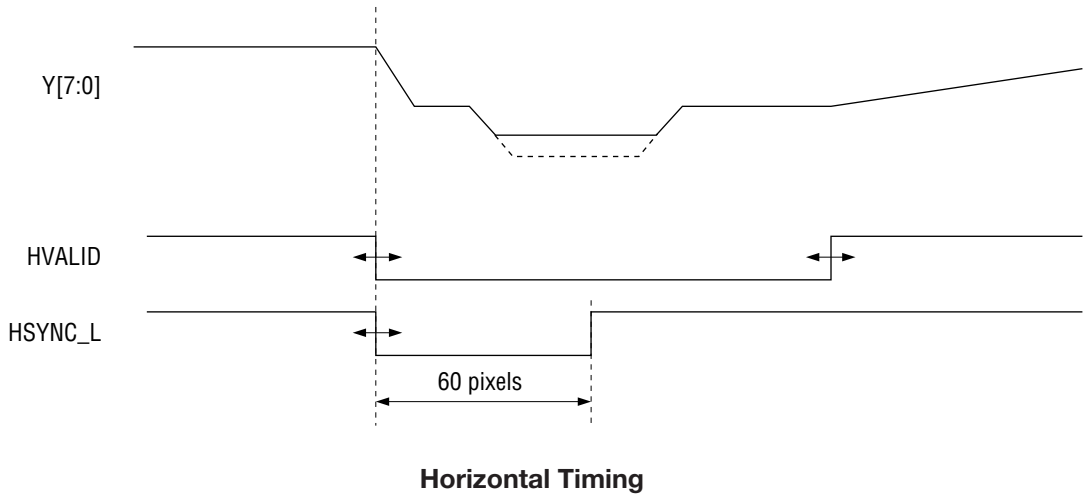
Vertical Synchronizing Signal (NTSC 60 Hz)



Vertical Synchronizing Signal (PAL 50 Hz)

### Horizontal Synchronizing Signal

The horizontal synchronizing signal timing is as follows.



### I<sup>2</sup>C BUS FORMAT

The I<sup>2</sup>C-bus interface input format is shown below.

|   |               |   |            |   |        |   |       |        |   |   |
|---|---------------|---|------------|---|--------|---|-------|--------|---|---|
| S | Slave Address | A | Subaddress | A | Data 0 | A | ..... | Data n | A | P |
|---|---------------|---|------------|---|--------|---|-------|--------|---|---|

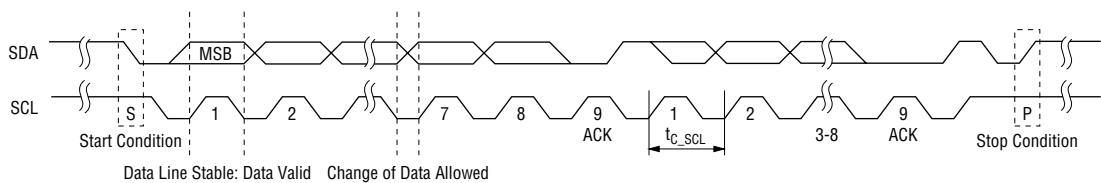
| Symbol        | Description  |
|---------------|--|
| S             | Start condition                                    |
| Slave Address | Slave address 1000001X, 8th bit is write signal.   |
| A             | Acknowledge. Generated by slave                    |
| Subaddress    | Subaddress byte                                    |
| Data n        | Data to write to address designated by subaddress. |
| P             | Stop condition                                     |

As mentioned above, the write operation can be executed from subaddress to subaddress continuously. When the write operation is executed at subaddresses discontinuously, the Acknowledge and Stop condition formats are input repeatedly after Data 0.

If one of the following matters occurs, the decoder will not return "A" (Acknowledge).

- The slave address does not match.
- A non-existent subaddress is specified.
- The write attribute of a register does not match "X" (read/write control bit).

The input timing is shown below.



**I<sup>2</sup>C-bus Basic Input/Output Timing**

## OPERATION MODE SETTING

The video mode includes ;

1. Internal terminal mode to be directly set by a dedicated terminal
2. Register setting mode to be specified by setting the internal registers

These modes can be changed by the mode register MRA [4].

The reset state (default) is the external terminal mode.

The following registers can be set in the external terminal mode.

|            |                   |       |                       |              |
|------------|-------------------|-------|-----------------------|--------------|
| MRA[3]     | input signal mode | *0:   | Composite video input |              |
|            |                   | 1:    | S-video input         |              |
| MRA[2 : 0] | input mode        | *000: | NTSC ITU-R601         | 13.5 MHz     |
|            |                   | 001:  | NTSC Square Pixel     | 12.27 MHz    |
|            |                   | 010:  | MTSC 4Fsc             | 14.31818 MHz |
|            |                   | 100:  | PAL ITU-R601          | 13.5 MHz     |
|            |                   | 101:  | PAL Square Pixel      | 14.75 MHz    |

## OPERATION CLOCK SETTING

The operation clock settings at ITU-R601 are shown below.

| Input clock | Input data | CLKSEL Pin | Register (MRB2)              | Clock for A/D converter    |
|-------------|------------|------------|------------------------------|----------------------------|
| 27.0 MHz    | 27.0 MHz   | "L"        | "0" (decimation filter used) | CLKX20 (27 MHz)            |
| 27.0 MHz    | 13.5 MHz   | "L"        | "1" (Unused)                 | CLKX0 (13.5 MHz)           |
| 13.5 MHz    | 13.5 MHz   | "H"        | "1" (Unused)                 | CLKX20 or CLKX0 (13.5 MHz) |

When the double speed clock is used, data can be input at a double speed or at an ordinary speed by setting the internal register (MRB2) and the clock for the A/D converter.

The internal processing after decimation filter is performed at an ordinary speed.

## INTERNAL REGISTERS

## Register List

| Register Function                        | Subaddress | Data byte |         |         |         |         |         |         |         |
|--|------------|-----------|---------|---------|---------|---------|---------|---------|---------|
|  |            | D7        | D6      | D5      | D4      | D3      | D2      | D1      | D0      |
| Mode Register A (MRA)                    | 0          | MRA7      | MRA6    | MRA5    | MRA4    | MRA3    | MRA2    | MRA1    | MRA0    |
| Mode Register B (MRB)                    | 1          | MRB7      | MRB6    | MRB5    | MRB4    | MRB3    | MRB2    | MRB1    | MRB0    |
| Horizontal Sync Trimmer (HSYT)           | 2          | HSYT7     | HSYT6   | HSYT5   | HSYT4   | HSYT3   | HSYT2   | HSYT1   | HSYT0   |
| Sync Threshold level adjust (STHR)       | 3          | STHR7     | STHR6   | STHR5   | STHR4   | STHR3   | STHR2   | STHR1   | STHR0   |
| Horizontal Sync Delay (HSDL)             | 4          | HSDL7     | HSDL6   | HSDL5   | HSDL4   | HSDL3   | HSDL2   | HSDL1   | HSDL0   |
| Horizontal Valid Trimmer (HVALID)        | 5          | HVALID7   | HVALID6 | HVALID5 | HVALID4 | HVALID3 | HVALID2 | HVALID1 | HVALID0 |
| Vertical Valid Trimmer (VVALID)          | 6          | VVALID7   | VVALID6 | VVALID5 | VVALID4 | VVALID3 | VVALID2 | VVALID1 | VVALID0 |
| Luminance Control (LUMC)                 | 7          | LUMC7     | LUMC6   | LUMC5   | LUMC4   | LUMC3   | LUMC2   | LUMC1   | LUMC0   |
| AGC/Pedestal Loop Filter Control (AGCLF) | 8          | AGCLF7    | AGCLF6  | AGCLF5  | AGCLF4  | AGCLF3  | AGCLF2  | AGCLF1  | AGCLF0  |
| Sync separation level (SSEPL)            | 9          | SSEPL7    | SSEPL6  | SSEPL5  | SSEPL4  | SSEPL3  | SSEPL2  | SSEPL1  | SSEPL0  |
| Chrominance Control (CHRC)               | A          | CHRC7     | CHRC6   | CHRC5   | CHRC4   | CHRC3   | CHRC2   | CHRC1   | CHRC0   |
| ACC Loop Filter Control (ACCLF)          | B          | ACCLF7    | ACCLF6  | ACCLF5  | ACCLF4  | ACCLF3  | ACCLF2  | ACCLF1  | ACCLF0  |
| Hue Control (HUE)                        | C          | HUE7      | HUE6    | HUE5    | HUE4    | HUE3    | HUE2    | HUE1    | HUE0    |
| Optional Mode Register (OMR)             | D          | OMR7      | OMR6    | OMR5    | OMR4    | OMR3    | OMR2    | OMR1    | OMR0    |
| Output Phase Control for Data Y (OPCY)   | E          | OPCY7     | OPCY6   | OPCY5   | OPCY4   | OPCY3   | OPCY2   | OPCY1   | OPCY0   |
| Output Phase Control for Data C (OPCC)   | F          | OPCC7     | OPCC6   | OPCC5   | OPCC4   | OPCC3   | OPCC2   | OPCC1   | OPCC0   |

**Relationship between Register Setting Value and Adjusted Value**

Horizontal Sync Trimmer

Position adjustment of sync chip clamp timing signal

HSYT [7:4] :Adjusting the starting position

|                             |     |     |     |    |   |    |     |     |     |     |     |     |     |     |     |     |
|-----------------------------|-----|-----|-----|----|---|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register Setting Value (0x) | C   | D   | E   | F  | 0 | 1  | 2   | 3   | 4   | 5   | 6   | 7   | 8   | 9   | A   | B   |
| Adjusted Value (Pixel)      | -32 | -24 | -16 | -8 | 0 | +8 | +16 | +24 | +32 | +40 | +48 | +56 | +64 | +72 | +80 | +88 |

HSYT [3:0] :Adjusting the end position

|                             |     |     |     |    |   |    |     |     |     |     |     |     |     |     |     |     |
|-----------------------------|-----|-----|-----|----|---|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register Setting Value (0x) | C   | D   | E   | F  | 0 | 1  | 2   | 3   | 4   | 5   | 6   | 7   | 8   | 9   | A   | B   |
| Adjusted Value (Pixel)      | -32 | -24 | -16 | -8 | 0 | +8 | +16 | +24 | +32 | +40 | +48 | +56 | +64 | +72 | +80 | +88 |

Horizontal Sync Delay

Adjustment of the starting position of horizontal sync signal

HSDL [7:0]

|                |   | MSB[7 : 4] |      |      |      |      |      |      |     |     |      |      |      |      |      |      |      |
|----------------|---|------------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|------|
|                |   | 8          | 9    | A    | B    | C    | D    | E    | F   | 0   | 1    | 2    | 3    | 4    | 5    | 6    | 7    |
| LSB<br>[3 : 0] | 0 | -512       | -448 | -384 | -320 | -256 | -192 | -128 | -64 | 0   | +64  | +128 | +192 | +256 | +320 | +384 | +448 |
|                | 1 | -508       | -444 | -380 | -316 | -252 | -188 | -124 | -60 | +4  | +68  | +132 | +196 | +260 | +324 | +388 | +452 |
|                | 2 | -504       | -440 | -376 | -312 | -248 | -184 | -120 | -56 | +8  | +72  | +136 | +200 | +264 | +328 | +392 | +456 |
|                | 3 | -500       | -436 | -372 | -308 | -244 | -180 | -116 | -52 | +12 | +76  | +140 | +204 | +268 | +332 | +396 | +460 |
|                | 4 | -496       | -432 | -368 | -304 | -240 | -176 | -112 | -48 | +16 | +80  | +144 | +208 | +272 | +336 | +400 | +464 |
|                | 5 | -492       | -428 | -364 | -300 | -236 | -172 | -108 | -44 | +20 | +84  | +148 | +212 | +276 | +340 | +404 | +468 |
|                | 6 | -488       | -424 | -360 | -296 | -232 | -168 | -104 | -40 | +24 | +88  | +152 | +216 | +280 | +344 | +408 | +472 |
|                | 7 | -484       | -420 | -356 | -292 | -228 | -164 | -100 | -36 | +28 | +92  | +156 | +220 | +284 | +348 | +412 | +476 |
|                | 8 | -480       | -416 | -352 | -288 | -224 | -160 | -96  | -32 | +32 | +96  | +160 | +224 | +288 | +352 | +416 | +480 |
|                | 9 | -476       | -412 | -348 | -284 | -220 | -156 | -92  | -28 | +36 | +100 | +164 | +228 | +292 | +356 | +420 | +484 |
|                | A | -472       | -408 | -344 | -280 | -216 | -152 | -88  | -24 | +40 | +104 | +168 | +232 | +296 | +360 | +424 | +488 |
|                | B | -468       | -404 | -340 | -276 | -212 | -148 | -84  | -20 | +44 | +108 | +172 | +236 | +300 | +364 | +428 | +492 |
|                | C | -464       | -400 | -336 | -272 | -208 | -144 | -80  | -16 | +48 | +112 | +176 | +240 | +304 | +368 | +432 | +496 |
|                | D | -460       | -396 | -332 | -268 | -204 | -140 | -76  | -12 | +52 | +116 | +180 | +244 | +308 | +372 | +436 | +500 |
|                | E | -456       | -392 | -328 | -264 | -200 | -136 | -72  | -8  | +56 | +120 | +184 | +248 | +312 | +376 | +440 | +504 |
|                | F | -452       | -388 | -324 | -260 | -196 | -132 | -68  | -4  | +60 | +124 | +188 | +252 | +316 | +380 | +444 | +508 |



Horizontal Valid Trimmer

Position adjustment of horizontal valid pixel timing signal

HVALT [7:4] :Adjusting the starting position

|                             |    |    |    |    |    |    |    |    |   |    |    |    |    |    |    |    |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8  | 9  | A  | B  | C  | D  | E  | F  | 0 | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
| Adjusted Value (Pixel)      | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

HVALT [3:0] :Adjusting the end position

|                             |    |    |    |    |    |    |    |    |   |    |    |    |    |    |    |    |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8  | 9  | A  | B  | C  | D  | E  | F  | 0 | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
| Adjusted Value (Pixel)      | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

Vertical Valid Trimmer

Position adjustment of vertical valid line timing signal

VVALT [7:4] :Adjusting the starting position

|                             |    |    |    |    |    |    |    |    |   |    |    |    |    |    |    |    |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8  | 9  | A  | B  | C  | D  | E  | F  | 0 | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
| Adjusted Value (Line)       | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

VVALT [3:0] :Adjusting the end position

|                             |    |    |    |    |    |    |    |    |   |    |    |    |    |    |    |    |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8  | 9  | A  | B  | C  | D  | E  | F  | 0 | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
| Adjusted Value (Line)       | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

AGC Loop filter control

AGCLF [5:0] :Adjusting sync level

| Register Setting Value (0x) | MSB [5 : 4] |     |     |     |     |
|-----------------------------|-------------|-----|-----|-----|-----|
|                             | 2           | 3   | 0   | 1   |     |
| LSB [3 : 0]                 | 0           | -32 | -16 | 0   | +16 |
|                             | 1           | -31 | -15 | +1  | +17 |
|                             | 2           | -30 | -14 | +2  | +18 |
|                             | 3           | -29 | -13 | +3  | +19 |
|                             | 4           | -28 | -12 | +4  | +20 |
|                             | 5           | -27 | -11 | +5  | +21 |
|                             | 6           | -26 | -10 | +6  | +22 |
|                             | 7           | -25 | -9  | +7  | +23 |
|                             | 8           | -24 | -8  | +8  | +24 |
|                             | 9           | -23 | -7  | +9  | +25 |
|                             | A           | -22 | -6  | +10 | +26 |
|                             | B           | -21 | -5  | +11 | +27 |
|                             | C           | -20 | -4  | +12 | +28 |
|                             | D           | -19 | -3  | +13 | +29 |
|                             | E           | -18 | -2  | +14 | +30 |
|                             | F           | -17 | -1  | +15 | +31 |

Sync separation level

SSEPL [6:0] :Adjusting the blanking level

| Register Setting Value (0x) |   | MSB [6 : 4] |     |     |     |     |     |     |     |
|-----------------------------|---|-------------|-----|-----|-----|-----|-----|-----|-----|
|                             |   | 4           | 5   | 6   | 7   | 0   | 1   | 2   | 3   |
| LSB<br>[3 : 0]              | 0 | -64         | -48 | -32 | -16 | 0   | +16 | +32 | +48 |
|                             | 1 | -63         | -47 | -31 | -15 | +1  | +17 | +33 | +49 |
|                             | 2 | -62         | -46 | -30 | -14 | +2  | +18 | +34 | +50 |
|                             | 3 | -61         | -45 | -29 | -13 | +3  | +19 | +35 | +51 |
|                             | 4 | -60         | -44 | -28 | -12 | +4  | +20 | +36 | +52 |
|                             | 5 | -59         | -43 | -27 | -11 | +5  | +21 | +37 | +53 |
|                             | 6 | -58         | -42 | -26 | -10 | +6  | +22 | +38 | +54 |
|                             | 7 | -57         | -41 | -25 | -9  | +7  | +23 | +39 | +55 |
|                             | 8 | -56         | -40 | -24 | -8  | +8  | +24 | +40 | +56 |
|                             | 9 | -55         | -39 | -23 | -7  | +9  | +25 | +41 | +57 |
|                             | A | -54         | -38 | -22 | -6  | +10 | +26 | +42 | +58 |
|                             | B | -53         | -37 | -21 | -5  | +11 | +27 | +43 | +59 |
|                             | C | -52         | -36 | -20 | -4  | +12 | +28 | +44 | +60 |
|                             | D | -51         | -35 | -19 | -3  | +13 | +29 | +45 | +61 |
|                             | E | -50         | -34 | -18 | -2  | +14 | +30 | +46 | +62 |
|                             | F | -49         | -33 | -17 | -1  | +15 | +31 | +47 | +63 |

ACC Loop filter control

ACCLF [4:0] :Adjusting the color burst level

| Register Setting Value (0x) |   | MSB [4] |     |
|-----------------------------|---|---------|-----|
|                             |   | 1       | 0   |
| LSB<br>[3 : 0]              | 0 | -16     | 0   |
|                             | 1 | -15     | +1  |
|                             | 2 | -14     | +2  |
|                             | 3 | -13     | +3  |
|                             | 4 | -12     | +4  |
|                             | 5 | -11     | +5  |
|                             | 6 | -10     | +6  |
|                             | 7 | -9      | +7  |
|                             | 8 | -8      | +8  |
|                             | 9 | -7      | +9  |
|                             | A | -6      | +10 |
|                             | B | -5      | +11 |
|                             | C | -4      | +12 |
|                             | D | -3      | +13 |
|                             | E | -2      | +14 |
|                             | F | -1      | +15 |

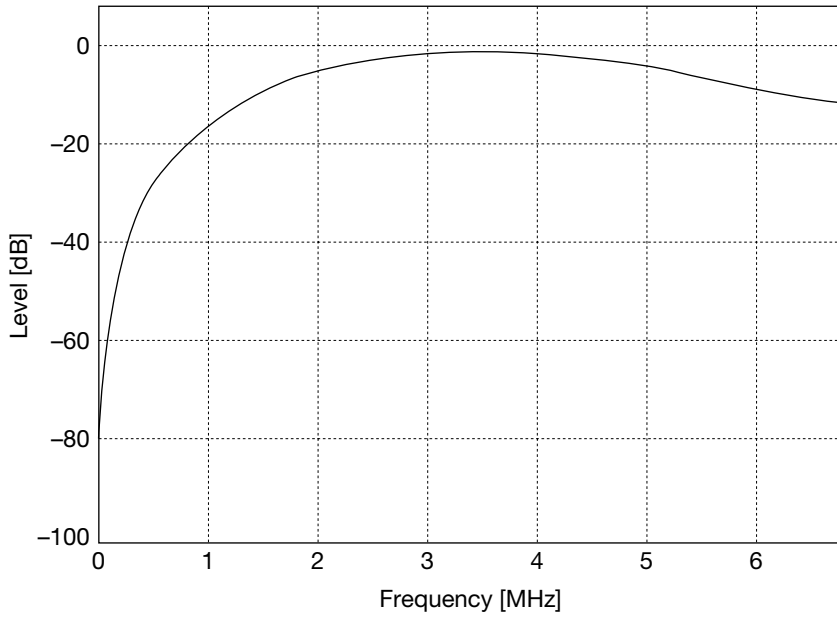
Hue control  
Adjustment of color subcarrier phase

HUE [7:0]

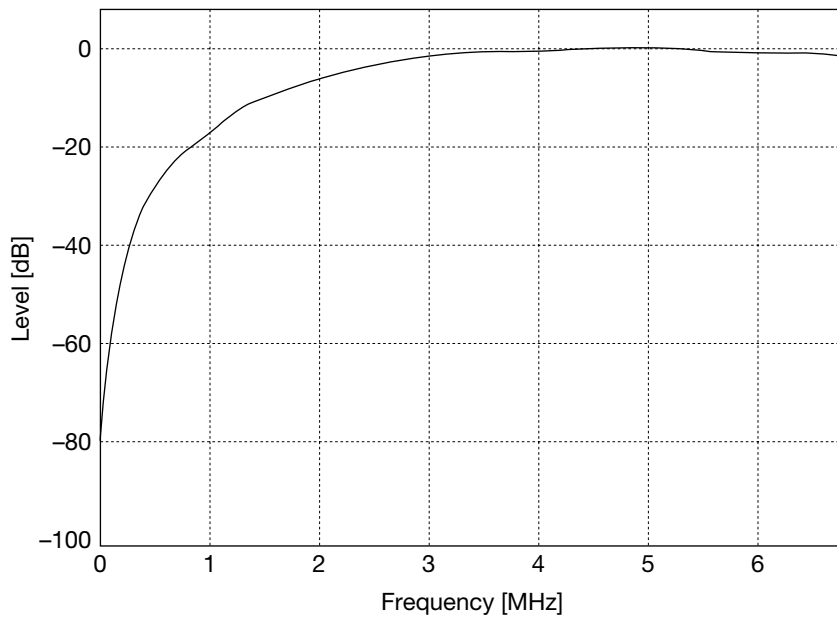
| Register Setting Value (0x) | MSB [7 : 4] |        |        |        |        |       |       |       |       |       |       |       |       |        |        |        |        |
|-----------------------------|-------------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|
|                             | 8           | 9      | A      | B      | C      | D     | E     | F     | 0     | 1     | 2     | 3     | 4     | 5      | 6      | 7      |        |
| LSB [3 : 0]                 | 0           | -180.0 | -157.5 | -135.0 | -112.5 | -90.0 | -67.5 | -45.0 | -22.5 | +0.0  | +22.5 | +45.0 | +67.5 | +90.0  | +112.5 | +135.0 | +157.5 |
|                             | 1           | -178.6 | -156.1 | -133.6 | -111.1 | -88.6 | -66.1 | -43.6 | -21.1 | +1.4  | +23.9 | +46.4 | +68.9 | +91.4  | +113.9 | +136.4 | +158.9 |
|                             | 2           | -177.2 | -154.7 | -132.2 | -109.7 | -87.2 | -64.7 | -42.2 | -19.7 | +2.8  | +25.3 | +47.8 | +70.3 | +92.8  | +115.3 | +137.8 | +160.3 |
|                             | 3           | -175.8 | -153.3 | -130.8 | -108.3 | -85.8 | -63.3 | -40.8 | -18.3 | +4.2  | +26.7 | +49.2 | +71.7 | +94.2  | +116.7 | +139.2 | +161.7 |
|                             | 4           | -174.4 | -151.9 | -129.4 | -106.9 | -84.4 | -61.9 | -39.4 | -16.9 | +5.6  | +28.1 | +50.6 | +73.1 | +95.6  | +118.1 | +140.6 | +163.1 |
|                             | 5           | -173.0 | -150.5 | -128.0 | -105.5 | -83.0 | -60.5 | -38.0 | -15.5 | +7.0  | +29.5 | +52.0 | +74.5 | +97.0  | +119.5 | +142.0 | +164.5 |
|                             | 6           | -171.6 | -149.1 | -126.6 | -104.1 | -81.6 | -59.1 | -36.6 | -14.1 | +8.4  | +30.9 | +53.4 | +75.9 | +98.4  | +120.9 | +143.4 | +165.9 |
|                             | 7           | -170.2 | -147.7 | -125.2 | -102.7 | -80.2 | -57.7 | -35.2 | -12.7 | +9.8  | +32.3 | +54.8 | +77.3 | +99.8  | +122.3 | +144.8 | +167.3 |
|                             | 8           | -168.8 | -146.3 | -123.8 | -101.3 | -78.8 | -56.3 | -33.8 | -11.3 | +11.3 | +33.8 | +56.3 | +78.8 | +101.3 | +123.8 | +146.3 | +168.8 |
|                             | 9           | -167.3 | -144.8 | -122.3 | -99.8  | -77.3 | -54.8 | -32.3 | -9.8  | +12.7 | +35.2 | +57.7 | +80.2 | +102.7 | +125.2 | +147.7 | +170.2 |
|                             | A           | -165.9 | -143.4 | -120.9 | -98.4  | -75.9 | -53.4 | -30.9 | -8.4  | +14.1 | +36.6 | +59.1 | +81.6 | +104.1 | +126.6 | +149.1 | +171.6 |
|                             | B           | -164.5 | -142.0 | -119.5 | -97.0  | -74.5 | -52.0 | -29.5 | -7.0  | +15.5 | +38.0 | +60.5 | +83.0 | +105.5 | +128.0 | +150.5 | +173.0 |
|                             | C           | -163.1 | -140.6 | -118.1 | -95.6  | -73.1 | -50.6 | -28.1 | -5.6  | +16.9 | +39.4 | +61.9 | +84.4 | +106.9 | +129.4 | +151.9 | +174.4 |
|                             | D           | -161.7 | -139.2 | -116.7 | -94.2  | -71.7 | -49.2 | -26.7 | -4.2  | +18.3 | +40.8 | +63.3 | +85.8 | +108.3 | +130.8 | +153.3 | +175.8 |
|                             | E           | -160.3 | -137.8 | -115.3 | -92.8  | -70.3 | -47.8 | -25.3 | -2.8  | +19.7 | +42.2 | +64.7 | +87.2 | +109.7 | +132.2 | +154.7 | +177.2 |
|                             | F           | -158.9 | -136.4 | -113.9 | -91.4  | -68.9 | -46.4 | -23.9 | -1.4  | +21.1 | +43.6 | +66.1 | +88.6 | +111.1 | +133.6 | +156.1 | +178.6 |

Filter Characteristics

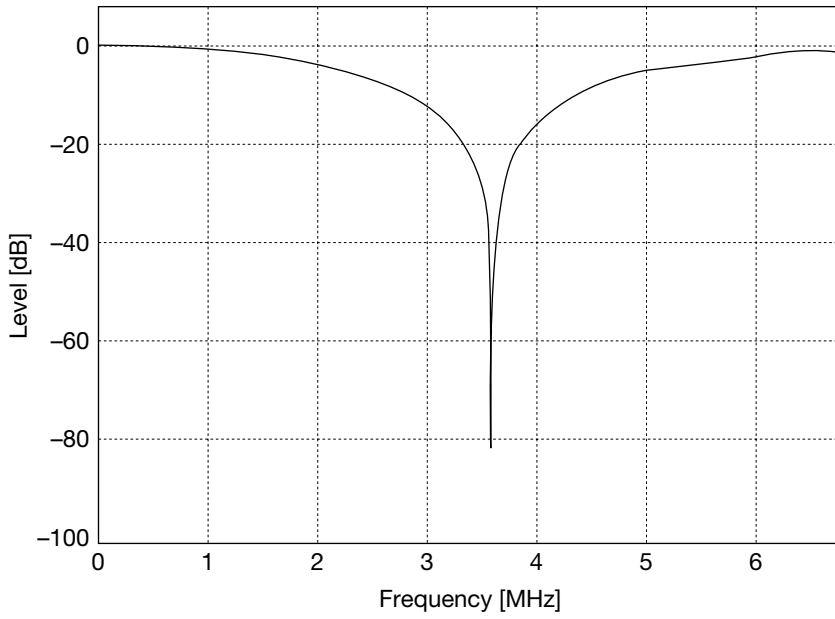
Band Pass Filter (NTSC ITU-R601)



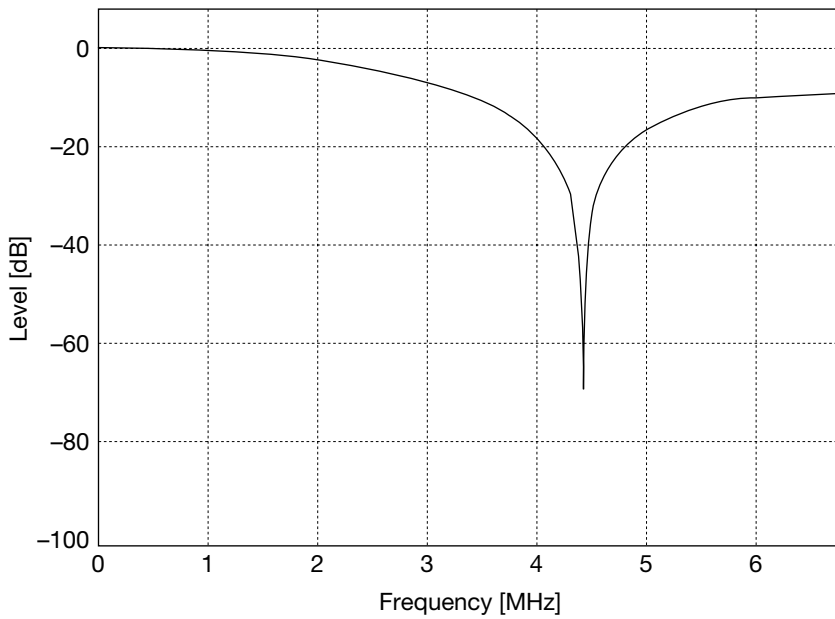
Band Pass Filter (PAL ITU-R601)



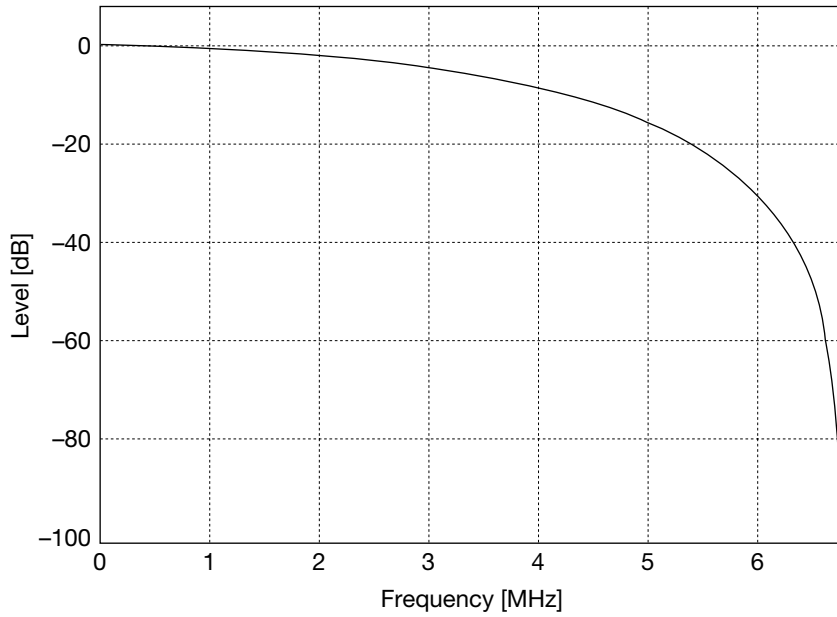
Trap Filter (NTSC ITU-R601)



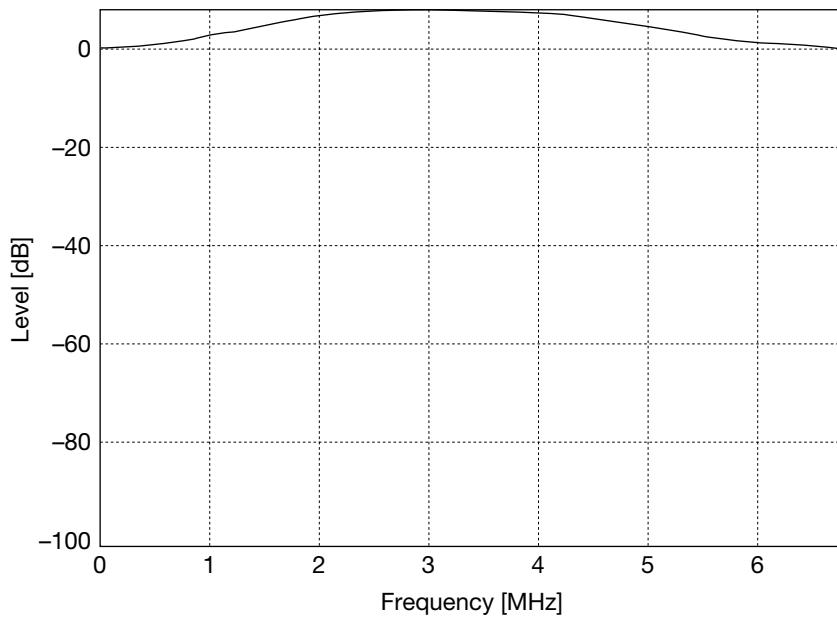
Trap Filter (PAL ITU-R601)

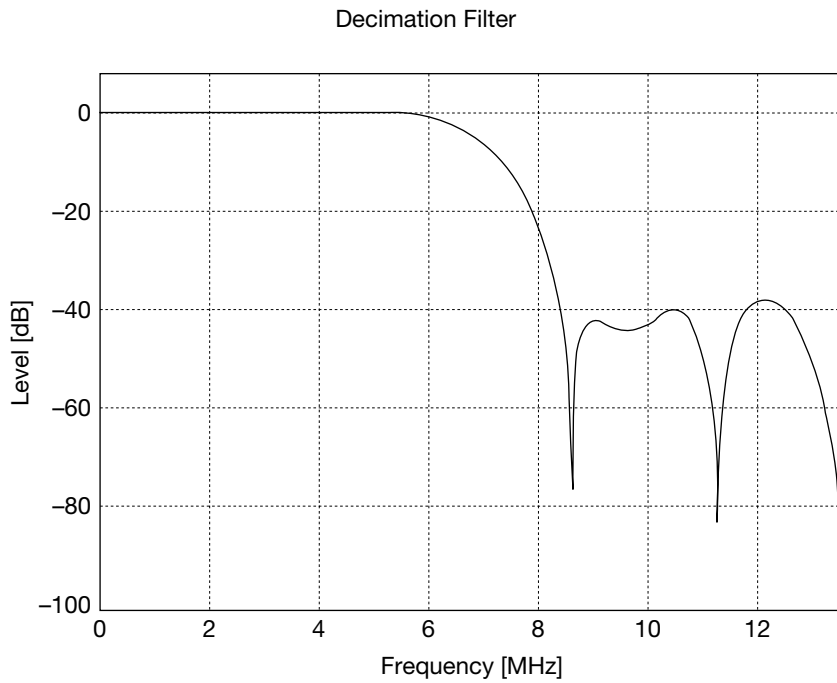


Pre Filter



Sharp Filter





\* The characteristics of the various filters shown above are based on design data.

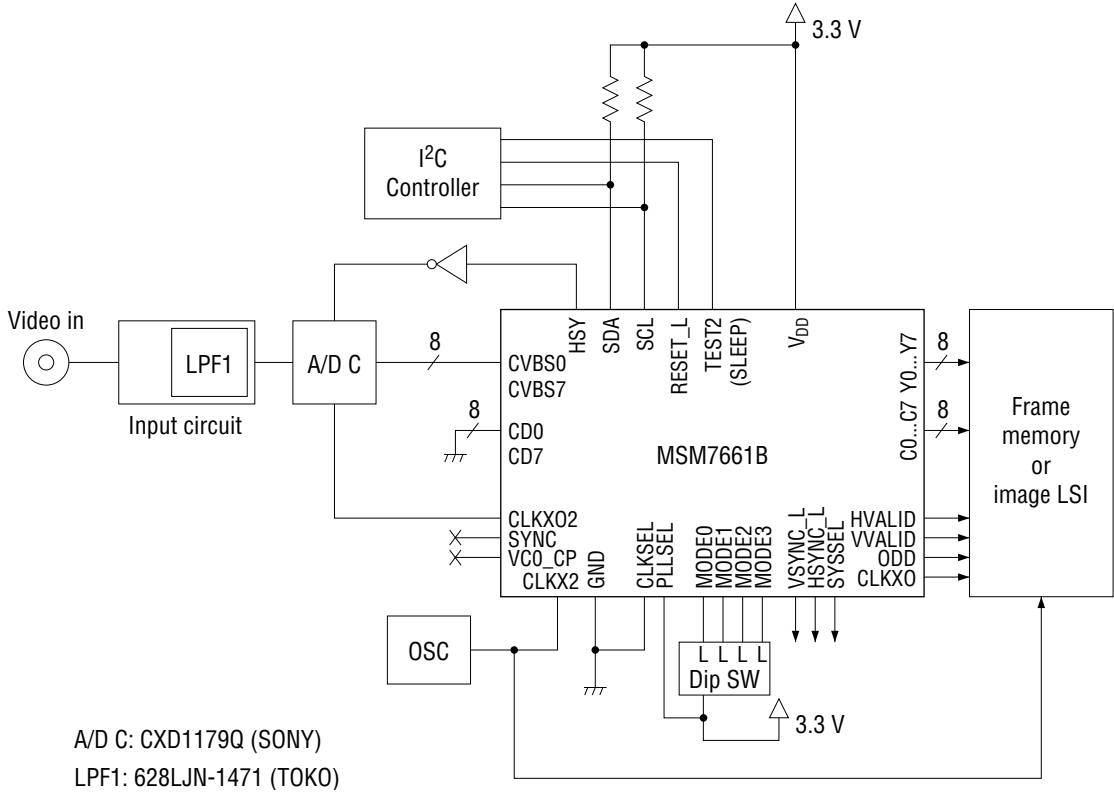
**BASIC APPLICATION CIRCUIT EXAMPLE**

**Application 1**

Mode setting

Video signal: NTSC-composite

CLKX2: 27 MHz

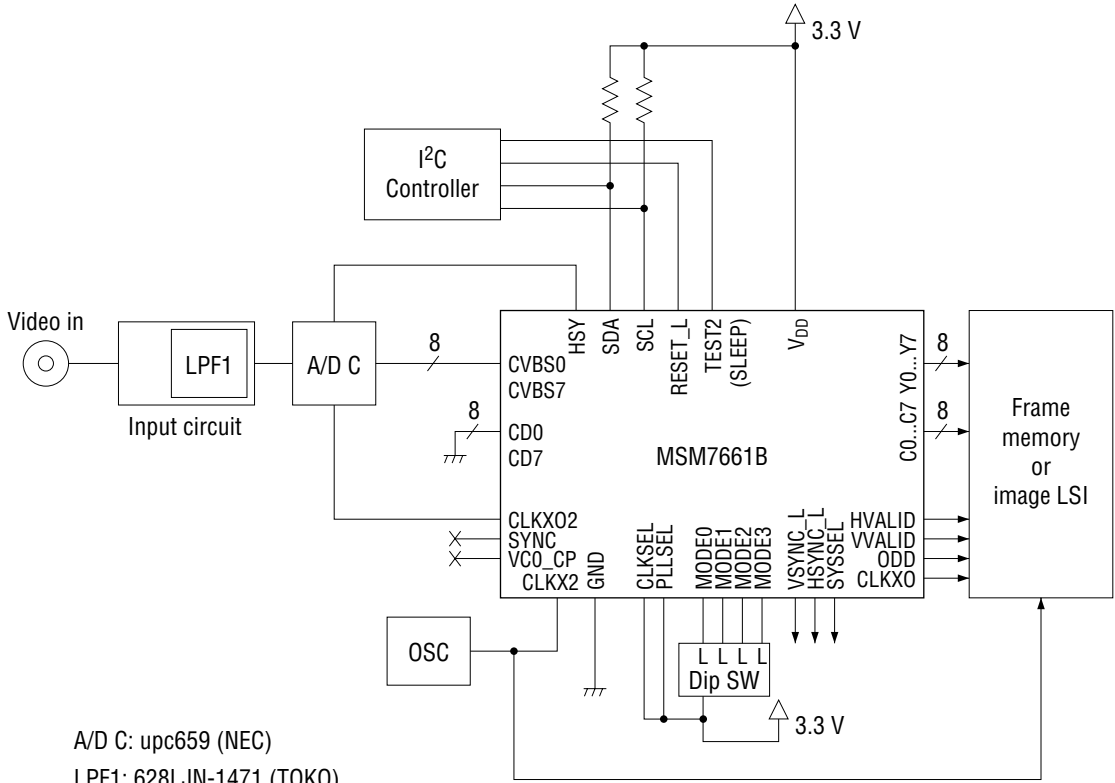




**Application 2**

Mode setting

Video signal: NTSC-composite  
 CLKX2: 13.5 MHz

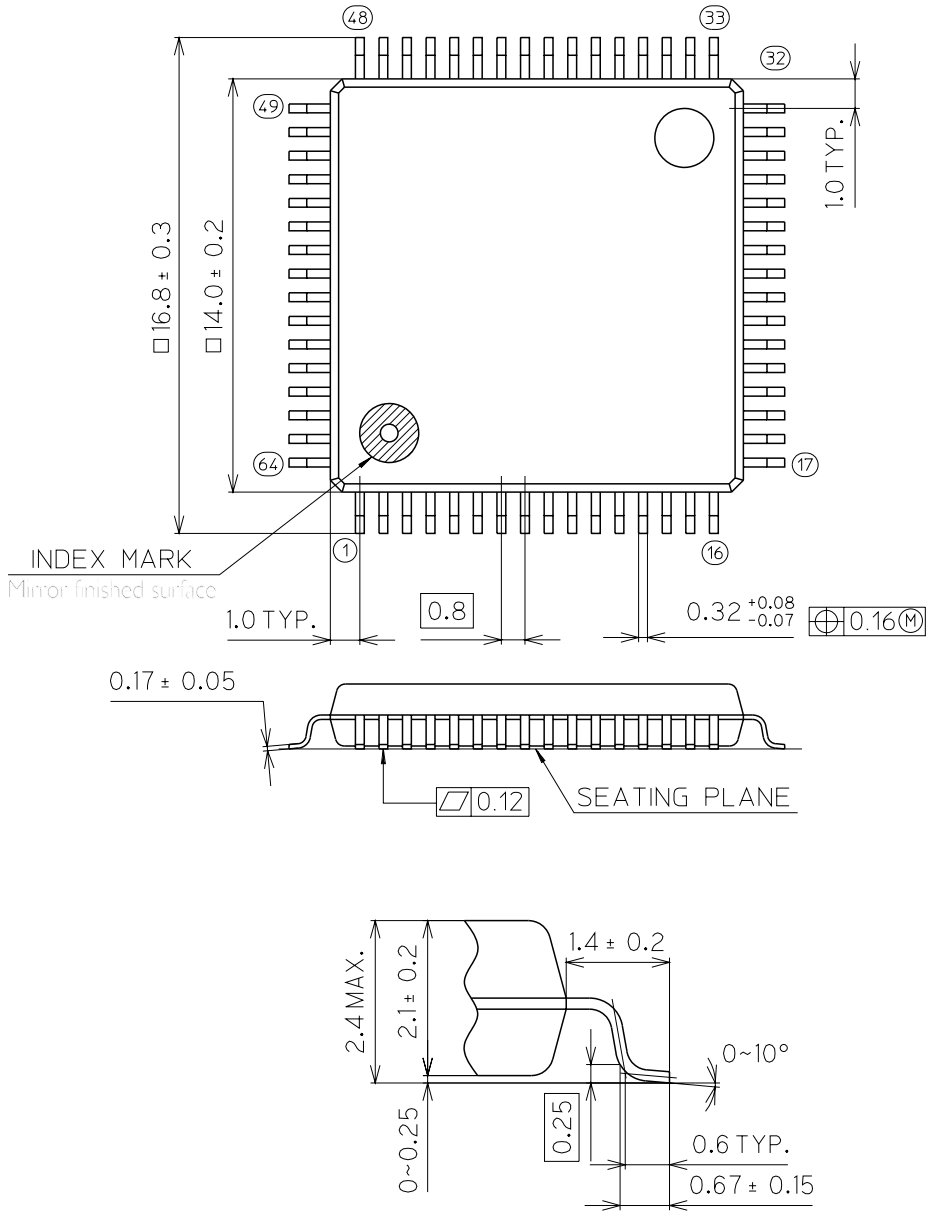


A/D C: upc659 (NEC)

LPF1: 628LJN-1471 (TOKO)

PACKAGE OUTLINES AND DIMENSIONS

(Unit : mm)



64-Pin Plastic QFP