ISO-9001 CERTIFIED BY DSCC

20 AMP, 200 VOLT MOSFET SMART POWER 3-PHASE MOTOR DRIVE HYBRID

4422

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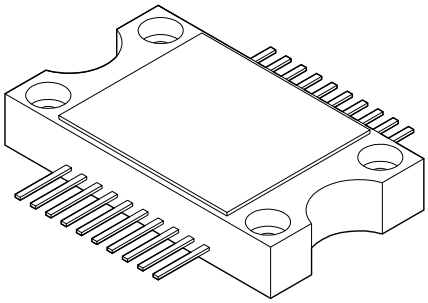
FEATURES:

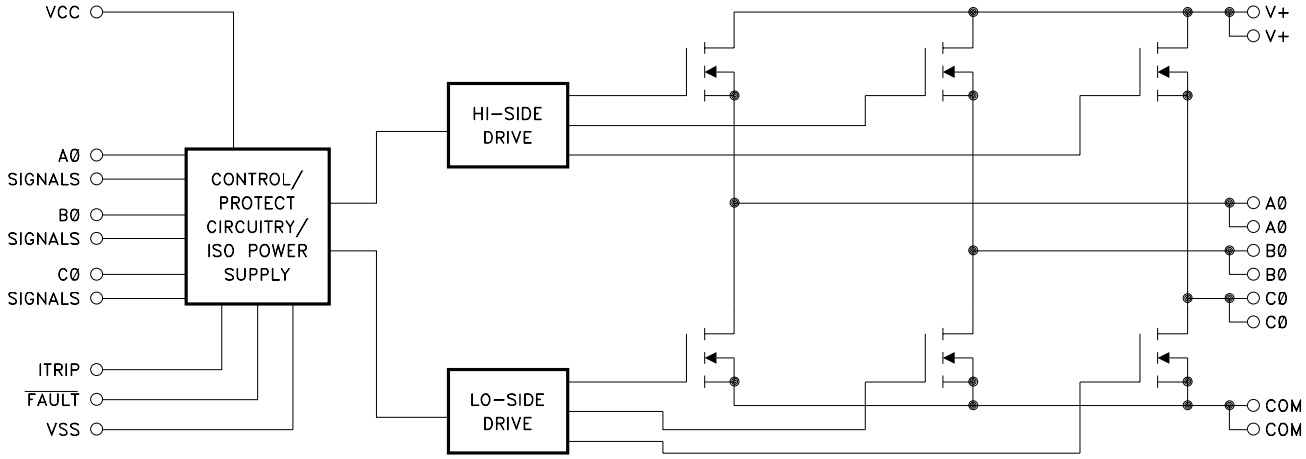
- 200V, 20 Amp Capability
- Self-Contained, Smart Lowside/Highside Drive Circuitry
- Under-Voltage Lockout, Internal 2μS Deadtime
- Capable of Switching Frequencies to 25KHz
- Isolated Case Allows Direct Heat Sinking
- Case Bolt-down Design Allows Superior Heat Dissipation



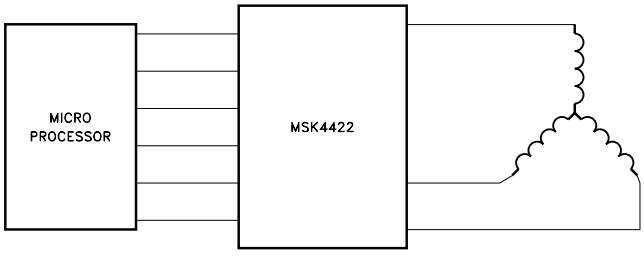
DESCRIPTION:

The MSK 4422 is a 20 Amp, 3 Phase Bridge Smart Power Motor Drive Hybrid with a 200 volt rating on the output switches. The output switches are power MOSFETs with intrinsic fast-recovery diodes for the free-wheeling currents of motor drives. This new smart power motor drive hybrid is compatible with 5V CMOS or TTL logic levels. The internal circuitry prevents simultaneous turn-on of the in-line half bridge transistors with a built-in 2μS deadtime to prevent shoot-through. Undervoltage lockout shuts down the bridge when the supply voltage gets to a point of incomplete turn-on of the output switches. The internal high-side boot strap power supply derived from the +15 volt supply completely eliminates the need for 3 floating independent power supplies for the high-side drive. Current sense circuitry is provided to sense current from an external resistor to shut down the bridge for overcurrent.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS



3 PHASE SIX STEP DC BRUSHLESS MOTOR DRIVE OR 3 PHASE SINUSOIDAL INDUCTION MOTOR DRIVE

PIN-OUT INFORMATION

1	VCC	20	AØ
2	$\overline{\text{AØHIN}}$	19	$\overline{\text{AØ}}$
3	$\overline{\text{BØHIN}}$	18	V+
4	$\overline{\text{CØHIN}}$	17	V+
5	$\overline{\text{AØLIN}}$	16	BØ
6	$\overline{\text{BØLIN}}$	15	$\overline{\text{BØ}}$
7	$\overline{\text{CØLIN}}$	14	CØ
8	$\overline{\text{FAULT}}$	13	$\overline{\text{CØ}}$
9	VSS	12	COM
10	ITRIP	11	COM

Rev. B 4/05

ABSOLUTE MAXIMUM RATINGS

V+ High Voltage Supply 200V
VCC Logic Supply 18V
IOUT Continuous Output Current 20A
IPK Peak Output Current 44A
θJC Thermal Resistance
(Output Switches)
(Junction to Case @ 125°C) . . . . . 2.3°C/W

TsT Storage Temperature Range . . . -55° to +125°C
TLD Lead Temperature Range
(10 Seconds) . . . . . 300°C
TC Case Operating Temperature
MSK 4422 . . . . . -40°C to +85°C
TJ Junction Temperature . . . . . +150°C

ELECTRICAL SPECIFICATIONS

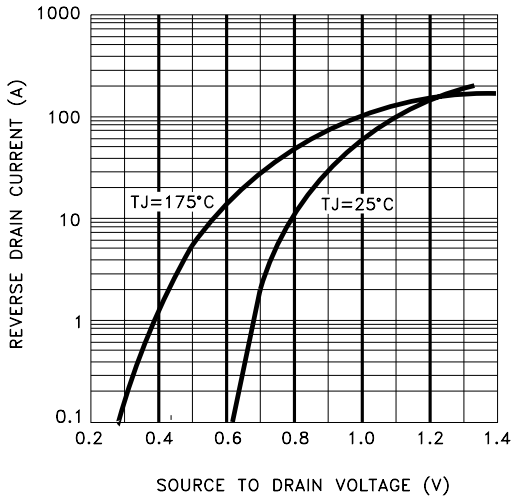
Parameters	Test Conditions ②	MSK 4422 Min.	MSK 4422 Typ.	MSK 4422 Max.	UNITS
OUTPUT CHARACTERISTICS					
VDS(ON) (Each Transistor) ③	ID = 20A	-	1.3	1.7	V
Instantaneous Forward Voltage (Intrinsic Diode) ③	Is = 20A	-	1.2	1.5	V
Reverse Recovery Time ①		-	-	330	nS
Leakage Current	V+ = 200V	-	3	250	μA
	V+ = 160V	-	-	-	μA
	V+ = 200V	-	-	-	μA
BIAS SUPPLY CHARACTERISTICS					
Quiescent Bias Current	Vcc = 15V (non-switching)	-	3	10	mA
		-	-	-	mA
		-	-	-	mA
INPUT SIGNAL CHARACTERISTICS					
Positive Trigger Threshold Voltage	Vcc = 15V	2.2	-	-	V
Negative Trigger Threshold Voltage	Vcc = 15V	-	-	0.8	V
I. Trip Threshold Voltage	Vcc = 15V	400	500	600	mV
SWITCHING CHARACTERISTICS ①	V+ = 100V, Vcc = 15V, ID = 20A				
Upper Drive:					
Turn-On Propagation Delay		-	0.98	-	μS
Turn-Off Propagation Delay		-	2.4	-	μS
Turn-On		-	330	-	nS
Turn-Off		-	440	-	nS
Lower Drive:					
Turn-On Propagation Delay		-	0.9	-	μS
Turn-Off Propagation Delay		-	2.0	-	μS
Turn-On		-	140	-	nS
Turn-Off		-	215	-	nS
Dead Time ①		-	2	-	μS
Minimum Pulse Width ①		300	-	-	nS

NOTES:

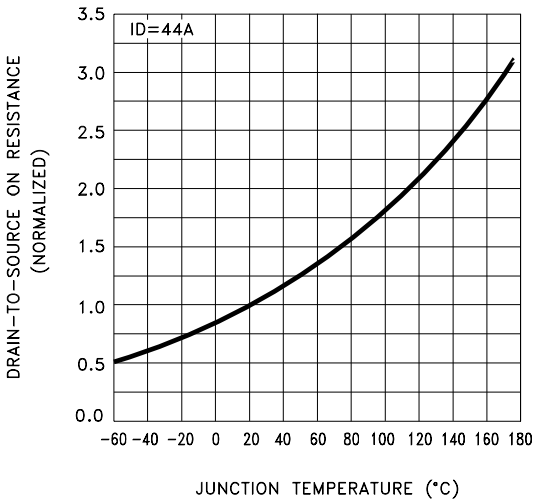
① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Vcc = +15V, ITRIP = 0V, V+ = 200V and Tcase = 25°C unless otherwise specified.
③ Measured using a 300μS pulse with a 2% duty cycle.
④ ON resistance is specified for the internal MOSFET for thermal calculations only. It does not include the package pin resistance.

TYPICAL PERFORMANCE CURVES

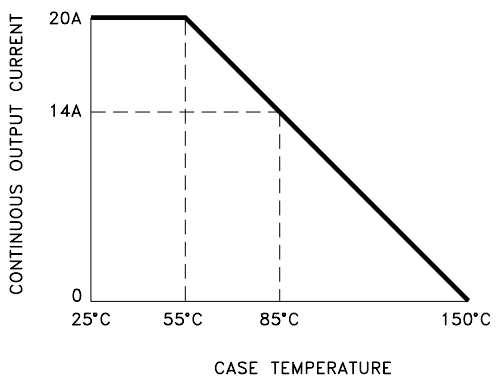
SOURCE TO DRAIN VOLTAGE
vs REVERSE DRAIN CURRENT



NORMALIZED ON−RESISTANCE vs TEMPERATURE



SAFE OPERATING AREA



APPLICATION NOTES

MSK 4422 PIN DESCRIPTION

VCC - Is the low voltage supply for all the internal logic and drivers. A 0.1 μF ceramic capacitor in parallel with a 10μF tantalum capacitor is recommended bypassing for the VCC-VSS pins.

VSS - Is the low voltage supply return pin and the input logic return reference. All logic input and logic output is referenced to this pin. This pin can vary ±5V from the COM power return pin without affecting any of the logic functions.

$\overline{\text{AØHIN}}$, $\overline{\text{BØHIN}}$, $\overline{\text{CØHIN}}$ - Are low active logic inputs for signalling the corresponding phase high-side switch to turn on. The input levels are 5V **CMOS** or **TTL** compatible.

$\overline{\text{AØLIN}}$, $\overline{\text{BØLIN}}$, $\overline{\text{CØLIN}}$ - Are low active inputs for signalling the corresponding phase low-side switch to turn on. The input levels are 5V **CMOS** or **TTL** compatible.

$\overline{\text{FAULT}}$ - Is an open drain logic output pin that gets enabled any time the **VCC** level goes below the cutoff point, or an overcurrent condition occurs. Bringing **VCC** back to normal levels will reset **$\overline{\text{FAULT}}$**. Removing the overcurrent condition and allowing the low-side logic inputs to remain high(off) for 10μS will restore operation.

ITRIP - Is an analog input pin for sensing current flowing from the **COM** pin through a sense resistor to the high power ground. A 0.5 volt level at this pin with respect to **VSS** will signal an overcurrent condition, enable the **$\overline{\text{FAULT}}$** pin and shut down all output switching. Bringing the voltage below this point (100 mV hysteresis) will remove the **$\overline{\text{FAULT}}$** output and leaving the low-side logic inputs simultaneously high (de-activated) for 10μS will restore normal operation.

V+ - Is the high voltage positive rail for the bridge. Proper bypassing to **VSS** with sufficient capacitance to suppress any voltage transients and to ensure removing any drooping during switching, should be done as close to the pins on the hybrid as possible.

COM - Is the return side of the bridge. A sense resistor can be connected between this point and **VSS**, which is the high voltage negative rail. **COM** can float above and below the **VSS** pin up to 5 volts and proper operation will be maintained. Precautions should be taken so as to not allow this voltage to get over ±5 volts under any conditions.

AØ, BØ, CØ - Are the pins connecting the 3 phase bridge switch outputs.

PROTECTION

- All logic inputs use a 300nS filter. A pulse width below this will get ignored.

- **VCC** voltage below the cutoff level of 8.65 volts will reset all switch outputs off and ignore subsequent logic inputs until **VCC** is restored.

- Undervoltage lockout of the internal drivers for the high-side switches also occurs at 8.65 volts, but will not flag with the **$\overline{\text{FAULT}}$** output. This may occur if the high-side output gets switched without switching the low-side. The internal boot strap powersupply for the high-side switch will sag too low for adequate switching. The boot strap supply depends on PWMing of the low-side switches for proper operation.

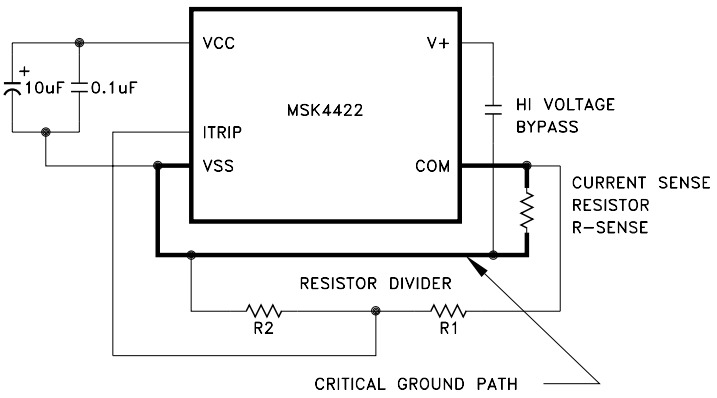
- Switching a low-side logic input while the corresponding phase high-side logic input is activated will turn off both switches. The opposite condition is also true. This is cross-conduction lockout and will occur any time low and high-side inputs for a phase are activated at the same time.

- A 2μS deadtime is automatically inserted between high and low-side output switching to allow complete turn-off of each switch so no overlap will occur.

- An overcurrent condition detected by the **ITRIP** pin will shut down all output switches until the overcurrent condition is removed and all three low-side logic inputs are held high for 10μS, then normal operation will resume.

- **ITRIP** has a 100nS leading edge blanking time after switching to ignore any switching current transients.

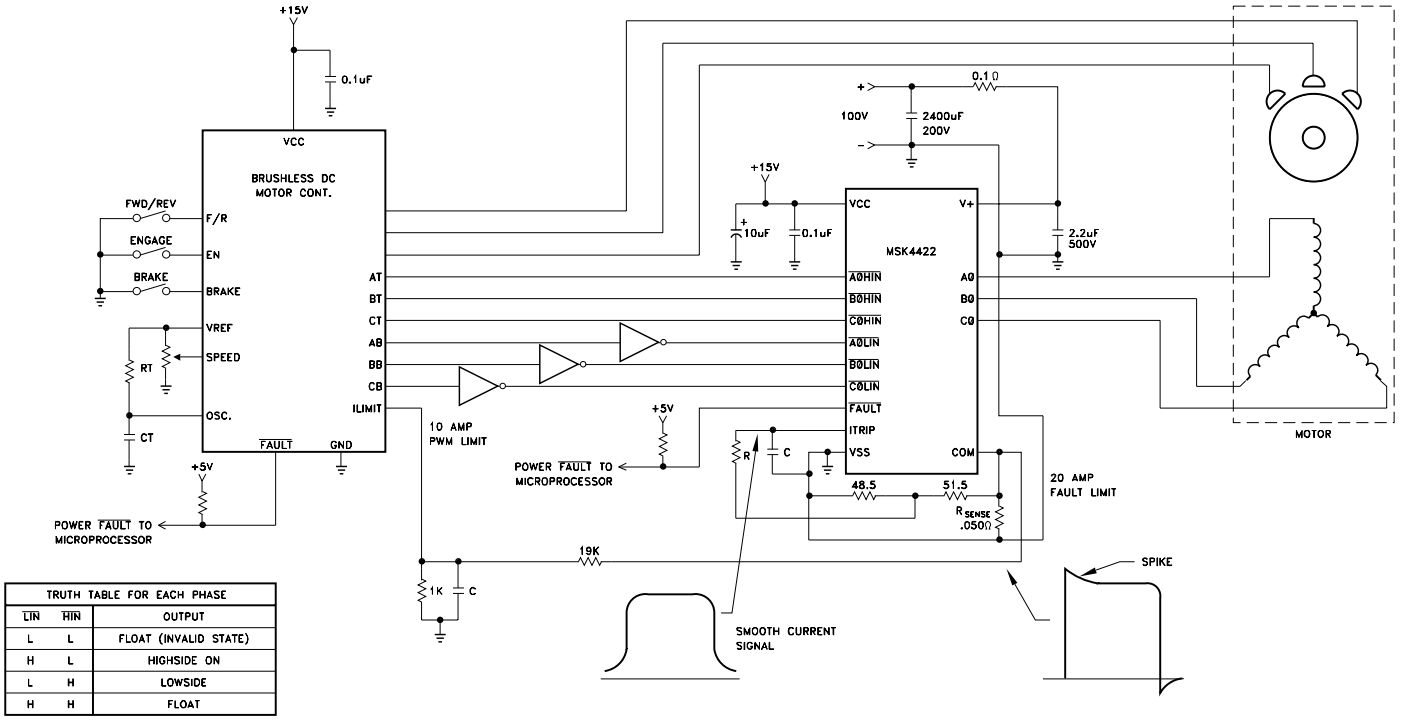
TYPICAL OPERATION



EXAMPLE:
FOR 20 AMP LIMIT:
R-SENSE = 0.050 OHMS
R-SENSE VOLT = 1 VOLT
R1 = 51.5 OHMS
R2 = 48.5 OHMS

FIGURE 1. GROUNDING, BYPASSING, CURRENT SENSE

TYPICAL SYSTEM OPERATION



TRUTH TABLE FOR EACH PHASE		
$\overline{LIN}$	$\overline{HIN}$	OUTPUT
L	L	FLOAT (INVALID STATE)
H	L	HIGHSIDE ON
L	H	LOWSIDE
H	H	FLOAT

The MSK 4422 is designed to be used with a +100 volt high voltage bus, +15 volt low power bus and +5 volt logic signals. Proper derating should be applied when designing the MSK 4422 into a system. High frequency layout techniques with ground planes on a printed circuit board is the only method that should be used for circuit construction. This will prevent pulse jitter caused by excessive noise pickup on the current sense signal or the error amp signal.

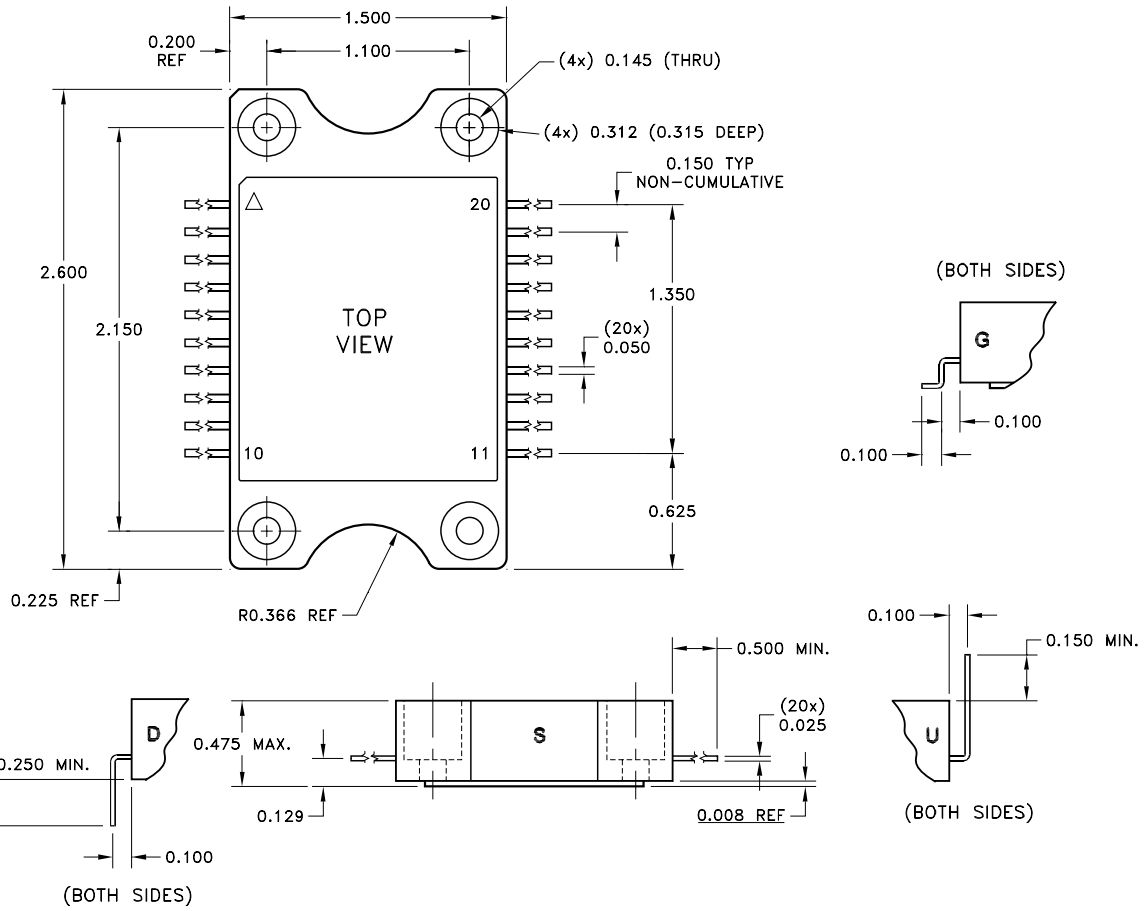
Ground planes for the low power circuitry and high power circuitry should be kept separate. The connection between the bottom of the current sense resistor, VSS pin and the high power ground are connected at this point. This is a critical path and high currents should not be flowing between the current sense and VSS. Inductance in this path should be kept to a minimum. An RC filter (shown in 2 places) will filter out the current spikes and keep the detected noise for those circuits down to a minimum.

In the system shown, two types of current limit are implemented. The first limit is a PWM pulse by pulse limit controlled by the motor controller. A second absolute maximum limit is set up for the MSK 4422 which will completely shut off the bridge in the event that current limit is exceeded.

When controlling the motor speed by the PWM method, it is required that the low side switches be PWM pulsed due to the bootstrap power supplies used to power the high side switch drives. The higher the PWM speed the higher the current load on the drive supply. PWM of the low side will prevent sagging of the high side bootstrap supplies.

The logic signals coming from the typical motor controller IC are set up for driving N channel low side and P channel high side switches directly and are usually 15 volt levels. Provision should be made for getting 5 volt logic signals to the MSK 4422 of the correct assertion levels. Typically, the low side signals out of the controller are high active and the high side are low active. Inverters are shown in the system schematic for the low side controller output.

MECHANICAL SPECIFICATIONS



Weight = 31 Grams Typical
ESD Triangle Indicates Pin 1

All dimensions are ±0.01 inches unless otherwise specified.

ORDERING INFORMATION

Part Number	Screening Level	Lead Configuration
MSK4422S	Industrial	Straight
MSK4422D	Industrial	Down
MSK4422U	Industrial	Up
MSK4422G	Industrial	Gull Wing

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