OKI semiconductor

MSC23436B-xxBS10/DS10

4,194,304 Word By 36-Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC23436B-xxBS10/DS10 is a fully decoded, 4,194,304 word X 36 bit CMOS dynamic random access memory composed of eight 16MbDRAMs (4Mx4) in SOJ and two 8Mb DRAMs(4Mx2) in SOJ. The mounting of ten DRAMs together with decoupling capacitors on a 72-pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required.

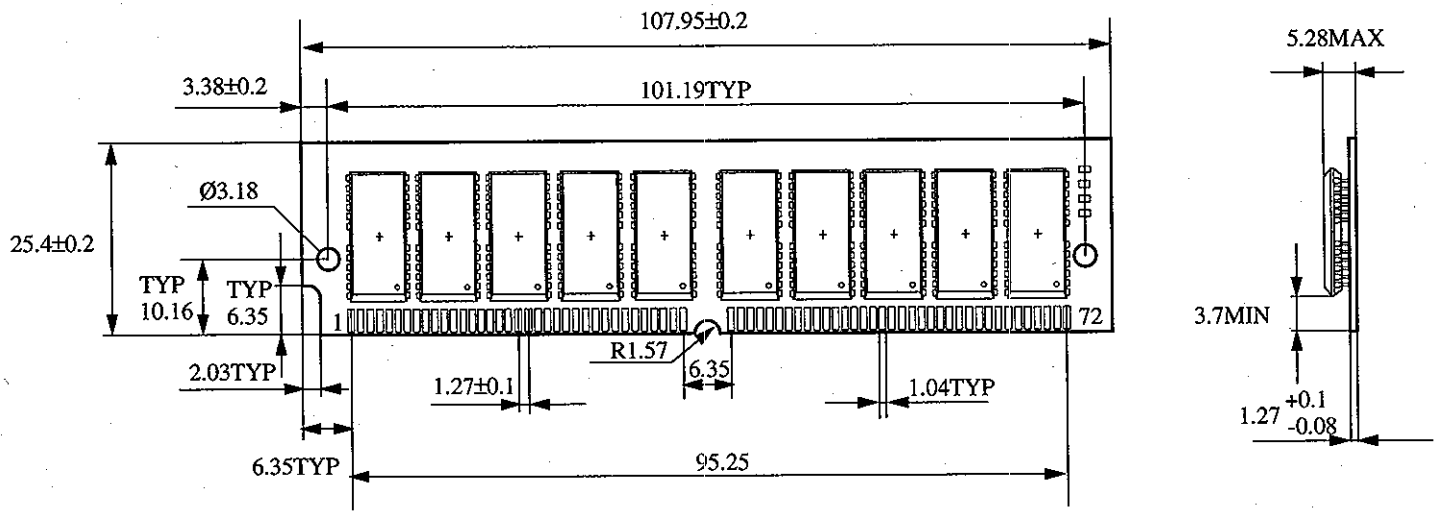
FEATURES

- 4,194,304 word x 36 bit Parity organization
- 72-Pin Socket Insertable Module
  MSC23436B-xxBS10 : Gold tab
  MSC23436B-xxDS10 : Solder tab
- Single +5V supply ± 10% tolerance
- Input : TTL compatible
- Output : TTL compatible,tristate,nonlach
- Refresh : 2048 cycles/32 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability

PRODUCT FAMILY

FAMILY	ACCESS TIME (MAX)			Cycle Time	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	(MAX)	Operating (MAX)	Standby (Max)
MSC23436B-60BS10/DS10	60ns	30ns	15ns	110ns	5720mW	55mW
MSC23436B-70BS10/DS10	70ns	35ns	20ns	130ns	5226mW	

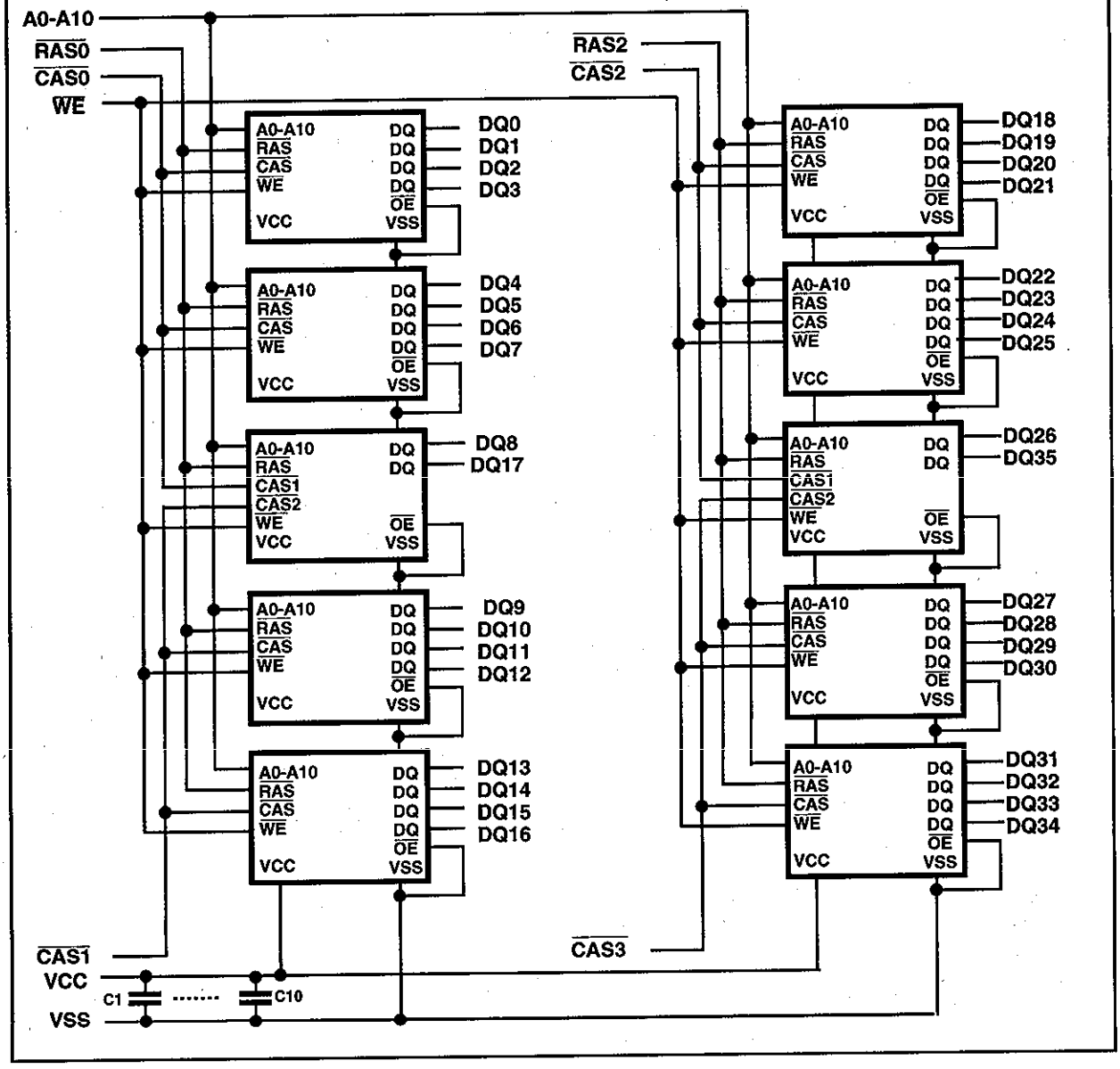
MSC23436B-xxBS10/DS10



*1 The common size difference of the board width 12.5mm of its height is specified as ±0.2. The value above 12.5mm is specified as ±0.5.

FUNCTIONAL BLOCK DIAGRAM

MSC23436B-xxBS10/DS10



PIN CONFIGURATION

MSC23436B-xxBS10/DS10

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	Vss	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	Vcc
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

PRESENCE DETECT PINS

Pin No.	Pin name	-60	-70
67	PD1	Vss	Vss
68	PD2	NC	NC
69	PD3	NC	Vss
70	PD4	NC	NC

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 1.0 ~ +7.0	V
Voltage Vcc supply relative to Vss	V_{CC}	- 1.0 ~+7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	10	W
Operating temperature	T_{OPR}	-0 ~ +70	°C
Storage temperature	T_{STG}	- 40 ~+ 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted within the limits as specified in this data sheet. Exposure to absolute maximum rating conditions for extended period may affect device reliabity.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYPE	MAX	UNIT	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0 °C ~ +70 °C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	-	6.5	V	
Input low voltage	V_{IL}	-1.0	-	0.8	V	

CAPACITANCE

Parameter	Symbol	Type	MAX	Unit
Input Capacitance(A0-A10)	C_{IN1}	-	62	pF
Input Capacitance($\overline{WE}$)	C_{IN2}	-	80	pF
Input Capacitance($\overline{RAS0}$,$\overline{RAS2}$)	C_{IN3}	-	43	pF
Input Capacitance($\overline{CAS0}$-$\overline{CAS3}$)	C_{IN4}	-	28	pF
I/O Capacitance(DQ0-35)	CDQ	-	16	pF

NOTE: Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

(Vcc = 5V ± 10%, Ta = 0~+70℃)

Parameter	Symbol	Condition	MSC23436B-60BS10/DS10		MSC23436B-70BS10/DS10		Unit	Note
			Min	Max	Min	Max		
Input Leakage Current	I_{LI}	$0V \le V_{in} \le 6.5V$: All other pins not under test = 0V	-100	100	-100	100	μA	
Output Leakage Current	I_{LO}	Data out is disable $0V \le V_{out} \le 5.5V$	-10	10	-10	10	μA	
Output High Voltage	V_{OH}	I_{OH} = -5.0mA	2.4	Vcc	2.4	Vcc	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	-	0.4	-	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$ cycling t_{RC} = min	-	1040	-	950	mA	1,2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} TTL	-	20	-	20	mA	
		$\overline{CAS}$ = V_{IH} MOS	-	10	-	10	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = VIH, t_{RC} = min	-	1040	-	950	mA	1,2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC} = min	-	1040	-	950	mA	1
Average power supply current (Fast page)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	-	920	-	830	mA	1,3

NOTE:
1. Icc is dependent on output loading and cycles rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC CHARACTERISTIC

(Vcc = 5V±10%, Ta = 0 ~70 ℃)

NOTE 1,2,3,9,10

Parameter	Symbol	MSC23436B-60BS10/DS10		MSC23436B-70BS10/DS10		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Random read or write cycle time	tRC	110	-	130	-	ns	
Fast page mode cycle time	tPC	40	-	45	-	ns	
Access time from $\overline{RAS}$	tRAC	-	60	-	70	ns	4,5
Access time from $\overline{CAS}$	tCAC	-	15	-	20	ns	4,5
Access time from column address	tAA	-	30	-	35	ns	4,6
Access time from $\overline{CAS}$ precharge	tCPA	-	35	-	40	ns	4
$\overline{CAS}$ to output in Low-Z	tCLZ	0	-	0	-	ns	4
Output buffer turn-off delay	tOFF	0	15	0	20	ns	7
Transition time	tT	3	50	3	50	ns	3
Refresh period	tREF	-	32	-	32	ms	
$\overline{RAS}$ precharge time	tRP	40	-	50	-	ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	tRASP	60	100K	70	100K	ns	
$\overline{RAS}$ hold time	tRSH	15	-	20	-	ns	
$\overline{CAS}$ precharge time	tCP	10	-	10	-	ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	ns	
$\overline{CAS}$ hold time	tCSH	60	-	70	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5	-	5	-	ns	5
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	ns	6
Row address set-up time	tASR	0	-	0	-	ns	
Row address hold time	tRAH	10	-	10	-	ns	
Column address set-up time	tASC	0	-	0	-	ns	
Column address hold time	tCAH	15	-	15	-	ns	
Column address to $\overline{RAS}$ lead time	tRAL	30	-	35	-	ns	

AC CHARACTERISTICS (Continued)
(Vcc = 5V±10%, Ta = 0 ~70 ℃)

Parameter	Symbol	MSC23436B-60BS10/DS10		MSC23436B-70BS10/DS10		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Read command set-up time	tRCS	0	-	0	-	ns	
Read command hold time	tRCH	0	-	0	-	ns	8
Read command hold time reference to $\overline{RAS}$	tRRH	0	-	0	-	ns	8
Write command set-up time	tWCS	0	-	0	-	ns	
Write command hold time	tWCH	10	-	13	-	ns	
Write command pulse width	tWP	10	-	10	-	ns	
Write command to $\overline{RAS}$ read time	tRWL	15	-	20	-	ns	
Write command to $\overline{CAS}$ read time	tCWL	15		20		ns	
Data-in set-up time	tDS	0	-	0	-	ns	
Data-in hold time	tDH	10	-	15	-	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	tRPC	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	tCSR	10	-	10	-	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	tCHR	10	-	10	-	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	tWRP	10	-	10	-	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	tWRH	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up tim (test mode)	tWTS	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (test mode)	tWTH	10	-	10	-	ns	

NOTES:
1. A start-up delay of 200 µs is required after power-up followed by a minimum of 8 *initialisation cycles (RAS only refresh or CAS before RAS refresh)* before proper device operation is achieved.
   When using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.
2. *AC measurement assume* $t_T = 5$ *ns.*
3) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring input signals. Transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit eqivalent to 2 TTL loads and 100 pF.
5. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
7. t_{OFF}defines the time at which time the output achieves an open circuit condition and *is not referenced to output voltage levels.*
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. The test mode is initiated by performing a $\overline{WE}$ and before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated.
   The test mode specified in this data sheets is an 8-bit parallel test function. CA10, CA1 and CA0 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level.
   The test mode is cleared and the memory device returned to its normal operating state *by performing a* $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
10. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.