

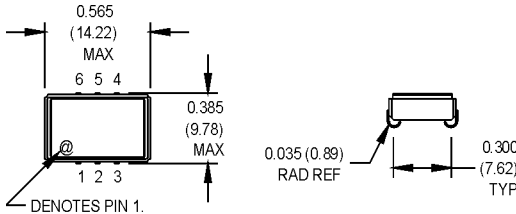
# MPV5J Series

## 9x14 mm, 5.0 Volt, PECL/LVDS VCXO

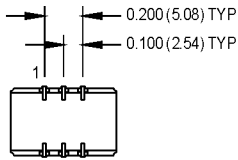
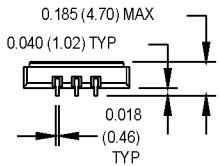


- Integrated phase jitter of less than 1 ps from 12 kHz to 20 MHz
- Ideal for low noise PLL applications

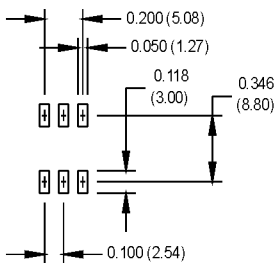
Ordering Information		MPV5J	1	0	B	1	P	J	00.0000
Product Series									MHz
Temperature Range									
1:	0°C to +70°C								
2:	-40°C to +85°C								
6:	-20°C to +70°C								
8:	0°C to +50°C								
Stability									
0:	Nominal per APR selection								
Output Type									
B:	Complementary, Enable (Enable High)								
S:	Complementary, Enable (Enable Low)								
U:	Complementary Output								
Absolute Pull Range									
1:	±50 ppm (±35 ppm typ. Stability)								
8:	±25 ppm (±50 ppm typ. Stability)								
Symmetry/Output Logic Type									
P:	45/55% PECL								
Q:	40/60% PECL								
Package/Lead Configurations									
J:	J-Lead								
Frequency (customer specified)									



All dimensions in inches (mm).



### SUGGESTED SOLDER PAD LAYOUT



### Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Output Enable or N/C
3	Ground/Case
4	Output Q
5	Output Q̄ or N/C
6	+Vcc

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Frequency Range	F	30		800	MHz	(Consult factory for exact frequency availability)
Frequency Stability	$\Delta F/F$	(See Ordering Information)				See Note 1
Operating Temperature	TA	(See Ordering Information)				
Storage Temperature	Ts	-55		+125	°C	
Input Voltage	Vcc	4.75	5.0	5.25	V	
Input Current	Idd		60	70	mA	
Symmetry (Duty Cycle)		(See Ordering Information)				
Load						See Note 2
Rise/Fall Time	Tr/Tf		.35	.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Logic "1" Level	Voh	Vcc - 1.02			V	
Logic "0" Level	Vol			Vcc - 1.63	V	
Phase Jitter	$\phi J$					
@ 77.76 MHz			0.6	0.9	ps RMS	Integrated 12 kHz - 20 MHz
@ 155.52 MHz			0.3	0.55	ps RMS	Integrated 12 kHz - 20 MHz
@ 622.08 MHz			0.25	0.5	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)						Offset from carrier
@ 77.76 MHz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	dBc/Hz
@ 155.52 MHz	-80	-110	-133	-144	-147	dBc/Hz
@ 622.08 MHz	-80	-110	-133	-144	-147	dBc/Hz
		-70	-125	-135	-137	dBc/Hz
Modulation Bandwidth	fm	10			Khz	-3 dB bandwidth
Input Impedance	Zin	50			K $\Omega$	
Control Voltage	Vcc	0		5.0	V	Pin 1 voltage
Center Frequency	Vc0		2.5		V	
Linearity			5	10	%	
Pullability	APR	(See Ordering Information)				See Note 3
Enable/Disable Logic		CMOS high, Vcc or N/C - enables output				Output Option B
		CMOS low or GND - disables output				
		PECL low, GND, or N/C - enables output				Output Option S
		PECL high - disables output				
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C				
	Vibration	Per MIL-STD-202, Method 201 & 204				
	Reflow Solder Conditions	240°C for 10 s max., or 230°C for 90 s max.				
	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 <sup>-8</sup> atm.cc/s of helium)				
	Solderability	Per MIL-STD-883, Method 2003				

1. Stability given for deviation over temperature.
2. PECL load - see load circuit diagram #5.
3. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.

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