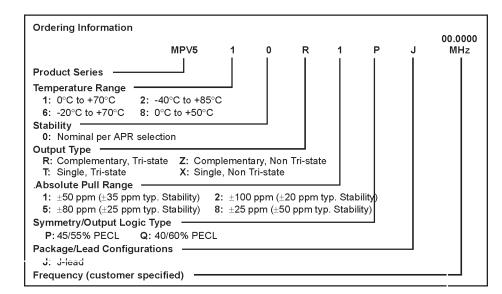
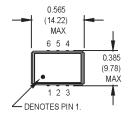
MPV5 Series 9x14 mm, 5.0 Volt, PECL, VCXO



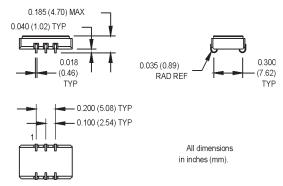


- LVDS and PECL Output Logic With Good Integrated Jitter Performance (5 ps)
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/ Demodulation





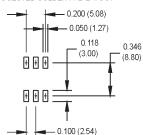
OBSOLETE



Pin Connections

PIN	FUNCTION			
1	Control Voltage			
2	Tri-state or N/C			
3	Ground/Case			
4	Output Q			
5	Output Q or N/C			
6	+Vcc			

SUGGESTED SOLDER PAD LAYOUT



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MPV5 Series 9x14 mm, 5.0 Volt, PECL, VCXO





		1						
	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition	
	Frequency Range	F	0.75		800	MHz	See Note 1	
	Frequency Stability	∆F/F	(See Orde	ring Inforr	nation)		See Note 2	
	Operating Temperature	Ts	-40		+85	°C	See ordering info.	
	Storage Temperature	TA	-55		+125	°C		
	Input Voltage	Vcc	4.75	5.0	5.25	٧		
	Input Current	ldd						
	0.75 MHz to 24 MHz				60	mA		
l	24 MHz to 160 MHz	i	İ	i	100	mA		
	160 MHz to 800 MHz				120	mA		
	Symmetry (Duty Cycle)		40	50	60	%	@ Vcc -1.3 VDC	
	Load						See Note 3	
	Rise/Fall Time	Tr/Tf		.35	.55	ns	@ 20/80%	
	'4" Le		Vcc -			,		
	Logic Le	ર્ગ			c -1.63	,		
	Cycle t yc						1 Sigma	
	@ 38 MI			5,		RMS		
<u>s</u>	3.52 N							
loi l	@ 622.08 MHz			10	20	ps RMS		
cat	Phase Jitter	φJ					Integrated 12 kHz - 20 MHz	
cifi	@ 38.88 MHz			.3	.5	ps RMS		
Electrical Specifications	@ 155.52 MHz			3	5	ps RMS		
	@ 622.08 MHz			3	5	ps RMS		
	Peak to Peak Jitter (+/-)	Tj					@ BER 1E-12	
) 	@ 38.88 MHz			2.1	3.5	ps RMS		
В	@ 155.52 MHz			21	35	ps RMS		
	@ 622.08 MHz			21	35	ps RMS		
	Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier	
	@ 38.88 MHz	-65	-97	-127	-143	-153	dBc/Hz	
	@ 155.52 MHz	-50	-80	-112	-128	-125	dBc/Hz	
	@ 622.08 MHz	-50	-80	-110	-123	-120	dBc/Hz	
iental	Modulation Bandwidth	fm			10k	Hz	-3 dB bandwidth	
	Input Impedance	Zin	50			ΚΩ		
	Control Voltage	Vcc	0.5	2.5	5	V	Pin 1 voltage	
	Center Frequency	Vc0		2.5		V		
	Linearity			5	10	%		
	Pullability	APR	(See Orde	ring Inforr	nation)		See Note 4	
	Tri-state Output "On"	OE	2.8			V	Pin 2 voltage	
	Tri-state Output "Off"	OE			0.6	V	Pin 2 voltage	
	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C						
	Vibration	Per MIL-STD-202, Method 201 & 204						
וצו		See "Figure 2" on page 147						
nme	Reflow Solder Conditions	See "Figu	iie z on paç	JO 177				
Environmental	Reflow Solder Conditions Hermeticity				(1 x 10 ⁻⁸ atm.	.cc/s of heliu	ım)	

- 1. Frequencies above 70 MHz utilize a PLL design. Fundamental and PLL designs are available for other frequencies. Contact factory.

 2. Stability is given for deviation over temperature.
- 3. PECL load see load circuit diagram #3 on page 148.
- 4. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.

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