MN3308

2048-Stage Ultra Low Voltage Operation BBD for Audio Signals

■ Overview

The MN3308 is a 2048-stage ultra low voltage operation BBD variable delay line in audio frequency range. The device operates on +3 V supply and provides a signal delay up to 102.4 ms and is suitable for use as reverberation effect of low voltage operation audio equipment such as portable stereo, radio cassette recorder and microphone.

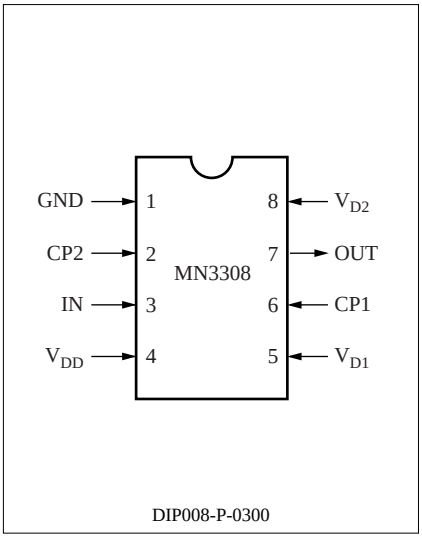
■ Features

- Variable signal delay of the audio signal : 3.42 to 102.4 ms
- Wide range of supply voltage : 1.8 to 7.0 V
- No insertion loss : L_i=0 dB typ.
- Wide dynamic range : S/N=66 dB typ.
- Clock frequency range : 10 to 100 kHz (1.8 V≤V_{DD}<4.0 V)
  10 to 300 kHz (4.0 V≤V_{DD}≤7.0 V)
- N-channel 2-layer silicon gate process
- 8-Pin Dual-In-Line Plastic Package

■ Applications

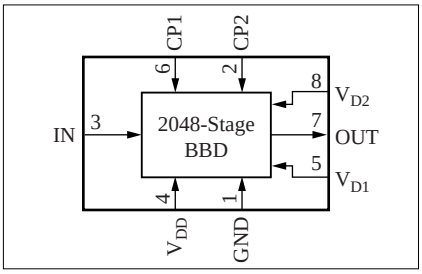
- Reverberation and echo effects of audio equipment such as radio cassette recorder, car radio, portable radio, portable stereo, echo microphone and Karaoke machine, etc.
- Sound effect of electronic musical instruments
- Variable or fixed delay of analog signals

■ Pin Assignment



DIP008-P-0300

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Pin Name	Description
1	GND	Ground pin	Connected to ground.
2	CP2	Clock input 2	Basic clock pulse is applied to transfer electric charge of BBD.
3	IN	Signal input pin	Analog signal to be delayed is input. Most suitable DC bias should be applied to this pin.
4	V_{DD}	V_{DD} apply pin	Bias is applied to the gate of MOS transistor which is inserted in series with clock pulse input gate of the BBD transfer gate. Furthermore, voltage is supplied to step-up circuit.
5	V_{D1}	V_{D1} apply pin	The same phase clock pulse as CP1 is applied through capacitor.
6	CP1	Clock input 1	Clock pulse of inverted phase to CP2 is applied.
7	OUT	Output pin	Composed signal of 1024th and 1025th stages is output.
8	V_{D2}	V_{D2} apply pin	The same phase clock pulse as CP2 is applied through capacitor.

■ Absolute Maximum Ratings Ta=25°C

Parameter	Symbol	Ratings	Unit
Pin voltage	V_{DD}, V_{D1}, V_{D2}, V_{CP}, V_I	– 0.3 to +8.0	V
Output voltage	V_O	– 0.3 to +8.0	V
Operating ambient temperature	T_{opr}	–20 to +60	°C
Storage temperature	T_{stg}	–55 to +125	°C

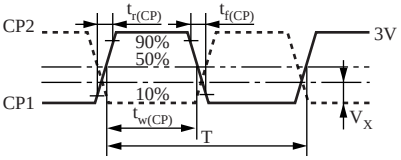
■ Operating Conditions Ta=25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		+1.8	+3.0	+7.0	V
Clock voltage "H"level	V_{CPH}			V_{DD}		V
Clock voltage "L"level	V_{CPL}			0		V
Clock input capacitance	C_{CP}				1400	pF
Clock frequency	f_{CP}		10		100(300)*1	kHz
Clock pulse width	$t_{w(CP)}$ *3				0.5T*2	
Clock rise time	$t_{r(CP)}$ *3				500	ns
Clock fall time	$t_{f(CP)}$ *3				500	ns
Clock cross point	V_X *3		0		0.3V_{CPH}	V

Note) *1 : ( ) : V_{DD}=4.0 to 5.0 V

*2 : T=1/f_{CP} (Clock period)

*3 : Clock pulse waveforms

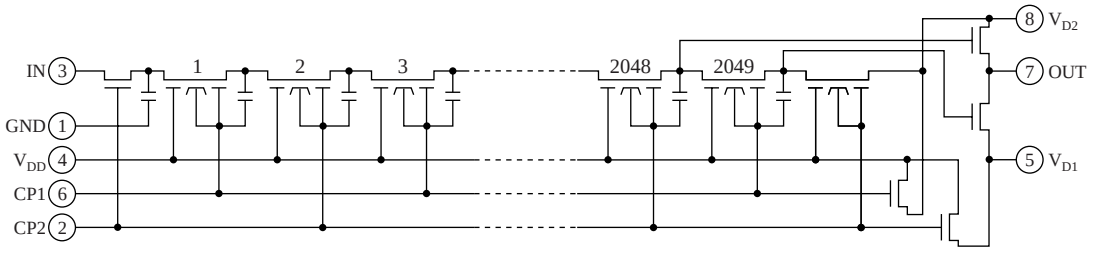


■ Electrical Characteristics V_{DD}=V_{CPH}=3V, V_{CPL}=0V, R_L=56kΩ, LPF : f_C=20kHz, A_{tt}=48dB/oct., Ta=25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current	I_{DD}	f_{CP}=40 kHz		0.05		mA
Signal delay time 1	t_{D1}	V_{DD}=1.8 to 4.0 V, f_{CP}=10 to 100 kHz		$\frac{N^*}{2 \cdot f_{CP}}$		ms
Signal delay time 2	t_{D2}	V_{DD}=4.0 to 5.0 V, f_{CP}=10 to 300kHz				
Input signal frequency	f_i	f_{CP}=40 kHz, V_i=0.22 V_{rms} Output attenuation≤3 dB(0 dB at f_i=1 kHz)	10			kHz
Input signal amplitude	υ_i	f_{CP}=40 kHz, f_i=1 kHz, THD=2.5 %	0.30	0.41		V_{rms}
Insertion loss	L_i	f_{CP}=40 kHz, f_i=1 kHz, V_i=0.22 V_{rms}	–4	0	4	dB
Total harmonic distortion	THD	f_{CP}=40 kHz, f_i=1 kHz, V_i=0.22 V_{rms}		1.0	2.5	%
Output noise voltage	V_{no}	f_{CP}=100 kHz, Weighted by "A"curve		0.19	0.35	mV_{rms}
Signal to noise ratio	S/N			66		dB

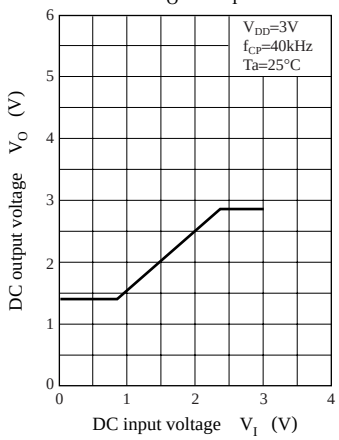
Note) * : N=BBD stages

■ Circuit Diagram

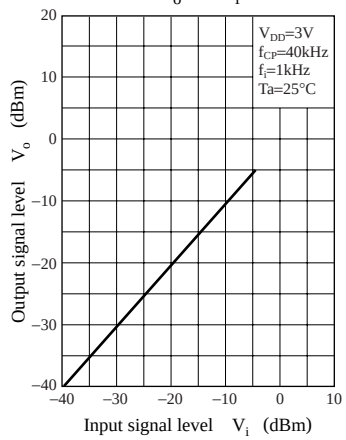


■ Typical Characteristics

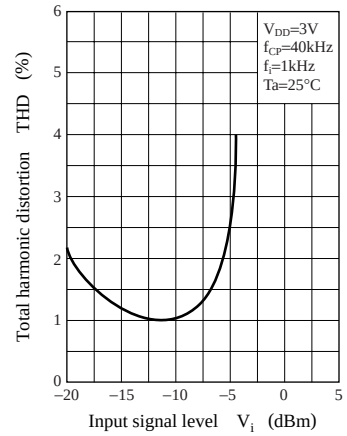
V_O — V_I



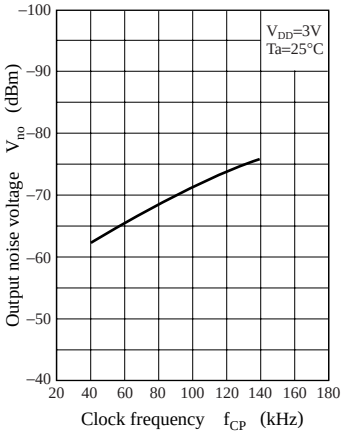
V_o — V_i



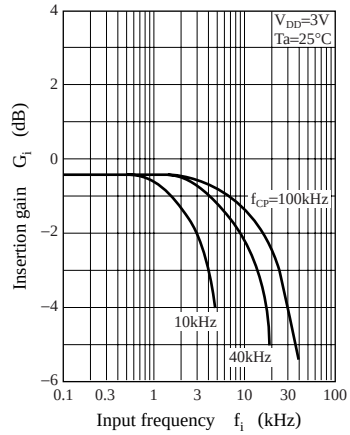
THD — V_i



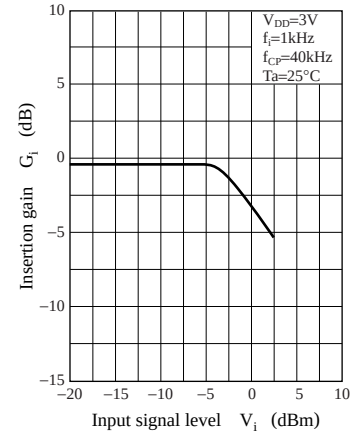
V_{no} — f_{CP}



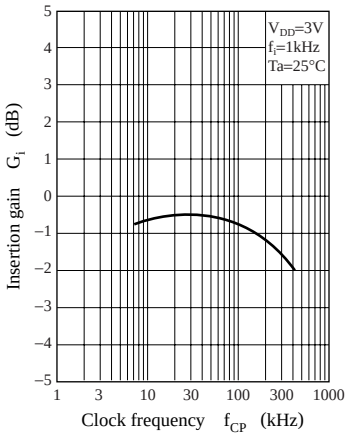
G_i — f_i



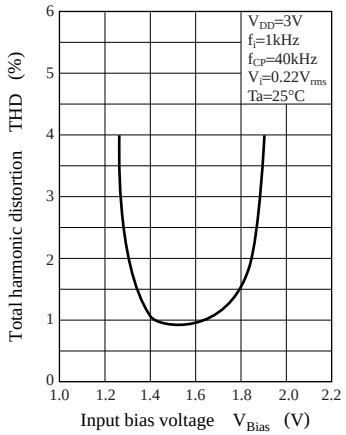
G_i — V_i



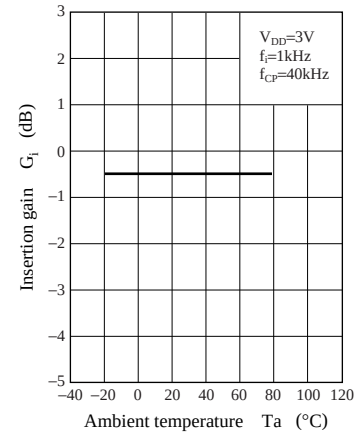
G_i — f_{CP}



THD — V_{Bias}

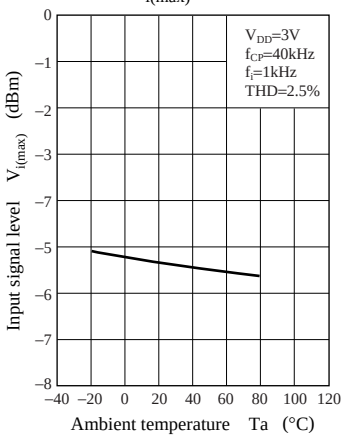


G_i — Ta

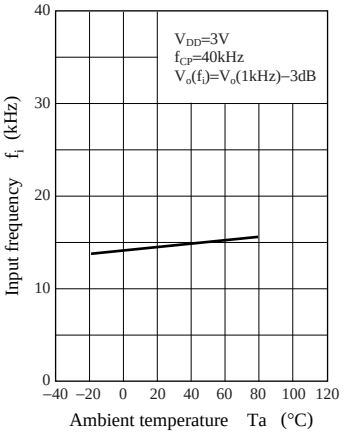


■ Typical Characteristics (To be continued)

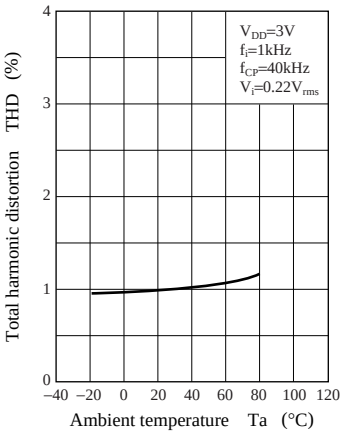
$V_{i(max)}$ — Ta



f_i — Ta

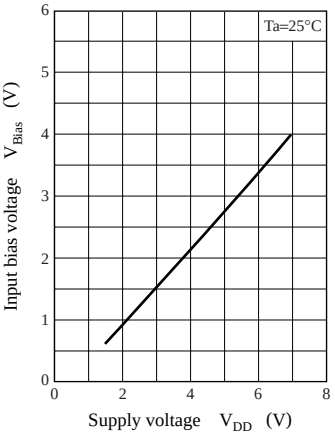


THD — Ta

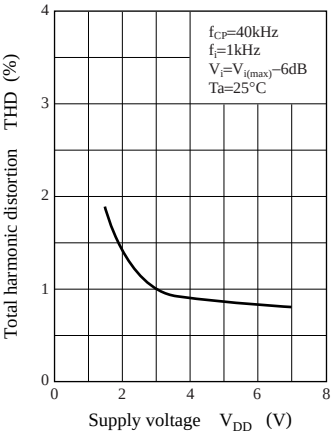


■ Supply Voltage Characteristics

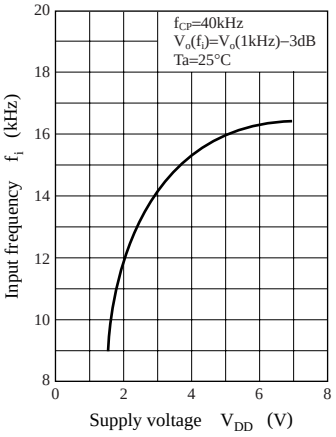
V_{Bias} — V_{DD}



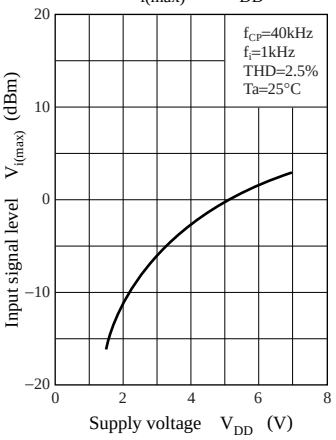
THD — V_{DD}



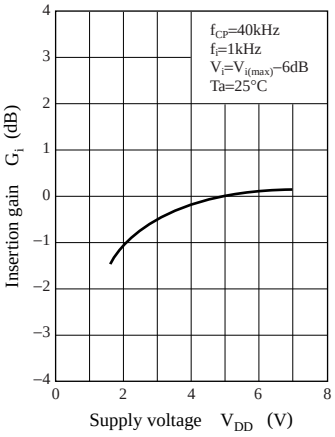
f_i — V_{DD}



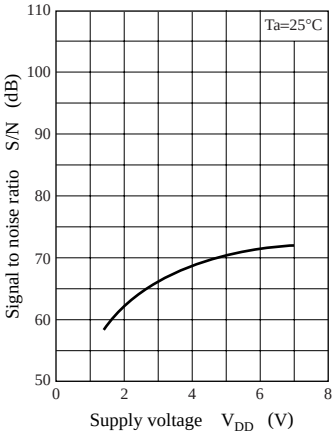
$V_{i(max)}$ — V_{DD}



G_i — V_{DD}



S/N — V_{DD}



■ Package Dimensions (Unit : mm)

• DIP008-P-0300