PEDL9371-01
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OKI Semiconductor

ML9371 Preliminary

64-Channel Organic EL Cathode Driver

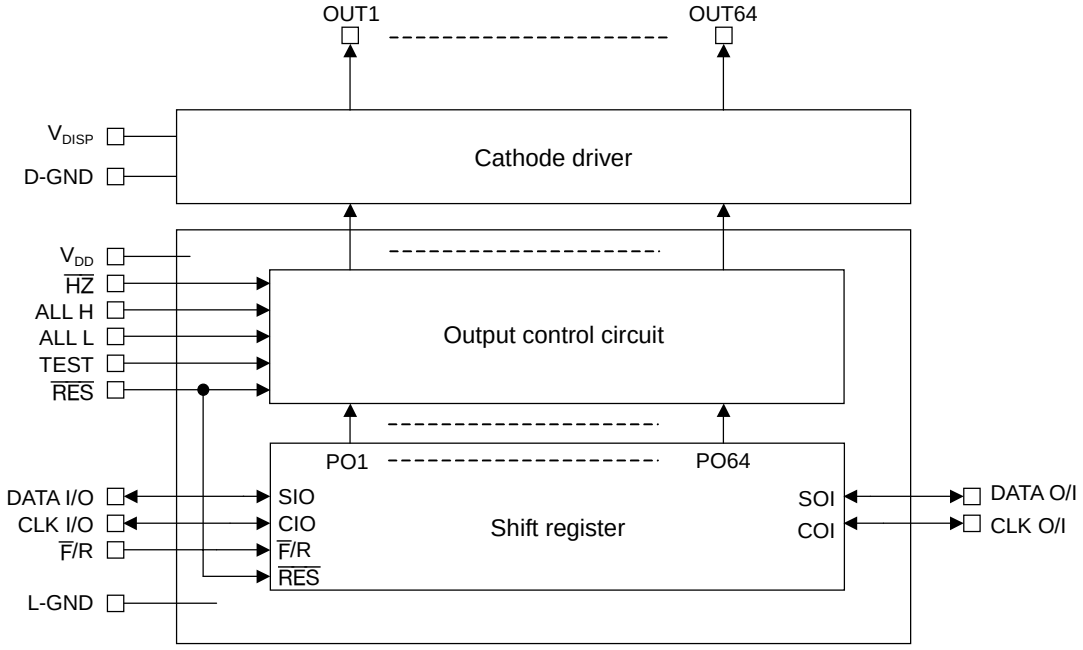
GENERAL DESCRIPTION

The ML9371 is an organic EL cathode driver LSI with 64 outputs. Since this LSI has the output condition setting function, which allows setting of all outputs High, all outputs Low, and all outputs High Impedance, the user can set driving methods suited to the characteristics of individual organic EL panel. When combined with ML9361 the organic EL anode driver, the ML9371 can drive a 64 × 128 full-dot panel.

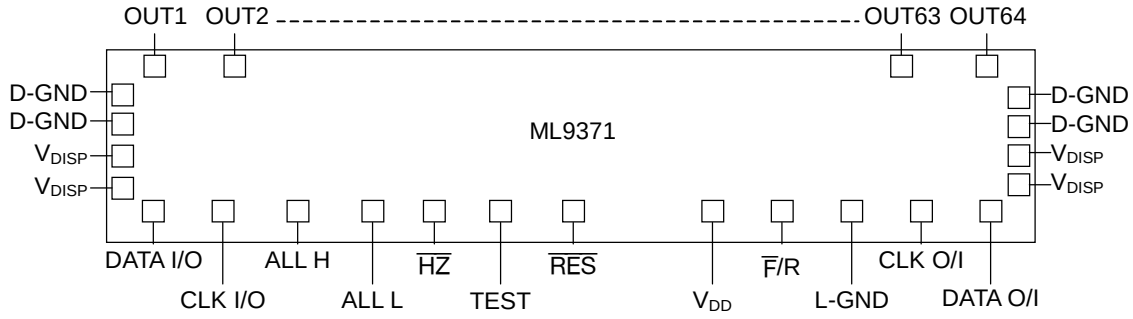
FEATURES

- Logic power supply voltage : 3.0 to 5.5 V
- EL drive voltage : 8.0 to 30 V
- Cathode outputs : 64 outputs
- Cathode low output current : 150 mA (max.)
- Cathode high output current : –50 mA (max.)
- Cathode low ON-resistance : 5Ω (max.)
- Cathode high ON-resistance : 100Ω (max.)
- All outputs High, all outputs Low, all outputs High Impedance
- Package : Gold bump chip (TCP is tailored for each customer requirement)

BLOCK DIAGRAM



PIN CONFIGURATION (View from the Pad Layout Side)



PIN DESCRIPTION

Symbol	Type	Description
V_{DISP} V_{DD} D-GND L-GND	—	V_{DISP} is the cathode driver circuit power supply pin. V_{DD} is the logic circuit power supply pin. D-GND is a ground pin for cathode driver circuit. L-GND is a ground pin for logic circuit. D-GND and L-GND should be connected outside the LSI.
$\overline{RES}$	I	Input pin for register initialization signal. When this pin is set low, the LSI enters the following initial setting states: • Shift register outputs (POm): all “low” (m = 1 to 64) • All cathode drive signal outputs (OUT1 to OUT64): “high impedance”
$\overline{F}$/R	I	Input pin for data transfer direction select signal for shift register. • When this pin is low, data is transferred starting at PO1 toward PO64. • When this pin is high, data is transferred starting at PO64 toward PO1.
DATA I/O	I/O	Cathode scan data input-output pin. When the $\overline{F}$/R pin is low, this pin is an input pin, and when it is high, this pin is an output pin.
DATA O/I	I/O	Cathode scan data input-output pin. When the $\overline{F}$/R pin is low, this pin is an output pin, and when it is high, this pin is an input pin.
CLK I/O	I/O	Cathode scan data transfer clock input-output pin. When the $\overline{F}$/R pin is low, this pin is an input pin, and when it is high, this pin is an output pin.
CLK O/I	I/O	Cathode scan data transfer clock input-output pin. When the $\overline{F}$/R pin is low, this pin is an output pin, and when it is high, this pin is an input pin.
$\overline{HZ}$	I	Input pin for cathode drive signal output control signal. When this pin is low, all cathode drive signal outputs (OUT1 to OUT64) are high impedance.
ALL H	I	Input pin for cathode drive signal output control signal. When this pin is high, all cathode drive signal outputs (OUT1 to OUT64) are high.
ALL L	I	Input pin for cathode drive signal output control signal. When this pin is high, all cathode drive signal outputs (OUT1 to OUT64) are low.
TEST	—	Pin for production tests. Leave this pin open or connect it to L-GND.
OUT 1 to 64	O	Cathode drive signal output pin.

FUNCTION TABLE

1. Shift Register Operation during Cathode Scan Data Transfer

Input/Output						Shift Register Parallel Out			
$\overline{RES}$	F/$\overline{R}$	CLK I/O	DATA I/O	CLK O/I	DATA O/I	PO 1	PO 2	PO 63	PO 64
L	L	Input	Input	Output	Output	L	L	L	L
	H	Output	Output	Input	Input	L	L	L	L
H	L	↑	L	Output	Output	L	PO 1n	PO 62n	PO 63n
			H			H	PO 1n	PO 62n	PO 63n
		↓	L			Invariable			
			H						
	H	Output	Output	↑	L	PO 2n	PO 3n	PO 64n	L
					H	PO 2n	PO 3n	PO 64n	H
				↓	L	Invariable			
					H				

PO1n to PO64n: States of PO1 to PO64 immediately before the clock rises

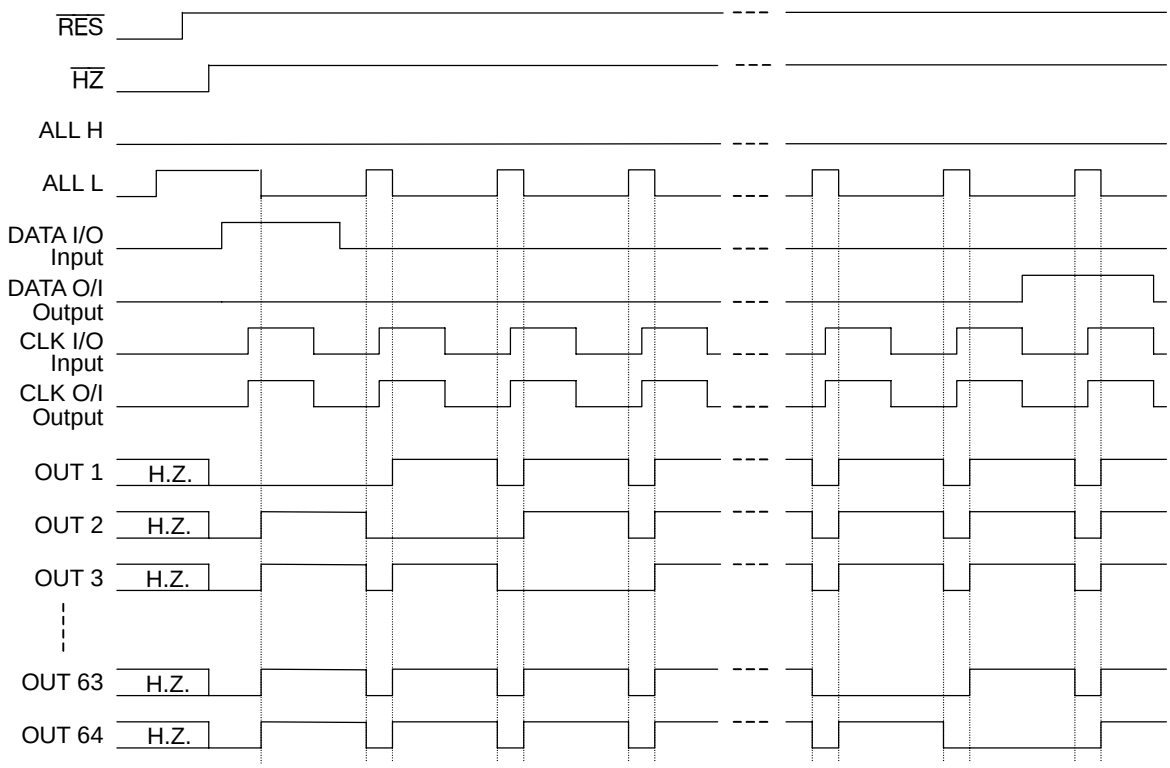
2. Operation of Output Section

$\overline{RES}$	$\overline{HZ}$	ALL H	ALL L	POm	OUTm
L	X	X	X	L	High impedance
H	L	X	X	X	High impedance
	H	H	X	X	High
		L	H	X	Low
			L	H	Low
				L	High

X: Don't Care

OUTPUT WAVEFORMS

When $\overline{F}$/R is low



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
EL drive power supply voltage (cathode)	V_{DISP}	Ta = 25°C	–0.3 to +35	V
Logic input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Logic output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
EL driver output voltage	V_{OUT-EL}	Applied to OUT1 to OUT64	–0.3 to V_{DISP} + 0.3	V
EL driver output voltage (pulse)*1	$V_{OUT-ELP}$	Applied to OUT1 to OUT64	$-V_{DISP}$ to 2 × V_{DISP}	V
EL driver output current	I_{ELL} (sink)	Applied to OUT1 to OUT64	200	mA
	I_{ELH} (source)		–70	mA
Storage temperature	Tstg	—	–40 to +125	°C

*1 Consult Oki for customization of pulse width.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Logic power supply voltage	V_{DD}	—		3.0 to 5.5	V
EL drive power supply voltage (cathode)	V_{DISP}	—		8 to 30	V
Logic input voltage	V_{IN}	—		0.0 to V_{DD}	V
EL driver output current	I_{ELL} (sink)	Applied to OUT1 to OUT64	V_O = 0.75 V	150	mA
	I_{ELH} (source)		V_{DISP} = 14 V $V_O = V_{DISP} - 5$ V	–50	mA
Junction operating temperature	Tjop	—		–40 to +125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{DD} = 3.0 to 5.5 V, V_{DISP} = 8 to 30 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable Pins	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	All input pins	—	$0.8V_{DD}$	—	V_{DD}	V
"L" input voltage	V_{IL}	All input pins	—	0	—	$0.2V_{DD}$	V
Schmitt voltage width	V_{SH}	CLK I/O, CLK O/I ALL H, ALL L	V_{DD} = 5.0 V	0.4	—	0.9	V
"H" input current	I_{IH1}	DATA I/O, DATA O/I CLK I/O, CLK O/I Input state	V_{DD} = 5.5 V V_I = 5.5 V	–10	—	10	μA
	I_{IH2}	$\overline{RES}$, $\overline{F}$/R, $\overline{HZ}$ ALL H, ALL L	V_{DD} = 5.5 V V_I = 5.5 V	30	—	140	μA
"L" input current	I_{IL1}	DATA I/O, DATA O/I CLK I/O, CLK O/I Input state	V_{DD} = 5.5 V V_I = 0.0 V	–10	—	10	μA
	I_{IL2}	$\overline{RES}$, $\overline{F}$/R, $\overline{HZ}$ ALL H, ALL L	V_{DD} = 5.5 V V_I = 0.0 V	–10	—	10	μA
"H" output voltage	V_{OH}	DATA I/O, DATA O/I CLK I/O, CLK O/I Output state	V_{DD} = 3.0 V I_O = –200 μA	$0.8V_{DD}$	—	—	V
"L" output voltage	V_{OL}	DATA I/O, DATA O/I CLK I/O, CLK O/I Output state	V_{DD} = 3.0 V I_O = 200 μA	—	—	$0.2V_{DD}$	V
"H" output current	I_{ELH}	OUT1 to OUT64	V_{DISP} = 14 V V_O = 9 V Only one output is high	–50	—	—	mA
"L" output current 1	I_{ELL1}	OUT1 to OUT64	V_{DISP} = 14 V V_O = 0.75 V Only one output is low	150	—	—	mA
"L" output current 2	I_{ELL2}	OUT1 to OUT64	V_{DISP} = 14 V V_O = 5 V ALL L = high	50	—	—	mA
Supply current	I_{DISP1}	V_{DISP}	V_{DD} = 5.5 V, V_{DISP} = 30 V Clock = 100 kHz The low state of only one output is scanned. *1 No load	—	—	30	mA
	I_{DISP2}	V_{DISP}	V_{DD} = 5.5 V, V_{DISP} = 30 V Clock = 10 kHz The low state of only one output is scanned. *1 No load	—	—	3	mA
	I_{DISPS}	V_{DISP}	V_{DD} = 5.5 V, V_{DISP} = 30 V Clock stopped $\overline{RES}$ = low No load	—	—	30	μA
	I_{DD}	V_{DD}	V_{DD} = 5.5 V, V_{DISP} = 30 V Clock = 100 kHz The low state of only one output is scanned. *1 No load	—	—	3	mA
	I_{DDS}	V_{DD}	$\overline{RES}$ = low No load	—	—	10	μA

*1 See the section of "OUTPUT WAVEFORMS".

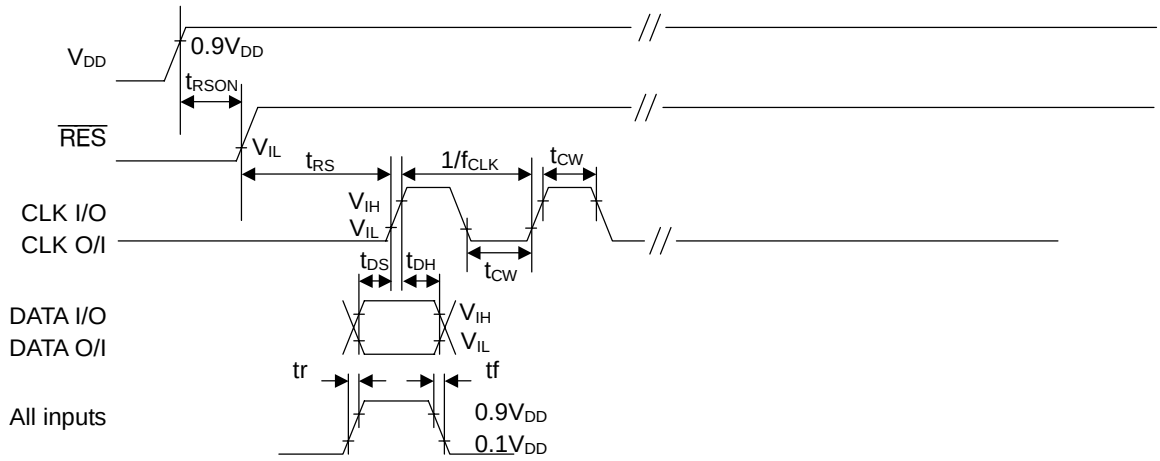
AC Characteristics

V_{DD} = 3.0 to 5.5 V, V_{DISP} = 8 to 30 V, Tjop = –40 to +125°C

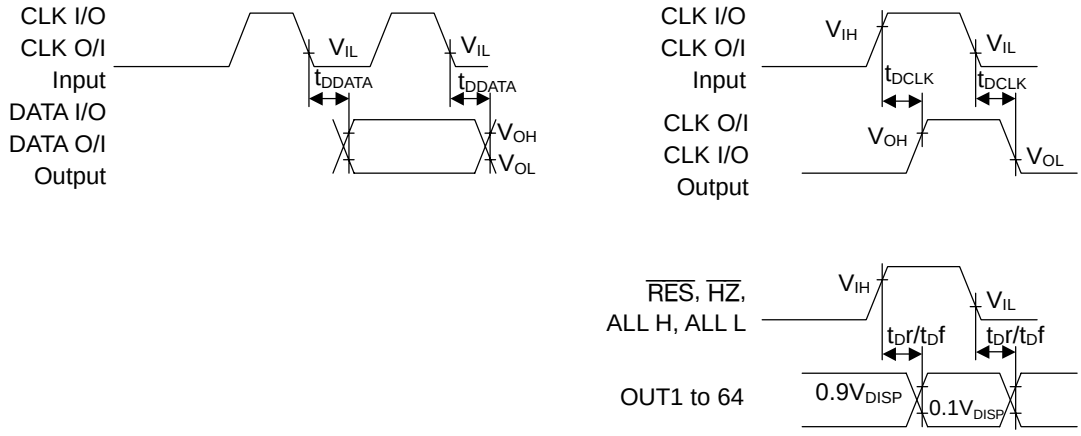
Parameter	Symbol	Applicable pins	Condition	Min.	Typ.	Max.	Unit
CLK frequency	f_{CLK}	CLK I/O, CLK O/I	—	—	—	100	kHz
CLK pulse width	t_{CW}	CLK I/O, CLK O/I	—	5	—	—	µs
DATA → CLK setup time	t_{DS}	CLK I/O, DATA I/O CLK O/I, DATA O/I	—	50	—	—	ns
CLK → DATA hold time	t_{DH}	CLK I/O, DATA I/O CLK O/I, DATA O/I	—	50	—	—	ns
Reset execution time	t_{RSON}	V_{DD}, $\overline{RES}$	—	250	—	—	ns
$\overline{RES}$ → CLK reset recovery time	t_{RS}	CLK I/O, CLK O/I $\overline{RES}$	—	250	—	—	ns
CLK input/output delay time	t_{DCLK}	CLK I/O, CLK O/I	CL = 45 pF	—	—	100	ns
Data output delay time	t_{DDATA}	CLK I/O, DATA O/I CLK O/I, DATA I/O	CL = 45 pF	—	—	100	ns
Cathode output delay time	t_Dr t_Df	$\overline{RES}$, $\overline{HZ}$, ALL H, ALL L OUT1 to OUT64	CL = 45 pF	—	—	2.0	µs
Input signal rise/fall time	tr tf	All input pins	—	—	—	500	ns

TIMING DIAGRAMS

Data Input



Output Delay



POWER APPLYING SEQUENCE

When applying power, apply it to the logic power supply (V_{DD}) first, then to the EL drive power supply (V_{DISP}). When turning the power off, turn off the EL drive power supply (V_{DISP}) first, then the logic power supply (V_{DD}).

Make the $\overline{RES}$ pin high at least 250 ns after applying power to V_{DD}.
(Refer to Reset execution time in AC Characteristics.)

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9371-01	Dec. 9, 2002	–	–	Preliminary edition 1

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