FEDL9261A-01
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OKI Semiconductor

ML9261A

60-Bit Vacuum Fluorescent Display Tube Grid/Anode Driver

GENERAL DESCRIPTION

The ML9261A is a monolithic IC designed for directly driving the grid and anode of the vacuum fluorescent display (VFD) tube. The device contains a 60-bit shift register, a 60-bit register circuit, and 60 VFD tube driving circuits on a single chip.

Display data is serially stored in the shift register at the rising edge of a clock pulse.

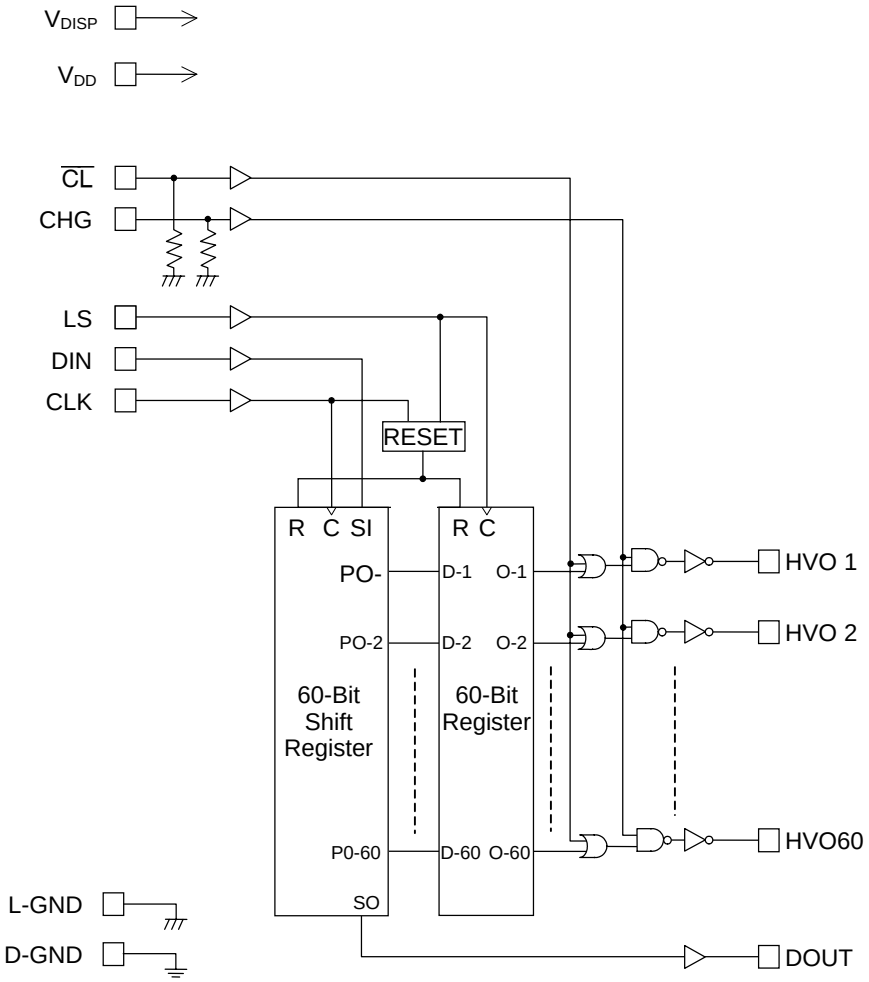
Setting the $\overline{CL}$ pin low allows all the VFD tube driving circuits to be driven low, which makes it possible to set the display blanking.

Also, setting both of the $\overline{CL}$ and CHG pins high allows all the VFD tube driving circuits to be driven high, which provides the easy testing of all lights after final assembly of a VFD tube panel.

FEATURES

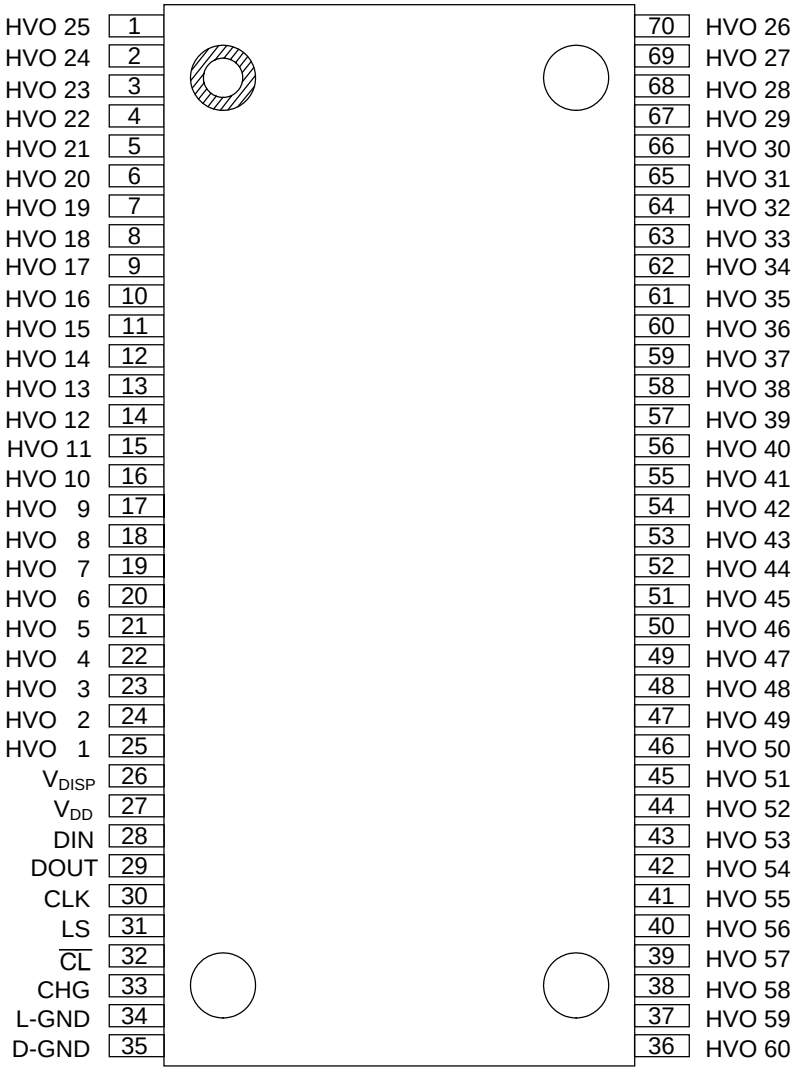
- Logic Supply Voltage (V_{DD}) : +3.3 V ± 10% or +5.0 V ± 10%
- Driver Supply Voltage (V_{DISP}) : +20 to +60 V
- Driver Output Current
  - I_{OHVH1} (Only one driver output: "H") : –40 mA (V_{DISP} = 40 V)
  - I_{OHVH2} (All the driver outputs: "H") : –120 mA (V_{DISP} = 40 V)
  - I_{OHVL} : 1 mA
- Directly connected to VFD tube by using push-pull output (Pull-down resistors are not needed)
- Data Transfer Speed : 4 MHz
- Package: 70-pin plastic SSOP (SSOP70-P-500-0.80-K) : ML9261AMB

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

ML9261A



70-Pin Plastic SSOP
(SSOP70-P-500-0.80-K)

PIN DESCRIPTION

Symbol	Type	Description
CLK	I	Shift register clock input pin. Shift register reads data from DIN while the CLK pin is low and the data in the shift register is shifted from one stage to the next stage at the rising edge of the clock.
DIN	I	Serial data input pin of the shift register. Display data (positive logic) is input in the DIN pin in synchronization with clock.
DOUT	O	Serial data output pin of the shift register. Data is output from the DOUT pin in synchronization with the CLK signal.
LS	I	Latch strobe input pin. The contents of the parallel outputs (PO1 to PO60) of the shift register are read at the rising edge of LS (edge-triggered). When the CLK rises while LS is high, the parallel outputs (PO1 to PO60) and latch outputs (O1 to O60) go low.
$\overline{CL}$	I	Clear input pin with a built-in pull-down resistor. The $\overline{CL}$ pin is normally set high. If the $\overline{CL}$ pin is high and the CHG pin is low, the driver outputs (HVO1 to HVO60) are in phase with the corresponding register outputs (O1 to O60). If the $\overline{CL}$ pin is high and the CHG pin is high, the driver outputs (HVO1 to HVO60) are high irrespective of the states of the register outputs. If the $\overline{CL}$ pin is set low, the driver outputs are driven low irrespective of the states of the CHG pin and register outputs. This allows display blanking to be set.
CHG	I	Input for testing (with a pull-down resistor). The $\overline{CL}$ pin is normally set low. If the CHG pin is low and the $\overline{CL}$ pin is high, the driver outputs (HVO1 to HVO60) are in phase with the corresponding register outputs (O1 to O60). If the CHG pin is low and the $\overline{CL}$ pin is low, the driver outputs (HVO1 to HVO60) are low irrespective of the states of the register outputs. If the CHG pin is set high, the driver outputs are driven high irrespective of the states of the register outputs. This provides the easy testing of all lights after final assembly.
VHO1-60	O	High voltage driver outputs for driving a VFD tube. If the $\overline{CL}$ pin is high and the CHG pin is low, the driver outputs are in phase with the corresponding register outputs (O1 to O60). The direct connection to the grid or anode of a VFD tube eliminates pull-down resistors.
V_{DISP}		Power supply pin for VFD tube driver circuits
V_{DD}		Power supply pin for logic
D-GND		GND pin for VFD tube driver circuits. Since the D-GND pin is not connected internally to the L-GND pin, connect these pins outside of the IC.
L-GND		GND pin for the logic circuits. Since the L-GND pin is not connected internally to the D-GND pin, connect thiese pins outside of the IC.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Condition	Rating	Unit
Supply Voltage (1)	*1	V_{DD}	Applicable to logic supply pin	–0.3 to +6.5	V
Supply Voltage (2)	*1, *2	V_{DISP}	Applicable to driver supply pin	–0.3 to +70	V
Input Voltage	*1	V_{IN}	Applicable to all input pins	–0.3 to V_{DD} +0.3	V
Output Voltage	*1	V_O	Applicable to DOUT	–0.3 to V_{DD} +0.3	V
Output Current		I_O	Applicable to HVO1 to HVO60	–50 to 0.0	mA
Withstand Output Voltage	*1, *2	V_{HVO}	Applicable to HVO1 to HVO60	–0.3 to V_{DISP} +0.3	V
Power Dissipation		P_D	Ta ≤ 25°C	1.47	W
Package Thermal Resistance	*3	R_{j-a}	Ta > 25°C	68	°C/W
Storage Temperature		T_{STG}	—	–55 to +150	°C

Notes: *1 Supply Voltage for L-GND and D-GND
*2 Permanent damage may be caused if the voltage is supplied over the rating value.
*3 Package Thermal Resistance (between junction and ambient)
The junction temperature (T_j) expressed by the equation indicated below should not exceed 125°C under the operating conditions.
$T_j = P \times R_{j-a} + Ta$ (P: Maximum power consumption)

RECOMMENDED OPERATING CONDITIONS-1

Unit Power Supply: 5.0 V (Typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply (1)	V_{DD}	—	4.5	5.0	5.5	V
Power Supply (2)	V_{DISP}	—	20	—	60	V
"H" Input Voltage	V_{IH}	Applicable to all inputs	0.7 V_{DD}	—	—	V
"L" Input Voltage	V_{IL}	Applicable to all inputs	—	—	0.3 V_{DD}	V
Driver Output Current	I_{OHVH1}	Only 1 output is ON.	—	—	–40	mA
	I_{OHVH2}	All outputs are ON.	—	—	–120	mA
CLK Frequency	f_{CLK}	—	—	—	4.0	MHz
Operating Temperature	T_{OP}	—	–40	—	+85	°C

RECOMMENDED OPERATING CONDITIONS-2

Unit Power Supply: 3.3 V (Typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply (1)	V_{DD}	—	3.0	3.3	3.6	V
Power Supply (2)	V_{DISP}	—	20	—	60	V
"H" Input Voltage	V_{IH}	Applicable to all inputs	0.8 V_{DD}	—	—	V
"L" Input Voltage	V_{IL}	Applicable to all inputs	—	—	0.2 V_{DD}	V
Driver Output Current	I_{OHVH1}	Only 1 output is ON.	—	—	–40	mA
	I_{OHVH2}	All outputs are ON.	—	—	–120	mA
CLK Frequency	f_{CLK}	—	—	—	4.0	MHz
Operating Temperature	T_{OP}	—	–40	—	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics-1

(V_{DD} = 4.5 to 5.5 V, V_{DISP} = 20 to 60 V, Ta = –40 to +85°C)

Parameter	Symbol	Applicable pin	Condition		Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	All inputs	—		0.7 V_{DD}	—	—	V
"L" Input Voltage	V_{IL}	All inputs	—		—	—	0.3 V_{DD}	V
"H" Input Current	I_{IH1}	DIN, CLK, LS	V_{DD} = V_{IN} = 5.5 V		–1.0	—	+1.0	µA
	I_{IH2}	$\overline{CL}$, CHG	V_{DD} = V_{IN} = 5.5 V		5.0	—	80	µA
"L" Input Current	I_{IL}	All inputs	V_{DD} = 5.5 V, V_{IN} = 0 V		–1.0	—	+1.0	µA
Input Capacitance	C_{IN}	All inputs	Ta = 25°C		—	15	—	pF
"H" Output Voltage	V_{OH1}	DOUT	I_{OH} = –0.1 mA		V_{DD}–1	—	—	V
	V_{OH2}	HVO1 to 60	V_{DISP} = 40 V I_{OH} = –40 mA		V_{DISP}–4	—	—	V
"L" Output Voltage	V_{OL1}	DOUT	I_{OL} = 0.1 mA		—	—	1.1	V
	V_{OL2}	HVO1 to 60	V_{DISP} = 40 V I_{OL} = 1 mA		—	—	3.0	V
Supply Current	I_{DD1}	V_{DD}	No load	All inputs: "L"	—	—	10.0	µA
	I_{DD2}	V_{DD}		All inputs: "H"	—	—	10.0	µA
	I_{DISP1}	V_{DISP}		All inputs: "L"	—	—	70.0	µA
	I_{DISP2}	V_{DISP}		All inputs: "H"	—	—	70.0	µA

DC Characteristics-2

(V_{DD} = 3.0 to 3.6 V, V_{DISP} = 20 to 60 V, Ta = –40 to +85°C)

Parameter	Symbol	Applicable pin	Condition		Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	All inputs	—		0.8 V_{DD}	—	—	V
"L" Input Voltage	V_{IL}	All inputs	—		—	—	0.2 V_{DD}	V
"H" Input Current	I_{IH1}	DIN, CLK, LS	V_{DD} = V_{IN} = 3.3 V		–1.0	—	+1.0	µA
	I_{IH2}	$\overline{CL}$, CHG	V_{DD} = V_{IN} = 3.3 V		2.0	—	50	µA
"L" Input Current	I_{IL}	All inputs	V_{DD} = 3.3 V, V_{IN} = 0 V		–1.0	—	+1.0	µA
Input Capacitance	C_{IN}	All inputs	Ta = 25°C		—	15	—	pF
"H" Output Voltage	V_{OH1}	DOUT	I_{OH} = –0.1 mA		V_{DD}–1	—	—	V
	V_{OH2}	HVO1 to 60	V_{DISP} = 40 V I_{OH} = –40 mA		V_{DISP}–4	—	—	V
"L" Output Voltage	V_{OL1}	DOUT	I_{OL} = 0.1 mA		—	—	1.1	V
	V_{OL2}	HVO1 to 60	V_{DISP} = 40 V I_{OL} = 1 mA		—	—	3.0	V
Supply Current	I_{DD1}	V_{DD}	No load	All inputs: "L"	—	—	10.0	µA
	I_{DD2}	V_{DD}		All inputs: "H"	—	—	10.0	µA
	I_{DISP1}	V_{DISP}		All inputs: "L"	—	—	70.0	µA
	I_{DISP2}	V_{DISP}		All inputs: "H"	—	—	70.0	µA

AC Characteristics-1

(V_{DD} = 4.5 to 5.5 V, V_{DISP} = 20 to 60 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CLK Pulse Width	t_W (CLK)	—	80	150	ns
DIN Setup Time	t_{SU} (D-CLK)	—	50	—	ns
DIN Hold Time	t_H (CLK-D)	—	50	—	ns
CLK-LS Setup Time	t_{SU} (CLK-LS)	—	50	—	ns
LS-CLK Setup Time	t_{SU} (LS-CLK)	During normal operation	50	—	ns
	t_{SU} (L-CLK)	At display data reset	50	—	ns
CLK-LS Hold Time	t_H (CLK-L)	At display data reset	50	—	ns
LS-CHG Setup Time	t_{SU} (LS-CHG)	—	50	—	ns
LS-$\overline{CL}$ Setup Time	t_{SU} (LS-$\overline{CL}$)	—	50	—	ns
LS Pulse Width	t_W (LS)	—	80	—	ns
CHG Pulse Width	t_W (CHG)	—	10	—	µs
$\overline{CL}$ Pulse Width	t_W ($\overline{CL}$)	—	10	—	µs
DOUT Delay time	t_{PD}, t_{PRD}	Load: 30 pF	—	50	ns
Driver Output Delay Time	t_{DLH}	V_{DISP} = 40 V	—	2.0	µs
	t_{DHL}	Load: 1.0 kΩ resistance in	—	2.0	µs
	t_{DRHL}	parallel with 20 pF capacitance	—	2.0	µs
Driver Output Slew Rate	t_{TLH}	V_{DISP} = 40 V	—	5.0	µs
	t_{THL}	Load: 1.0 kΩ resistance in parallel with 20 pF capacitance	—	5.0	µs

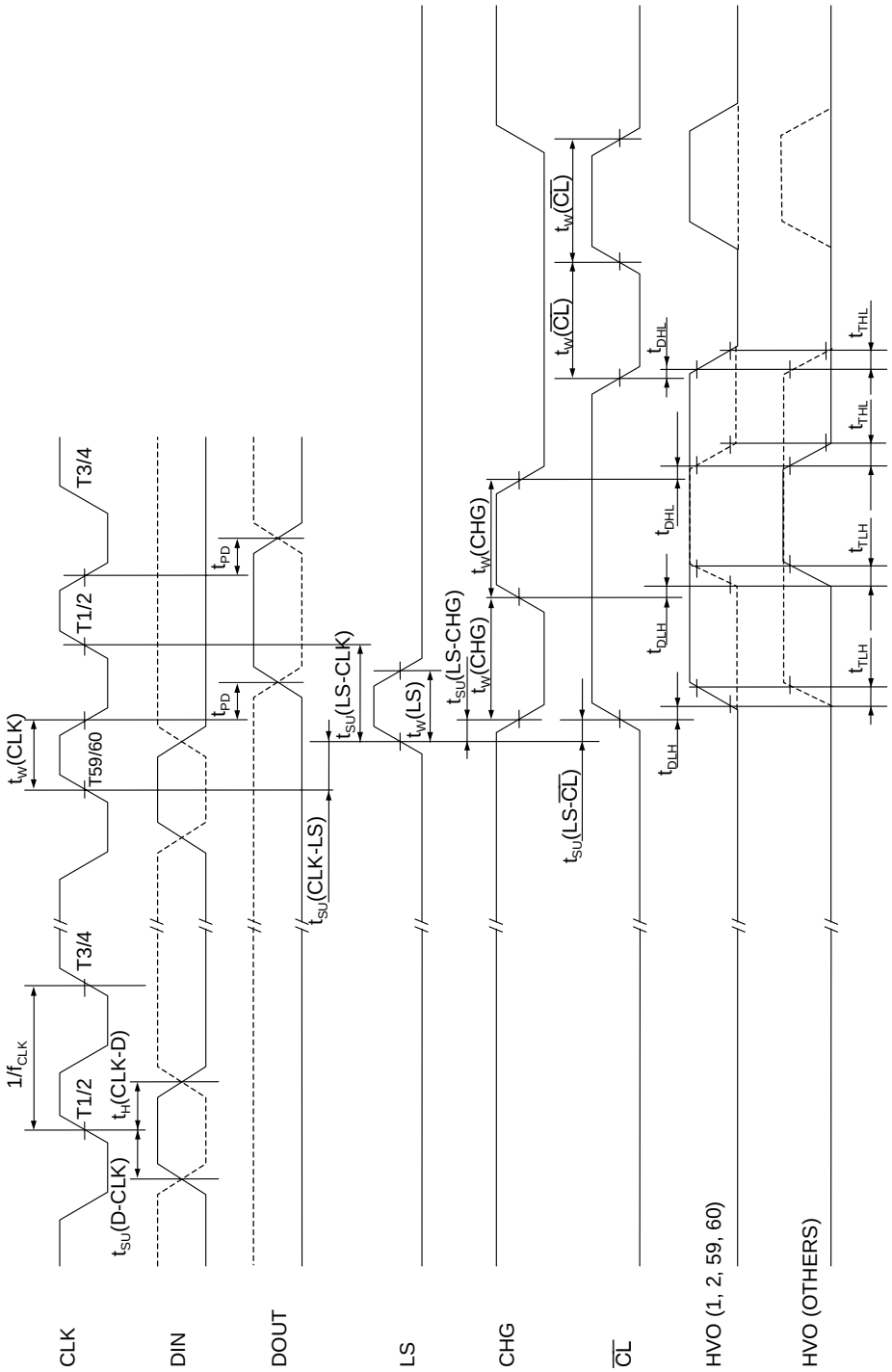
AC Characteristics-2

(V_{DD} = 3.0 to 3.6 V, V_{DISP} = 20 to 60 V, Ta = –40 to +85°C)

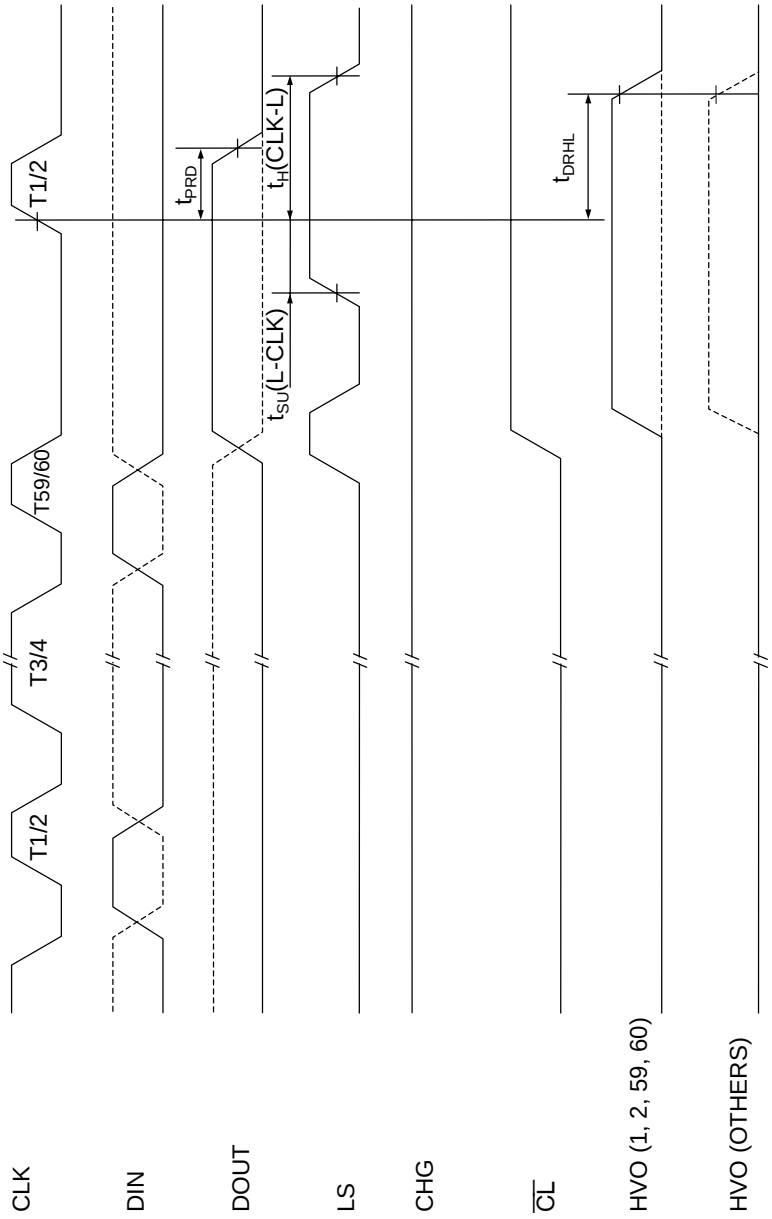
Parameter	Symbol	Condition	Min.	Max.	Unit
CLK Pulse Width	t_W (CLK)	—	80	150	ns
DIN Setup Time	t_{SU} (D-CLK)	—	50	—	ns
DIN Hold Time	t_H (CLK-D)	—	50	—	ns
CLK-LS Setup Time	t_{SU} (CLK-LS)	—	50	—	ns
LS-CLK Setup Time	t_{SU} (LS-CLK)	During normal operation	50	—	ns
	t_{SU} (L-CLK)	At display data reset	50	—	ns
CLK-LS Hold Time	t_H (CLK-L)	At display data reset	50	—	ns
LS-CHG Setup Time	t_{SU} (LS-CHG)	—	50	—	ns
LS-$\overline{CL}$ Setup Time	t_{SU} (LS-$\overline{CL}$)	—	50	—	ns
LS Pulse Width	t_W (LS)	—	80	—	ns
CHG Pulse Width	t_W (CHG)	—	10	—	µs
$\overline{CL}$ Pulse Width	t_W ($\overline{CL}$)	—	10	—	µs
DOUT Delay time	t_{PD}, t_{PRD}	Load: 30 pF	—	50	ns
Driver Output Delay Time	t_{DLH}	V_{DISP} = 40 V	—	3.0	µs
	t_{DHL}	Load: 1.0 kΩ resistance in	—	3.0	µs
	t_{DRHL}	parallel with 20 pF capacitance	—	3.0	µs
Driver Output Slew Rate	t_{TLH}	V_{DISP} = 40 V	—	5.0	µs
	t_{THL}	Load: 1.0 kΩ resistance in parallel with 20 pF capacitance	—	5.0	µs

TIMING DIAGRAMS

Normal Display Operation



Display Data Reset Operation



FUNCTIONAL DESCRIPTION

Display Data Reset

When the power is turned on, the shift register outputs (PO1 to PO60) and register outputs (O1 to O60) are indeterminate. Consequently the display of a VFD tube may flicker because unnecessary driver outputs go high. To prevent such flicker, it is required to perform the following operations.

1. Turn on the logic power supply while the $\overline{CL}$ input is kept low.
2. Set the LS input high.
3. Switch the CLK input from a low level to a high level at least once.

By performing the above operations, all of the shift register outputs (PO1 to PO60) and register outputs (O1 to O60) are set low.

4. Enter display data.
5. Set the $\overline{CL}$ input high.

Data Transfer

Write display data by using a serial transfer.
Serial data is input in the shift register at the rising edge of a CLK input pulse.
When the LS input rises, display data is written in the latch.

Driver Output Control

1. To turn on or off driver outputs by using display data transferred into the shift register, set the $\overline{CL}$ input high and set the CHG input low.
2. To set all the driver outputs low, set the $\overline{CL}$ input low.
3. To set all the driver outputs high, set the $\overline{CL}$ input and CHG input high at a time.

Function Table

Shift register

Input			Shift Register Parallel Out					Output
CLK	DIN	LS	PO1	PO2	• • • •	PO59	PO60	DOUT
↑	H	L	H	PO1n	• • • •	PO58n	PO59n	PO59n
↑	L	L	L	PO1n	• • • •	PO58n	PO59n	PO59n
↓	X	L	PO1n	PO2n	• • • •	PO59n	PO60n	PO60n
↑	X	H	L	L	• • • •	L	L	L

X: Don't Care
PO1n to PO59n: PO1 to PO59 data just before CLOCK rises.

Register

Input		Shift Register Parallel Out	Latch Output
CLK	LS	POm	Om
X	↑	H	H
X	↑	L	L
X	↓	X	No Change
↑	H	L	L

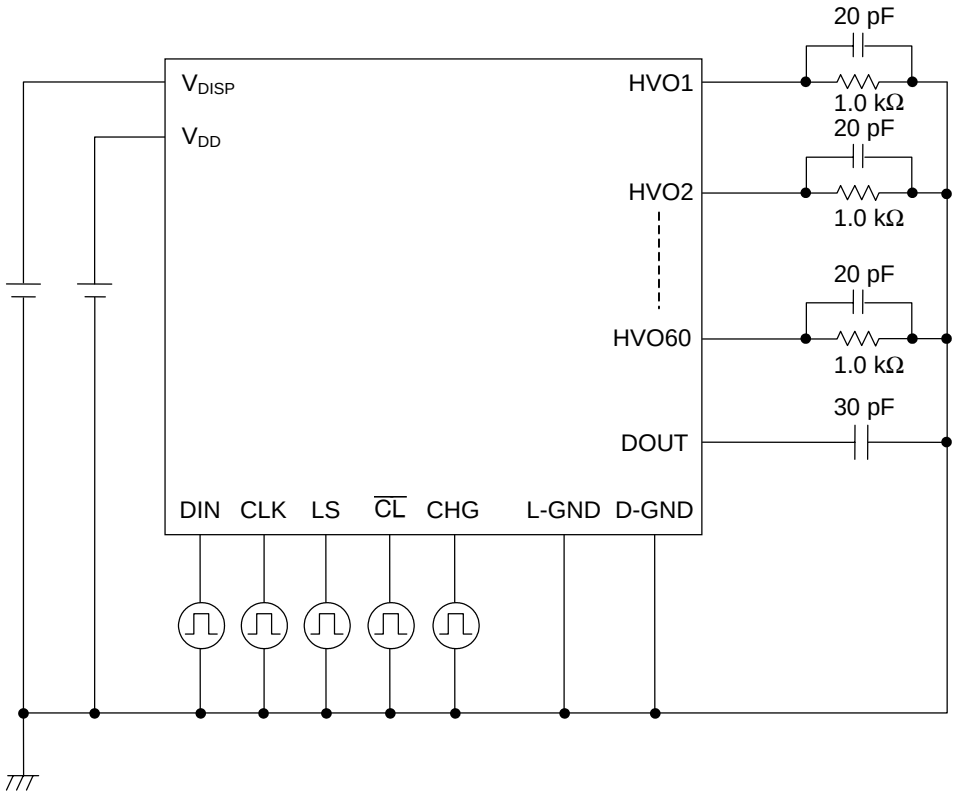
X: Don't Care, m: 1 to 60

Driver output

Input				Latch Output	Output
$\overline{CL}$	CHG	CLK	LS	Om	HVOm
H	L	X	X	H	H
H	L	X	X	L	L
H	H	X	X	X	H
L	X	X	X	X	L
X	X	↑	H	L	L

X: Don't Care, m: 1 to 60

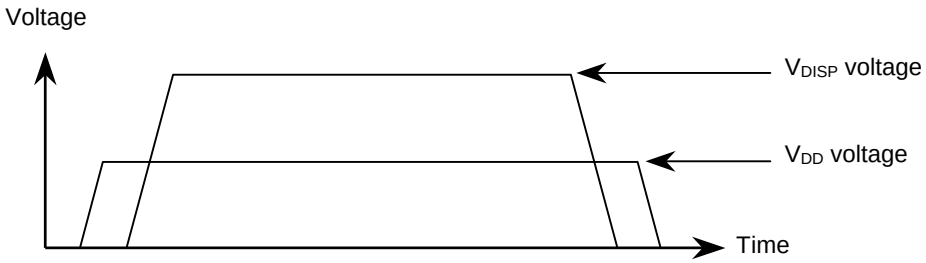
TEST CIRCUIT



NOTES ON POWER APPLICATION

Connect L-GND and G-GND pins externally to provide the equal potential.

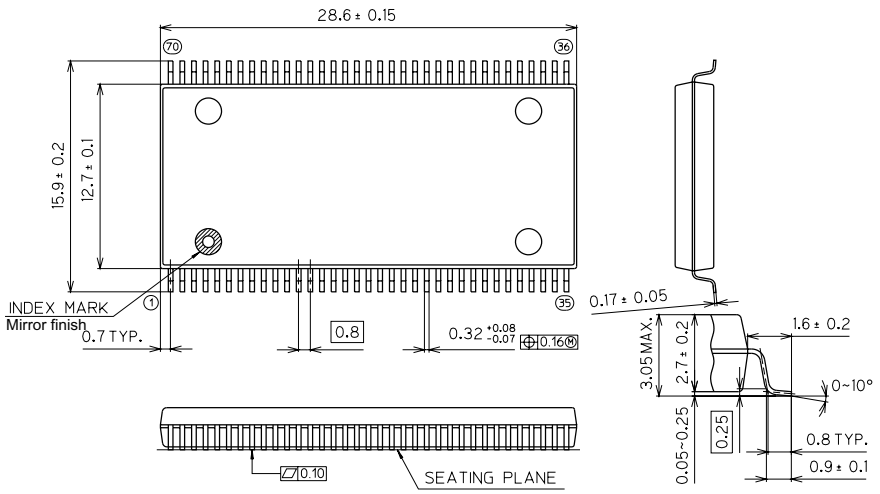
To prevent IC erroneous operation, turn on V_{DD} before turning on V_{DISP}, and turn off V_{DISP} before turning off V_{DD}.



PACKAGE DIMENSIONS

(Unit: mm)

SSOP70-P-500-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	2.15 TYP.
Rev. No./Last Revised	3/Dec. 5, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9261A-01	Jan. 22, 2002	–	–	Preliminary first edition
FEDL9261A-01	Mar. 28, 2002	1	1	Removed Preliminary classification.
				The following contents of “FEATURES” have been revised: • “Logic Supply Voltage (V_{CC})” to “Logic Supply Voltage (V_{DD})”. • “Drive Supply Voltage (V_{HV}): +60 V” to “Drive Supply Voltage (V_{DISP}): +20 to +60 V”.
		5	5	Rating and Unit of Parameter “Power Dissipation” in the table have been revised from 1.9 and mW to 1.47 and W, respectively.
				Partially changed the content of Note *3.
		7	7	Removed (Design Goal) from Parameter “Supply Current” in the two tables.
		12	12	Symbol “PO2n” has been changed to Symbol “PO1n” in Column “PO2” of Column “Shift Register Parallel Out”.
		13	13	The test circuit has been partially changed. “The logic power supply” and “the driver power supply” have been changed to V_{DD} and V_{DISP} in the sentence of “NOTES ON POWER APPLICATIONS”.
				Changed “V_{DISP} pin voltage” and “V_{DD} pin voltage” to “V_{DISP} voltage” and V_{DD} voltage” in the bottom figure.

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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