FEDL63295A-02

OKI Semiconductor

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ML63295A

4-Bit Microcontroller with Built-in 3072-Dot Matrix LCD Driver and Melody Circuit

GENERAL DESCRIPTION

The ML63295A is a CMOS 4-bit microcontroller that employs Oki's original CPU core nX-4/250.
The ML63295A operates on a power supply voltage of 6 V.
With built-in 3072-dot matrix LCD drivers (96 SEG. × 32 COM.), the ML63295A is suited for applications such as electronic dictionaries with an LCD.

FEATURES

• Extensive instruction set
  439 instructions:
    Transfer, rotate, increment/decrement, arithmetic operations, compare, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, jump, conditional branch, call/return, control

• Wide variety of addressing modes
  Indirect addressing mode for 4 types of data memory with current bank register, extra bank register, HL register and XY register
  Data memory bank internal direct addressing mode

• Processing speed
  2 clocks per machine cycle, with most instructions executed in 1 machine cycle
  Minimum instruction execution time : 61 μs (@ 32.768 kHz system clock)
  : 1 μs (@ 2 MHz system clock)

• Clock generation circuit
  Low-speed clock : Crystal oscillation or RC oscillation selected with mask option
  (30 kHz to 80 kHz)
  High-speed clock: Ceramic oscillation or RC oscillation selected with software
  (2 MHz max)

• Program memory space
  32 K words
  Basic instruction length is 16 bits/1word.

• Data memory space
  2048 nibbles

• External data memory space
  64 Kbytes (expandable furthermore by using the I/O ports)

• Stack level
  Call stack level : 16 levels
  Register stack level : 16 levels

• Ports

Input ports:

Selectable as input pull-up resistor/input pull-down resistor/high impedance input.

Output ports:

Selectable as P-channel open drain output/N-channel open drain output/high-impedance output/CMOS output.

I/O ports:

Selectable as input pull-up resistor/input pull-down resistor/high impedance input.
Selectable as P-channel open drain output/N-channel open drain output/high-impedance output/ CMOS output.

Can be interfaced with external peripherals that use a different power supply than this device uses.

Number of ports:

Input port	: 2 ports × 4 bits
Output port	: 6 ports × 4 bits
Input-output port	: 6 ports × 4 bits

• Melody output

Melody frequency	: 529 Hz to 2979 Hz
Tone length	: 63 varieties
Tempo	: 15 varieties
Melody data	: Stored in program memory
Buzzer driver signal output	: 4 kHz

• LCD driver

Number of segments	: 3072 Max. (96 SEG. × 32 COM.)
Duty	: Selectable as 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, 1/14, 1/16, 1/18, 1/20, 1/22, 1/24, 1/26, 1/28, 1/30, or 1/32 duty
Bias	: Selectable as 1/5 or 1/6 bias (regulator built-in)
Frame frequency	: ex. 64 Hz (at 1/32 duty), 128 Hz (at 1/16 duty), 256 Hz (at 1/8 duty), 512 Hz (at 1/4 duty), 1024 Hz (at 1/2 duty)
Contrast	: 16 levels adjustable
Display modes	: Selectable as all-ON mode/all-OFF mode/power down mode/normal display mode

• Multiplier/divider circuit

Multiplier	: (8 bits) × (8 bits) → Product (16 bits)
Divider	: (16 bits)/(8 bits) → Quotient (16 bits), Remainder (8 bits)

• System reset function

System reset through RESET pin
System reset by power-on detection
System reset by low-speed oscillation halt

• Battery check

Low-voltage supply check

The value of the judgment voltage is selected by the software (by setting the LD1 and LD0 bits of BLDCON).

LD1	LD0	Judgment voltage (V)	Remarks
1	0	4.5 ±0.1	Ta = 25°C
1	1	5.1 ±0.1	Ta = 25°C

• Timers and Counter

8-bit timer	: 2 Selectable as auto-reload mode/clock frequency measurement mode
Watchdog timer	: 1
100 Hz timer	: 1 Measurable in steps of 1/100 sec.
15-bit time-base counter	: 1 1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read

• Serial port

Mode	: Selectable as UART mode, synchronous mode
UART communication speed	: 1200 bps, 2400 bps, 4800 bps, 9600 bps
Clock frequency in synchronous mode	: Internal clock mode (32.768 kHz), External clock frequency
Data length	: 5 to 8 bits

• Shift register

Shift clock	: 1 × or 1/2 × system clock, external clock
Data length	: 8 bits

• Interrupt factors

External interrupt	: 5
Internal interrupt	: 12

• Operating temperature : –20 to +70°C

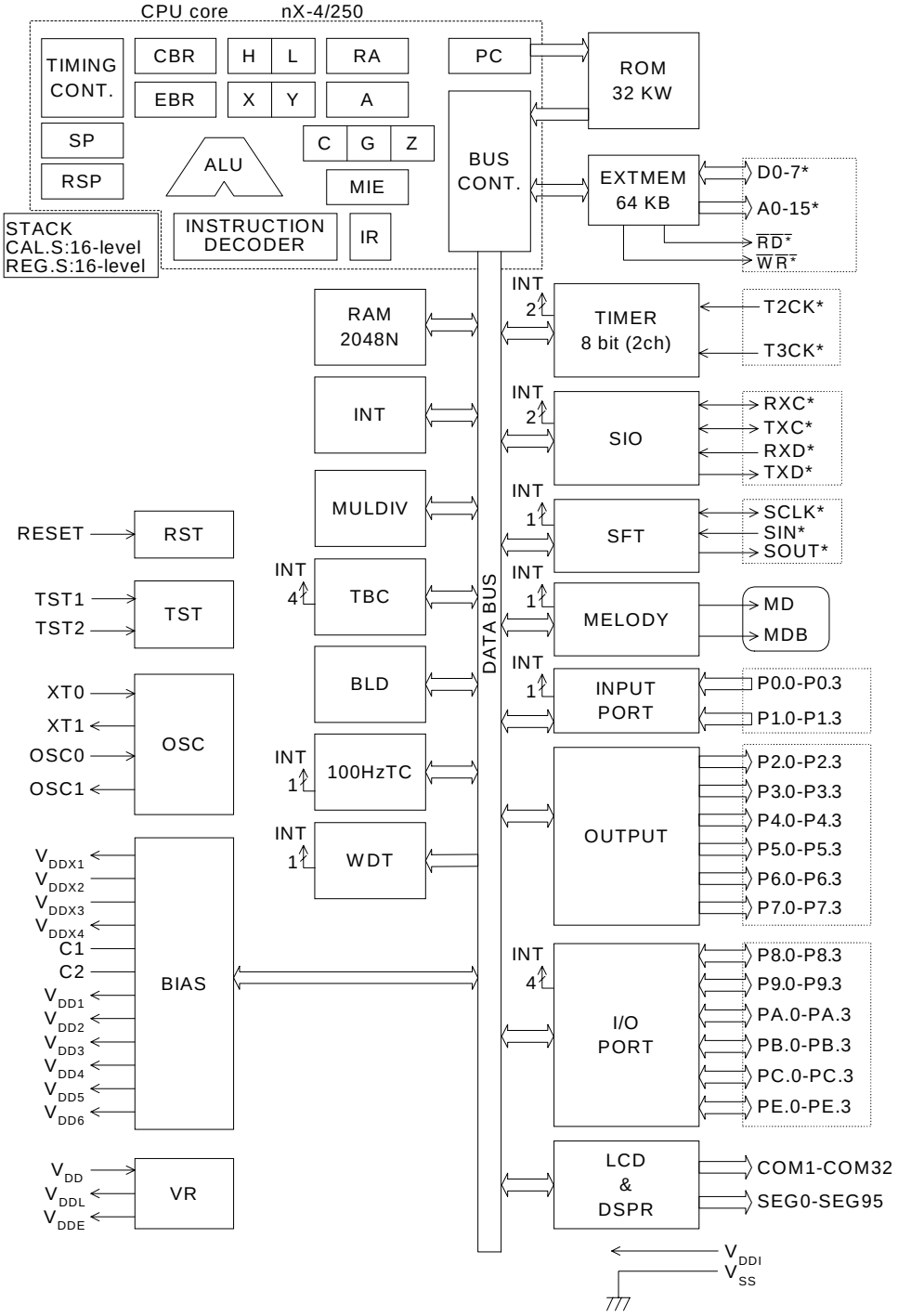
• Power supply voltage : 3.5 to 7.2 V

• Package:

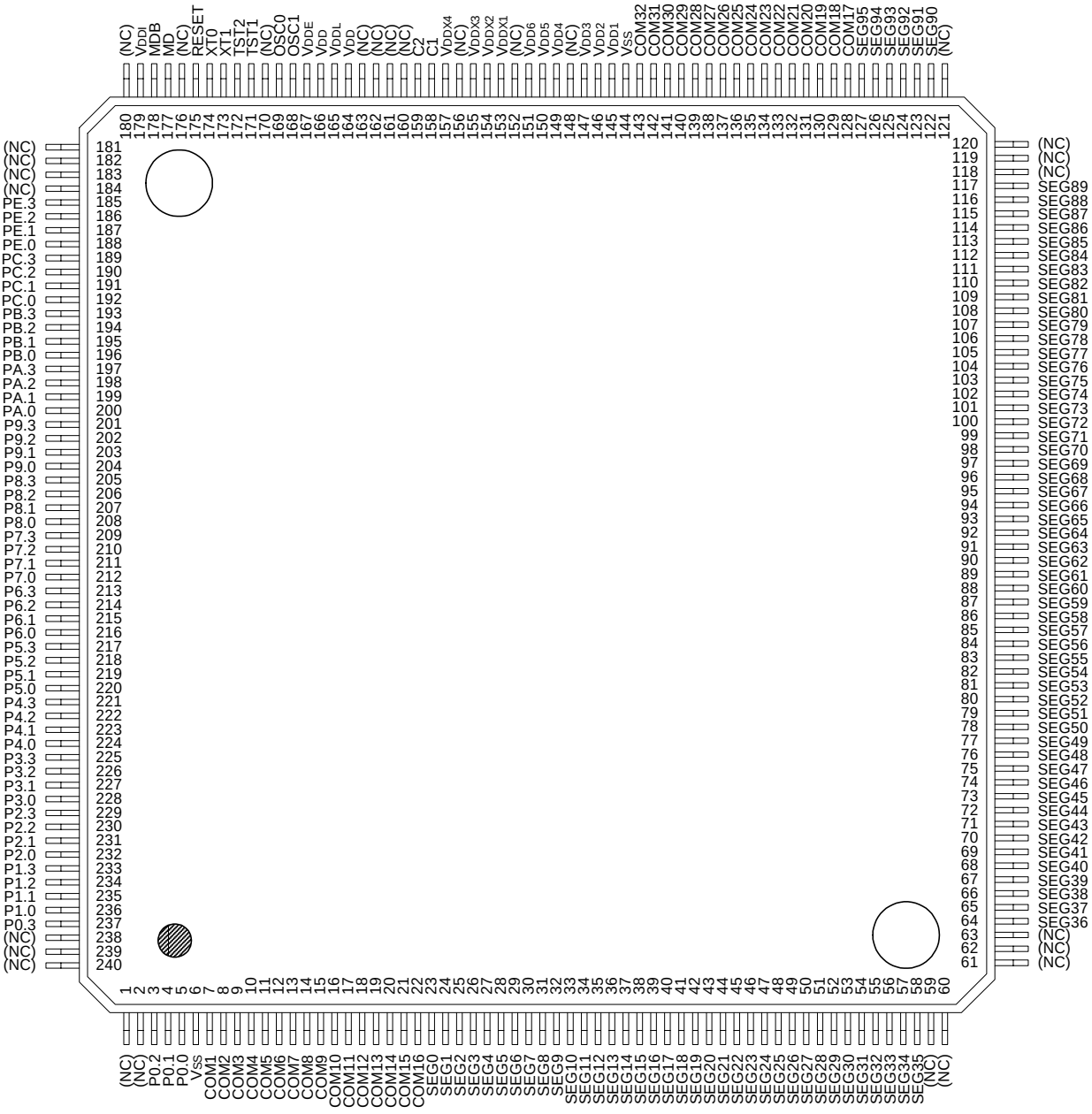
Chip (212 pads)	: (Product name: ML63295A-xxxWA)
240-pin plastic QFP (QFP240-P-3232-0.50-BK4)	: (Product name: ML63295A-xxxGA) ….under consideration xxx indicates a code number.

BLOCK DIAGRAM

Asterisks (*) indicate the port secondary functions. Signal names enclosed by chain lines (.....) indicate interface signals of the V_{DDI} power supply system. Signal names enclosed by ▭ indicates signals of the V_{DDE} power supply system.



PIN CONFIGURATION (TOP VIEW)

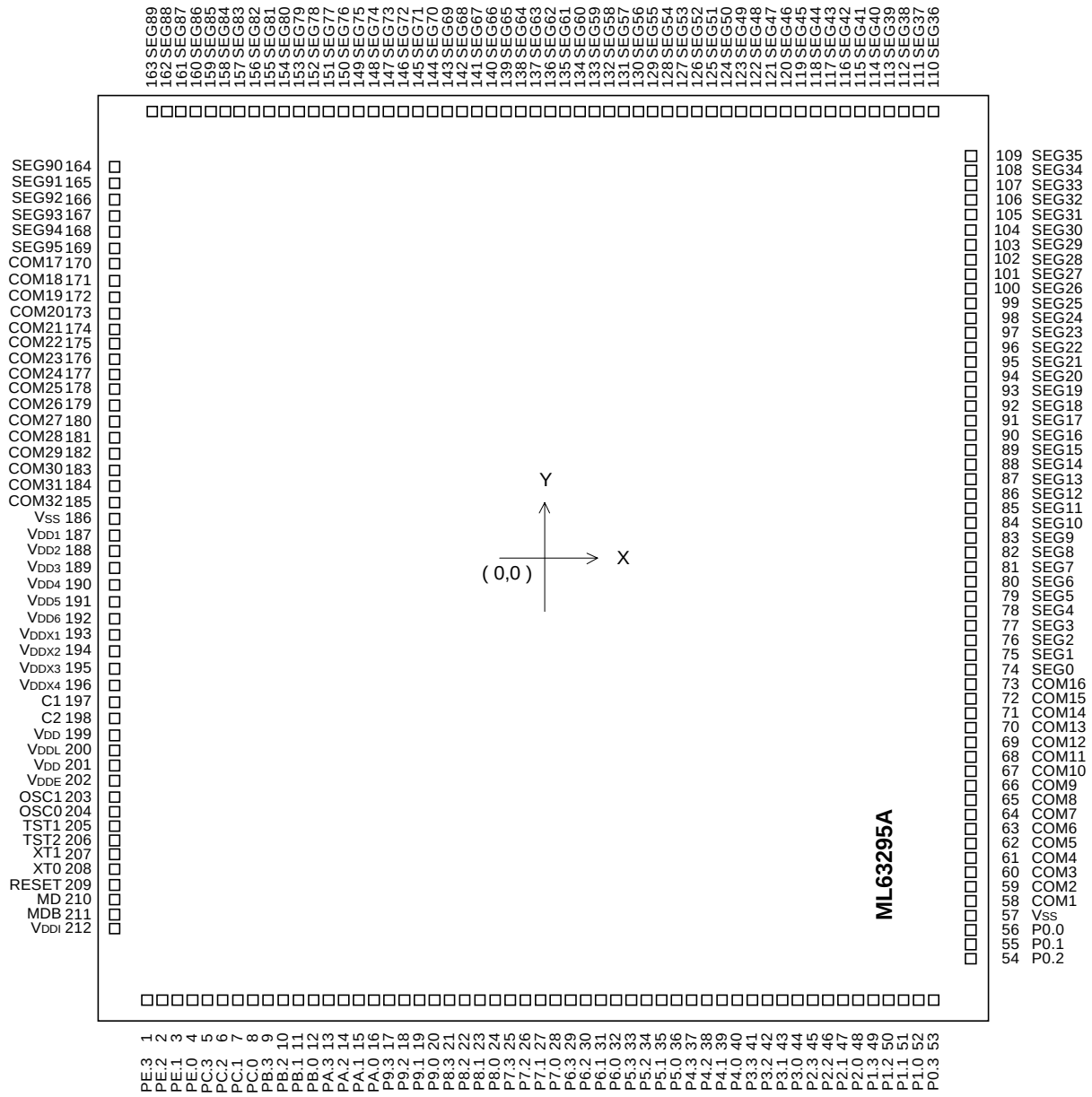


240-Pin Plastic QFP
(GA:QFP240-P-3232-0.50-BK4)

Note: Pins marked as (NC) are no-connection pins which are left open.

PAD CONFIGURATION

Pad Layout



Chip size	: 8.25 mm × 8.20 mm
Chip thickness	: 350 μm (280 μm: available as required)
Coordinate origin	: center of chip
Pad hole size	: 100 μm × 100 μm
Pad size	: 110 μm × 110 μm
Minimum pad pitch	: 120 μm

Note: The chip substrate voltage is V_{SS}.

Pad Coordinates

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)
1	PE.3	–3138	–3905
2	PE.2	–3018	–3905
3	PE.1	–2898	–3905
4	PE.0	–2778	–3905
5	PC.3	–2658	–3905
6	PC.2	–2538	–3905
7	PC.1	–2418	–3905
8	PC.0	–2298	–3905
9	PB.3	–2178	–3905
10	PB.2	–2058	–3905
11	PB.1	–1938	–3905
12	PB.0	–1818	–3905
13	PA.3	–1698	–3905
14	PA.2	–1578	–3905
15	PA.1	–1458	–3905
16	PA.0	–1338	–3905
17	P9.3	–1218	–3905
18	P9.2	–1098	–3905
19	P9.1	–978	–3905
20	P9.0	–858	–3905
21	P8.3	–738	–3905
22	P8.2	–618	–3905
23	P8.1	–498	–3905
24	P8.0	–378	–3905
25	P7.3	–258	–3905
26	P7.2	–138	–3905
27	P7.1	–18	–3905
28	P7.0	102	–3905
29	P6.3	222	–3905
30	P6.2	342	–3905
31	P6.1	462	–3905
32	P6.0	582	–3905
33	P5.3	702	–3905
34	P5.2	822	–3905
35	P5.1	942	–3905
36	P5.0	1062	–3905
37	P4.3	1182	–3905
38	P4.2	1302	–3905
39	P4.1	1422	–3905
40	P4.0	1542	–3905
41	P3.3	1662	–3905
42	P3.2	1782	–3905
43	P3.1	1902	–3905
44	P3.0	2022	–3905
45	P2.3	2142	–3905
46	P2.2	2262	–3905
47	P2.1	2382	–3905
48	P2.0	2502	–3905
49	P1.3	2622	–3905
50	P1.2	2742	–3905
51	P1.1	2862	–3905
52	P1.0	2982	–3905
53	P0.3	3102	–3905
54	P0.2	3965	–3281
55	P0.1	3965	–3161
56	P0.0	3965	–3041
57	V_{SS}	3965	–2907
58	COM1	3965	–2766
59	COM2	3965	–2646
60	COM3	3965	–2526
61	COM4	3965	–2406
62	COM5	3965	–2286
63	COM6	3965	–2166
64	COM7	3965	–2046
65	COM8	3965	–1926
66	COM9	3965	–1806
67	COM10	3965	–1686
68	COM11	3965	–1566
69	COM12	3965	–1446
70	COM13	3965	–1326
71	COM14	3965	–1206
72	COM15	3965	–1086
73	COM16	3965	–966
74	SEG0	3965	–846
75	SEG1	3965	–726
76	SEG2	3965	–606
77	SEG3	3965	–486
78	SEG4	3965	–366

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)
79	SEG5	3965	–246
80	SEG6	3965	–126
81	SEG7	3965	–6
82	SEG8	3965	114
83	SEG9	3965	234
84	SEG10	3965	354
85	SEG11	3965	474
86	SEG12	3965	594
87	SEG13	3965	714
88	SEG14	3965	834
89	SEG15	3965	954
90	SEG16	3965	1074
91	SEG17	3965	1194
92	SEG18	3965	1314
93	SEG19	3965	1434
94	SEG20	3965	1554
95	SEG21	3965	1674
96	SEG22	3965	1794
97	SEG23	3965	1914
98	SEG24	3965	2034
99	SEG25	3965	2154
100	SEG26	3965	2274
101	SEG27	3965	2394
102	SEG28	3965	2514
103	SEG29	3965	2634
104	SEG30	3965	2754
105	SEG31	3965	2874
106	SEG32	3965	2994
107	SEG33	3965	3114
108	SEG34	3965	3234
109	SEG35	3965	3354
110	SEG36	3185	3905
111	SEG37	3065	3905
112	SEG38	2945	3905
113	SEG39	2825	3905
114	SEG40	2705	3905
115	SEG41	2585	3905
116	SEG42	2465	3905
117	SEG43	2345	3905

Pad No.	Pad Name	X (μm)	Y (μm)
118	SEG44	2225	3905
119	SEG45	2105	3905
120	SEG46	1985	3905
121	SEG47	1865	3905
122	SEG48	1745	3905
123	SEG49	1625	3905
124	SEG50	1505	3905
125	SEG51	1385	3905
126	SEG52	1265	3905
127	SEG53	1145	3905
128	SEG54	1025	3905
129	SEG55	905	3905
130	SEG56	785	3905
131	SEG57	665	3905
132	SEG58	545	3905
133	SEG59	425	3905
134	SEG60	305	3905
135	SEG61	185	3905
136	SEG62	65	3905
137	SEG63	–55	3905
138	SEG64	–175	3905
139	SEG65	–295	3905
140	SEG66	–415	3905
141	SEG67	–535	3905
142	SEG68	–655	3905
143	SEG69	–775	3905
144	SEG70	–895	3905
145	SEG71	–1015	3905
146	SEG72	–1135	3905
147	SEG73	–1255	3905
148	SEG74	–1375	3905
149	SEG75	–1495	3905
150	SEG76	–1615	3905
151	SEG77	–1735	3905
152	SEG78	–1855	3905
153	SEG79	–1975	3905
154	SEG80	–2095	3905
155	SEG81	–2215	3905
156	SEG82	–2335	3905

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)
157	SEG83	–2455	3905
158	SEG84	–2575	3905
159	SEG85	–2695	3905
160	SEG86	–2815	3905
161	SEG87	–2935	3905
162	SEG88	–3055	3905
163	SEG89	–3175	3905
164	SEG90	–3965	3432
165	SEG91	–3965	3312
166	SEG92	–3965	3192
167	SEG93	–3965	3072
168	SEG94	–3965	2952
169	SEG95	–3965	2832
170	COM17	–3965	2712
171	COM18	–3965	2592
172	COM19	–3965	2472
173	COM20	–3965	2352
174	COM21	–3965	2232
175	COM22	–3965	2112
176	COM23	–3965	1992
177	COM24	–3965	1872
178	COM25	–3965	1752
179	COM26	–3965	1632
180	COM27	–3965	1512
181	COM28	–3965	1392
182	COM29	–3965	1272
183	COM30	–3965	1152
184	COM31	–3965	1032

Pad No.	Pad Name	X (μm)	Y (μm)
185	COM32	–3965	912
186	V_{SS}	–3965	730
187	V_{DD1}	–3965	580
188	V_{DD2}	–3965	430
189	V_{DD3}	–3965	280
190	V_{DD4}	–3965	130
191	V_{DD5}	–3965	–20
192	V_{DD6}	–3965	–170
193	V_{DDX1}	–3965	–320
194	V_{DDX2}	–3965	–470
195	V_{DDX3}	–3965	–620
196	V_{DDX4}	–3965	–770
197	C1	–3965	–920
198	C2	–3965	–1070
199	V_{DD}	–3965	–1220
200	V_{DDL}	–3965	–1370
201	V_{DD}	–3965	–1520
202	V_{DDE}	–3965	–1670
203	OSC1	–3965	–1924
204	OSC0	–3965	–2074
205	TST1	–3965	–2268
206	TST2	–3965	–2388
207	XT1	–3965	–2593
208	XT0	–3965	–2743
209	RESET	–3965	–2912
210	MD	–3965	–3120
211	MDB	–3965	–3240
212	V_{DDI}	–3965	–3392

PIN DESCRIPTIONS

The basic functions of each pin of the ML63295A are described in Table 1.
A symbol with a slash "/" denotes a pin that has a secondary function. Refer to Table 2 for secondary functions.
For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

Table 1 Pin Descriptions (Basic Functions)

Function	Symbol	Pin No.	Pad No.	Type	Description
Power Supply	V_{DD}	164, 166	199, 201	—	Positive power supply pin
	V_{SS}	6, 144	57, 186	—	Negative power supply pin
	V_{DD1}	145	187	—	Power supply pins for LCD bias voltage (internally generated): Capacitors (1.0 μF) should be connected between these pins and V_{SS}.
	V_{DD2}	146	188		
	V_{DD4}	149	190		
	V_{DD5}	150	191		
	V_{DD6}	151	192		
	V_{DDX1}	153	193	—	Positive power supply for low-speed oscillation.
	V_{DD3}	147	189	—	Power supply pins for LCD bias voltage generation: Capacitors (1.0 μF) should be connected between these pins and V_{SS}.
	V_{DDX4}	157	196		
	C1	158	197	—	Capacitor connection pins for LCD bias voltage generation: A capacitor (1.0 μF) should be connected between C1 and C2, and between V_{DDX2} and V_{DDX3}.
	C2	159	198		
	V_{DDX2}	154	194	—	
	V_{DDX3}	155	195		
	V_{DDI}	179	212	—	Positive power supply pin for external interface (Power supply for input, output, and input-output ports)
	V_{DDL}	165	200	—	Positive power supply pin for internal logic (internally generated): A capacitor (0.1 μF) should be connected between this pin and V_{SS}.
	V_{DDE}	167	202	—	Constant voltage output pin: A capacitor (1.0 μF) should be connected between this pin and V_{SS}.
Oscillation	XT0	174	208	I	Low-speed clock oscillation pins: An option for using crystal oscillation or RC oscillation is chosen by the mask option. If the crystal oscillation is chosen, a crystal should be connected between XT0 and XT1, and capacitor (C_G) should be connected between XT0 and V_{SS}. If the RC oscillation is chosen, external oscillation resistor (R_{OSL}) should be connected between XT0 and XT1.
	XT1	173	207	O	

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
Oscillation	OSC0	169	204	I	High-speed clock oscillation pins: A ceramic resonator and capacitors (C_{L0}, C_{L1}) or external oscillation resistor (R_{OSH}) should be connected to these pins.
	OSC1	168	203	O	
Test	TST1	171	205	I	Input pins for testing. A pull-down resistor is internally connected to these pins.
	TST2	172	206	I	
Reset	RESET	175	209	I	System reset input pin. Setting this pin to “H” level puts this device into a reset state. Then, setting this pin to “L” level starts executing an instruction from address 0000H. A pull-down resistor is internally connected to this pin.
Melody	MD	177	210	O	Melody output pin (non-inverted output)
	MDB	178	211	O	Melody output pin (inverted output)

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
Port	P0.0/INT5	5	56	I	4-bit input ports: Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.
	P0.1/INT5	4	55		
	P0.2/INT5	3	54		
	P0.3/INT5	237	53		
	P1.0/INT5	236	52	I	
	P1.1/INT5	235	51		
	P1.2/INT5	234	50		
	P1.3/INT5	233	49		
	P2.0	232	48	O	4-bit output ports: P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P2.1	231	47		
	P2.2	230	46		
	P2.3	229	45		
	P3.0	228	44	O	
	P3.1	227	43		
	P3.2	226	42		
	P3.3	225	41		
	P4.0/A0	224	40	O	
	P4.1/A1	223	39		
	P4.2/A2	222	38		
	P4.3/A3	221	37		
	P5.0/A4	220	36	O	
	P5.1/A5	219	35		
	P5.2/A6	218	34		
	P5.3/A7	217	33		
	P6.0/A8	216	32	O	
	P6.1/A9	215	31		
	P6.2/A10	214	30		
	P6.3/A11	213	29		
	P7.0/A12	212	28	O	
	P7.1/A13	211	27		
	P7.2/A14	210	26		
	P7.3/A15	209	25		
	P8.0/$\overline{RD}$	208	24	I/O	4-bit input-output ports: In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit. In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	P8.1/$\overline{WR}$	207	23		
	P8.2	206	22		
	P8.3/INT4	205	21		
	P9.0/D0	204	20	I/O	
	P9.1/D1	203	19		
	P9.2/D2	202	18		
	P9.3/D3	201	17		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
Port	PA.0/D4	200	16	I/O	4-bit input-output ports: In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit. In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.
	PA.1/D5	199	15		
	PA.2/D6	198	14		
	PA.3/D7	197	13		
	PB.0/INT0	196	12	I/O	
	PB.1/INT0	195	11		
	PB.2/INT0/ T2CK	194	10		
	PB.3/INT0/ T3CK	193	9		
	PC.0/INT1/ RXD	192	8	I/O	
	PC.1/INT1/ TXC	191	7		
	PC.2/INT1/ RXC	190	6		
	PC.3/INT1/ TXD	189	5		
	PE.0/SIN	188	4	I/O	
	PE.1/SOUT	187	3		
	PE.2/SCLK	186	2		
	PE.3/INT2	185	1		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
LCD	COM1	7	58	O	LCD common signal output pins
	COM2	8	59		
	COM3	9	60		
	COM4	10	61		
	COM5	11	62		
	COM6	12	63		
	COM7	13	64		
	COM8	14	65		
	COM9	15	66		
	COM10	16	67		
	COM11	17	68		
	COM12	18	69		
	COM13	19	70		
	COM14	20	71		
	COM15	21	72		
	COM16	22	73		
	COM17	128	170		
	COM18	129	171		
	COM19	130	172		
	COM20	131	173		
	COM21	132	174		
	COM22	133	175		
	COM23	134	176		
	COM24	135	177		
	COM25	136	178		
	COM26	137	179		
	COM27	138	180		
	COM28	139	181		
	COM29	140	182		
	COM30	141	183		
	COM31	142	184		
	COM32	143	185		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
LCD	SEG0	23	74	O	LCD segment signal output pins
	SEG1	24	75		
	SEG2	25	76		
	SEG3	26	77		
	SEG4	27	78		
	SEG5	28	79		
	SEG6	29	80		
	SEG7	30	81		
	SEG8	31	82		
	SEG9	32	83		
	SEG10	33	84		
	SEG11	34	85		
	SEG12	35	86		
	SEG13	36	87		
	SEG14	37	88		
	SEG15	38	89		
	SEG16	39	90		
	SEG17	40	91		
	SEG18	41	92		
	SEG19	42	93		
	SEG20	43	94		
	SEG21	44	95		
	SEG22	45	96		
	SEG23	46	97		
	SEG24	47	98		
	SEG25	48	99		
	SEG26	49	100		
	SEG27	50	101		
	SEG28	51	102		
	SEG29	52	103		
	SEG30	53	104		
	SEG31	54	105		
	SEG32	55	106		
	SEG33	56	107		
	SEG34	57	108		
	SEG35	58	109		
	SEG36	64	110		
	SEG37	65	111		
	SEG38	66	112		
	SEG39	67	113		
	SEG40	68	114		
	SEG41	69	115		
	SEG42	70	116		
	SEG43	71	117		
	SEG44	72	118		
	SEG45	73	119		
	SEG46	74	120		

Table 1 Pin Descriptions (Basic Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
LCD	SEG47	75	121	O	LCD segment signal output pins
	SEG48	76	122		
	SEG49	77	123		
	SEG50	78	124		
	SEG51	79	125		
	SEG52	80	126		
	SEG53	81	127		
	SEG54	82	128		
	SEG55	83	129		
	SEG56	84	130		
	SEG57	85	131		
	SEG58	86	132		
	SEG59	87	133		
	SEG60	88	134		
	SEG61	89	135		
	SEG62	90	136		
	SEG63	91	137		
	SEG64	92	138		
	SEG65	93	139		
	SEG66	94	140		
	SEG67	95	141		
	SEG68	96	142		
	SEG69	97	143		
	SEG70	98	144		
	SEG71	99	145		
	SEG72	100	146		
	SEG73	101	147		
	SEG74	102	148		
	SEG75	103	149		
	SEG76	104	150		
	SEG77	105	151		
	SEG78	106	152		
	SEG79	107	153		
	SEG80	108	154		
	SEG81	109	155		
	SEG82	110	156		
	SEG83	111	157		
	SEG84	112	158		
	SEG85	113	159		
	SEG86	114	160		
	SEG87	115	161		
	SEG88	116	162		
	SEG89	117	163		
	SEG90	122	164		
	SEG91	123	165		
	SEG92	124	166		
	SEG93	125	167		
	SEG94	126	168		
	SEG95	127	169		

Table 2 shows the secondary functions of each pin of the ML63295A.

Table 2 Pin Descriptions (Secondary Functions)

Function	Symbol	Pin No.	Pad No.	Type	Description
External Interrupt	PB.0/INT0	196	12	I	External 0 interrupt input pins The change of input signal level causes an interrupt to occur. The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit.
	PB.1/INT0	195	11		
	PB.2/INT0	194	10		
	PB.3/INT0	193	9		
	PC.0/INT1	192	8	I	External 1 interrupt input pins The change of input signal level causes an interrupt to occur. The Port C Interrupt Enable register (PCIE) enables or disables an interrupt for each bit.
	PC.1/INT1	191	7		
	PC.2/INT1	190	6		
	PC.3/INT1	189	5		
	PE.3/INT2	185	1	I	External 2 interrupt input pin The change of input signal level causes an interrupt to occur.
	P8.3/INT4	205	21	I	External 4 interrupt input pin The change of input signal level causes an interrupt to occur.
	P0.0/INT5	5	56	I	External 5 interrupt input pins The change of input signal level causes an interrupt to occur. The Port 0 Interrupt Enable register (P0IE) and Port 1 Interrupt Enable register (P1IE) enable or disable an interrupt for each bit.
	P0.1/INT5	4	55		
	P0.2/INT5	3	54		
	P0.3/INT5	237	53		
	P1.0/INT5	236	52		
	P1.1/INT5	235	51		
	P1.2/INT5	234	50		
	P1.3/INT5	233	49		
Timer	PB.2/T2CK	194	10	I	External clock input pin for timer 2
	PB.3/T3CK	193	9	I	External clock input pin for timer 3

Table 2 Pin Descriptions (Secondary Functions) (continued)

Function	Symbol	Pin No.	Pad No.	Type	Description
Serial Port	PC.0/RXD	192	8	I	Serial port receive data input pin
	PC.1/TXC	191	7	I/O	Sync serial port clock input-output pin Transmit clock output when this device is used as a master processor. Transmit clock input when this device is used as a slave processor.
	PC.2/RXC	190	6	I/O	Sync serial port clock input-output pin Receive clock output when this device is used as a master processor. Receive clock input when this device is used as a slave processor.
	PC.3/TXD	189	5	O	Serial port transmit data output pin
Shift Register	PE.0/SIN	188	4	I	Shift register receive data input pin
	PE.1/SOUT	187	3	O	Shift register transmit data output pin
	PE.2/SCLK	186	2	I/O	Shift register clock input-output pin. Clock output when this device is used as a master processor. Clock input when this device is used as a slave processor.
External Memory	P4.0/A0	224	40	O	Address output bus for external memory
	P4.1/A1	223	39		
	P4.2/A2	222	38		
	P4.3/A3	221	37		
	P5.0/A4	220	36		
	P5.1/A5	219	35		
	P5.2/A6	218	34		
	P5.3/A7	217	33		
	P6.0/A8	216	32		
	P6.1/A9	215	31		
	P6.2/A10	214	30		
	P6.3/A11	213	29		
	P7.0/A12	212	28		
	P7.1/A13	211	27		
	P7.2/A14	210	26		
	P7.3/A15	209	25		
	P9.0/D0	204	20	I/O	Data bus for external memory
	P9.1/D1	203	19		
	P9.2/D2	202	18		
	P9.3/D3	201	17		
	PA.0/D4	200	16		
	PA.1/D5	199	15		
	PA.2/D6	198	14		
	PA.3/D7	197	13		
	P8.0/$\overline{RD}$	208	24	O	Read signal output pin for external memory (negative logic)
	P8.1/$\overline{WR}$	207	23	O	Write signal output pin for external memory (negative logic)

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{DD1}	Ta = 25°C	–0.3 to +1.5	V
Power Supply Voltage 2	V_{DD2}	Ta = 25°C	–0.3 to +2.5	V
Power Supply Voltage 3	V_{DD3}	Ta = 25°C	–0.3 to +6.5	V
Power Supply Voltage 4	V_{DD4}	Ta = 25°C	–0.3 to +4.5	V
Power Supply Voltage 5	V_{DD5}	Ta = 25°C	–0.3 to +5.5	V
Power Supply Voltage 6	V_{DD6}	Ta = 25°C	–0.3 to +6.5	V
Power Supply Voltage 7	V_{DDX1}	Ta = 25°C	–0.3 to +2.0	V
Power Supply Voltage 8	V_{DDX4}	Ta = 25°C	–0.3 to +6.5	V
Power Supply Voltage 9	V_{DD}	Ta = 25°C	–0.3 to +7.5	V
Power Supply Voltage 10	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 11	V_{DDL}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 12	V_{DDE}	Ta = 25°C	–0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD1} output, Ta = 25°C	–0.3 to V_{DD1} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DD2} output, Ta = 25°C	–0.3 to V_{DD2} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DD3} output, Ta = 25°C	–0.3 to V_{DD3} + 0.3	V
Output Voltage 4	V_{OUT4}	V_{DD4} output, Ta = 25°C	–0.3 to V_{DD4} + 0.3	V
Output Voltage 5	V_{OUT5}	V_{DD5} output, Ta = 25°C	–0.3 to V_{DD5} + 0.3	V
Output Voltage 6	V_{OUT6}	V_{DD6} output, Ta = 25°C	–0.3 to V_{DD6} + 0.3	V
Output Voltage 7	V_{OUT7}	V_{DDX1} output, Ta = 25°C	–0.3 to V_{DDX1} + 0.3	V
Output Voltage 8	V_{OUT8}	V_{DDX4} output, Ta = 25°C	–0.3 to V_{DDX4} + 0.3	V
Output Voltage 9	V_{OUT11}	V_{DD} output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output Voltage 10	V_{OUT12}	V_{DDI} output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 11	V_{OUT13}	V_{DDE} output, Ta = 25°C	–0.3 to V_{DDE} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

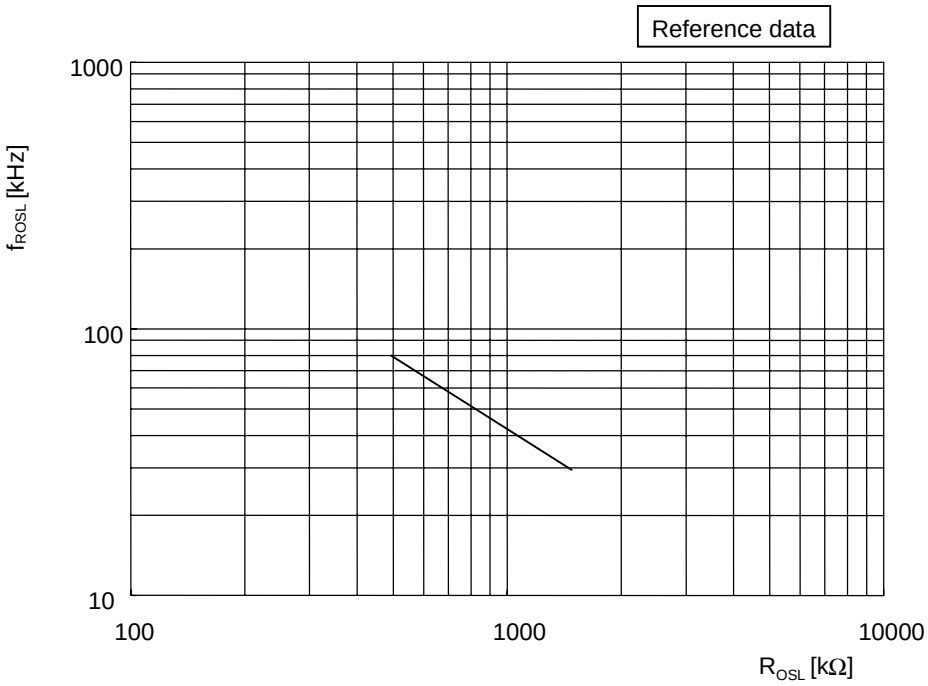
RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V)

Parameter	Symbol	Condition		Range	Unit
Operating Temperature	T_{OP}	—		–20 to +70	°C
Operating Voltage	V_{DD}	—		3.5 to 7.2	V
	V_{DDI}	—		1.8 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	C_G = 5 to 25 pF		32.768 to 76.8	kHz
Low-speed RC Oscillation Frequency	f_{ROSL}	R_{OSL} = 1.5 MΩ		32 k ±30%	Hz
		R_{OSL} = 700 kΩ		60 k ±30%	
		R_{OSL} = 500 kΩ		80 k ±30%	
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 3.5 to 7.2 V		200 k to 2 M	Hz
High-speed RC Oscillation Frequency	f_{ROSH}	V_{DD} = 3.5 to 7.2 V	R_{OSH} = 100 kΩ	700 k ±30%	Hz
			R_{OSH} = 75 kΩ	1 M ±30%	
			R_{OSH} = 51 kΩ	1.35 M ±30%	
			R_{OSH} = 30 kΩ	2 M ±30%	

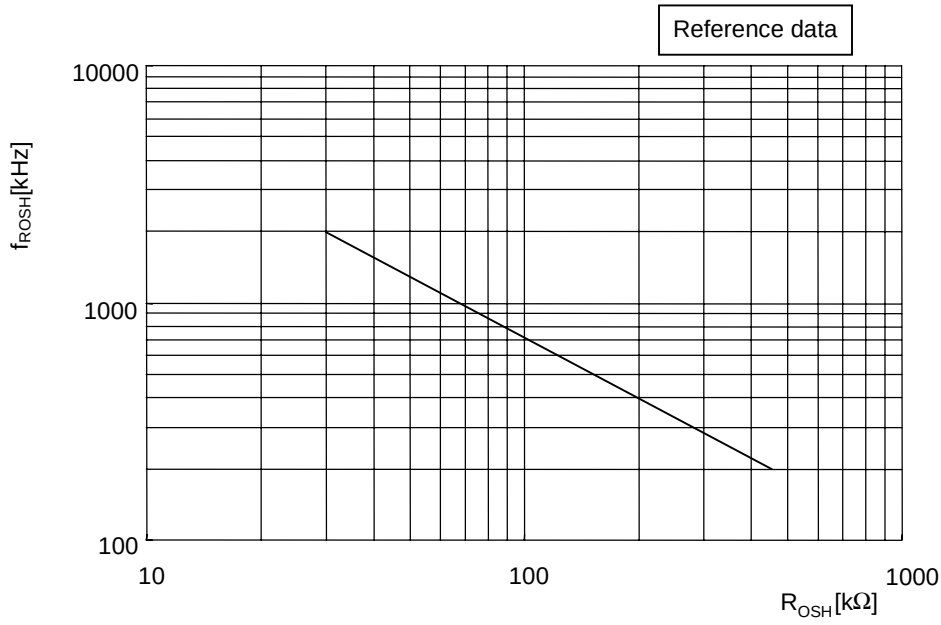
Typical characteristics of low-speed RC oscillation

(V_{DD} = 6.0 V, V_{DDI} = 3.0 V)



Typical characteristics of high-speed RC oscillation

(V_{DD} = 6.0 V, V_{DDI} = 3.0 V)



ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD} = 3.5 to 7.2 V, V_{DDI} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DDE} Voltage	V_{DDE}	I_{OUT} = 0 to 15 mA, Ta = 25°C	2.7	3.0	3.3	V	1
V_{DDE} Voltage Temperature Deviation	ΔV_{DDE}	—	—	–4.0	—	mV/°C	
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillation stopped	1.0	1.5	2.0	V	
		During operation at high-speed clock oscillation (V_{DD} = 3.5 to 7.2 V)	1.2	—	3.3		
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	3.5	—	—		
Crystal Oscillation Hold Voltage	V_{HOLD}	—	3.5	—	—		
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External RC Oscillator Capacitance	C_G	—	5	—	25	pF	
Internal RC Oscillator Capacitance	C_D	—	20	25	30		
External Ceramic Oscillator Capacitance	C_{L0}, C_{L1}	CSA2.00MG (Murata MFG.-make) used V_{DDE} = 3.0 V	—	30	—		
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16		
POR Voltage	V_{POR1}	V_{DD} = 6.0 V	0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD} = 6.0 V	2.0	—	6.0		
BLD Judgment Voltage	V_{BLDC}	LD1 = 1, LD0 = 1, Ta = 25°C	5.00	5.10	5.20	V	—
		LD1 = 1, LD0 = 0, Ta = 25°C	4.40	4.50	4.60		
BLD Judgment Voltage Temperature Deviation	ΔV_{BLDC}	V_{BLDC} = 5.10 V (LD1 = 1, LD0 = 1)	—	–3.5	—	mV/°C	
		V_{BLDC} = 4.50 V (LD1 = 1, LD0 = 0)	—	–2.3	—		

Notes:
1. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.
2. "POR" denotes Power On Reset.
3. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}
4. "V_{POR2}" indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD}.

DC Characteristics (2)

(V_{DD} = 6.0 V, V_{DDI} = 3.0 V, V_{SS} = 0 V, 1/6 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU in HALT state, LCD is being driven, no panel load (Crystal oscillation: 32.768 kHz) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	11.0	14.5	µA	1
			Ta = –20 to +70°C	—	11.0	19.5		
		CPU in HALT state, LCD is being driven, no panel load (RC oscillation: R_{OSL} = 1.5 MΩ) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	14.5	18.0		
			Ta = –20 to +70°C	—	14.5	23.0		
Supply Current 2	I_{DD2}	CPU in HALT state, LCD in Power Down mode (Crystal oscillation: 32.768 kHz) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	4.0	5.0		
			Ta = –20 to +70°C	—	4.0	6.5		
		CPU in HALT state, LCD in Power Down mode (RC oscillation: R_{OSL} = 1.5 MΩ) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	7.0	8.0		
			Ta = –20 to +70°C	—	7.0	9.5		
Supply Current 3	I_{DD3}	CPU operating at low speed, LCD is being driven, no panel load (Crystal oscillation: 32.768 kHz) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	20.5	29.0		
			Ta = –20 to +70°C	—	20.5	34.0		
		CPU operating at low speed, LCD is being driven, no panel load (RC oscillation: R_{OSL} = 1.5 MΩ) (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	24.5	33.0		
			Ta = –20 to +70°C	—	24.5	38.0		
Supply Current 4	I_{DD4}	CPU operating at high-speed oscillation (1 MHz RC oscillation, R_{OSH} = 75 kΩ)		—	1100	1700		
Supply Current 5	I_{DD5}	CPU operating at high-speed oscillation (2 MHz ceramic oscillation)		—	1500	2000		

DC Characteristics (3)

(V_{DD} = 3.5 to 7.2 V, V_{DDI} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD6} Voltage	V_{DD6}	1/6 bias, 1/5 bias	4.0	4.1	4.2	V	1
V_{DD5} Voltage	V_{DD5}	1/6 bias	Typ.–0.1	5/6 × V_{DD6}	Typ.+0.1		
		1/5 bias	Typ.–0.1	4/5 × V_{DD6}	Typ.+0.1		
V_{DD4} Voltage	V_{DD4}	1/6 bias	Typ.–0.1	4/6 × V_{DD6}	Typ.+0.1		
		1/5 bias	Typ.–0.1	3/5 × V_{DD6}	Typ.+0.1		
V_{DD2} Voltage	V_{DD2}	1/6 bias	Typ.–0.1	2/6 × V_{DD6}	Typ.+0.1		
		1/5 bias	Typ.–0.1	2/5 × V_{DD6}	Typ.+0.1		
V_{DD1} Voltage	V_{DD1}	1/6 bias	Typ.–0.1	1/6 × V_{DD6}	Typ.+0.1		
		1/5 bias	Typ.–0.1	1/5 × V_{DD6}	Typ.+0.1		

Note: "V_{DD6}" changes in the range from 4.10 to 6.14 V (Typ. value) according to the value of Display Contrast register (DSPCNT).

(V_{DD} = 3.5 to 7.2 V, V_{DDI} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DDE} Voltage Temperature Deviation	ΔV_{DDE}	—	—	–4.0	—	mV/°C	1
V_{DD6} Voltage	V_{DD6}	1/6 bias, 1/5 bias	3.6	4.1	4.6	V	
V_{DD5} Voltage	V_{DD5}	1/6 bias	Typ.–0.5	5/6 × V_{DD6}	Typ.+0.5		
		1/5 bias	Typ.–0.5	4/5 × V_{DD6}	Typ.+0.5		
V_{DD4} Voltage	V_{DD4}	1/6 bias	Typ.–0.5	4/6 × V_{DD6}	Typ.+0.5		
		1/5 bias	Typ.–0.5	3/5 × V_{DD6}	Typ.+0.5		
V_{DD2} Voltage	V_{DD2}	1/6 bias	Typ.–0.5	2/6 × V_{DD6}	Typ.+0.5		
		1/5 bias	Typ.–0.5	2/5 × V_{DD6}	Typ.+0.5		
V_{DD1} Voltage	V_{DD1}	1/6 bias	Typ.–0.5	1/6 × V_{DD6}	Typ.+0.5		
		1/5 bias	Typ.–0.5	1/5 × V_{DD6}	Typ.+0.5		

Note: "V_{DD6}" changes in the range from 4.10 to 6.14 V (Typ. value) according to the value of Display Contrast register (DSPCNT).

• Contrast voltage (V_{DD6} voltage)

Ta = 25°C, V_{DD6} = 4.1 V (Typ.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.1	—	Light
1H	0	0	0	1	Typ.–0.1	4.2	Typ.+0.1	
2H	0	0	1	0	Typ.–0.1	4.3	Typ.+0.1	
3H	0	0	1	1	Typ.–0.1	4.4	Typ.+0.1	
4H	0	1	0	0	Typ.–0.1	4.5	Typ.+0.1	
5H	0	1	0	1	Typ.–0.1	4.62	Typ.+0.1	
6H	0	1	1	0	Typ.–0.1	4.74	Typ.+0.1	
7H	0	1	1	1	Typ.–0.1	4.86	Typ.+0.1	
8H	1	0	0	0	Typ.–0.1	5.00	Typ.+0.1	
9H	1	0	0	1	Typ.–0.1	5.14	Typ.+0.1	
0AH	1	0	1	0	Typ.–0.1	5.29	Typ.+0.1	
0BH	1	0	1	1	Typ.–0.1	5.44	Typ.+0.1	
0CH	1	1	0	0	Typ.–0.1	5.60	Typ.+0.1	
0DH	1	1	0	1	Typ.–0.1	5.77	Typ.+0.1	
0EH	1	1	1	0	Typ.–0.1	5.95	Typ.+0.1	
0FH	1	1	1	1	Typ.–0.1	6.14	Typ.+0.1	Dark

Ta = 25°C, V_{DD6} = 4.0 V (Min.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.0	—	Light
1H	0	0	0	1	Typ.–0.1	4.1	Typ.+0.1	
2H	0	0	1	0	Typ.–0.1	4.2	Typ.+0.1	
3H	0	0	1	1	Typ.–0.1	4.3	Typ.+0.1	
4H	0	1	0	0	Typ.–0.1	4.4	Typ.+0.1	
5H	0	1	0	1	Typ.–0.1	4.52	Typ.+0.1	
6H	0	1	1	0	Typ.–0.1	4.64	Typ.+0.1	
7H	0	1	1	1	Typ.–0.1	4.76	Typ.+0.1	
8H	1	0	0	0	Typ.–0.1	4.90	Typ.+0.1	
9H	1	0	0	1	Typ.–0.1	5.04	Typ.+0.1	
0AH	1	0	1	0	Typ.–0.1	5.19	Typ.+0.1	
0BH	1	0	1	1	Typ.–0.1	5.34	Typ.+0.1	
0CH	1	1	0	0	Typ.–0.1	5.50	Typ.+0.1	
0DH	1	1	0	1	Typ.–0.1	5.67	Typ.+0.1	
0EH	1	1	1	0	Typ.–0.1	5.85	Typ.+0.1	
0FH	1	1	1	1	Typ.–0.1	6.04	Typ.+0.1	Dark

• Contrast voltage (V_{DD6} voltage)

Ta = 25°C, V_{DD6} = 4.2 V (Max.)

DSPCNT					V_{DD6} Voltage (V)			Display Contrast
CN0 to CN3	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	—	4.2	—	Light
1H	0	0	0	1	Typ.–0.1	4.3	Typ.+0.1	
2H	0	0	1	0	Typ.–0.1	4.4	Typ.+0.1	
3H	0	0	1	1	Typ.–0.1	4.5	Typ.+0.1	
4H	0	1	0	0	Typ.–0.1	4.6	Typ.+0.1	
5H	0	1	0	1	Typ.–0.1	4.72	Typ.+0.1	
6H	0	1	1	0	Typ.–0.1	4.84	Typ.+0.1	
7H	0	1	1	1	Typ.–0.1	4.96	Typ.+0.1	
8H	1	0	0	0	Typ.–0.1	5.10	Typ.+0.1	
9H	1	0	0	1	Typ.–0.1	5.24	Typ.+0.1	
0AH	1	0	1	0	Typ.–0.1	5.39	Typ.+0.1	
0BH	1	0	1	1	Typ.–0.1	5.54	Typ.+0.1	
0CH	1	1	0	0	Typ.–0.1	5.70	Typ.+0.1	
0DH	1	1	0	1	Typ.–0.1	5.87	Typ.+0.1	
0EH	1	1	1	0	Typ.–0.1	6.05	Typ.+0.1	
0FH	1	1	1	1	Typ.–0.1	6.24	Typ.+0.1	Dark

DC Characteristics (4)

(V_{DD} = 6.0 V, V_{DDI} = V_{DDE} = 3.0 V, V_{DD1} = 1.0 V, V_{DD2} = 2.0 V, V_{DD3} = 3.0 V, V_{DD4} = 4.0 V, V_{DD5} = 5.0 V, V_{DD6} = 6.0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P2.0 to P2.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	I_{OH1}	$V_{OH1} = V_{DDI} - 0.5$ V	V_{DDI} = 3.0 V	–6.0	–3.5	–1.0	mA	2
			V_{DDI} = 5.0 V	–8.5	–5.0	–1.5		
	I_{OL1}	V_{OL1} = 0.5 V	V_{DDI} = 3.0 V	1.0	3.0	6.0		
			V_{DDI} = 5.0 V	1.5	3.7	8.5		
Output Current 2 (MD, MDB)	I_{OH2}	$V_{OH2} = V_{DDE} - 0.7$ V	V_{DDE} = 3.0 V	–11.0	–6.0	–2.0		
	I_{OL2}	V_{OL2} = 0.7 V	V_{DDE} = 3.0 V	2.0	5.5	11.0		
Output Current 3 (SEG0 to SEG95) (COM1 to COM32)	I_{OH3}	$V_{OH3} = V_{DD6} - 0.2$ V (V_{DD6} level)		—	—	–4	µA	
	I_{OHM3}	$V_{OHM3} = V_{DD5} + 0.2$ V (V_{DD5} level)		4	—	—		
	I_{OHM3S}	$V_{OHM3S} = V_{DD5} - 0.2$ V (V_{DD5} level)		—	—	–4		
	I_{OMH3}	$V_{OMH3} = V_{DD4} + 0.2$ V (V_{DD4} level)		4	—	—		
	I_{OMH3S}	$V_{OMH3S} = V_{DD4} - 0.2$ V (V_{DD4} level)		—	—	–4		
	I_{OML3}	$V_{OML3} = V_{DD2} + 0.2$ V (V_{DD2} level)		4	—	—		
	I_{OML3S}	$V_{OML3S} = V_{DD2} - 0.2$ V (V_{DD2} level)		—	—	–4		
	I_{OLM3}	$V_{OLM3} = V_{DD1} + 0.2$ V (V_{DD1} level)		4	—	—		
	I_{OLM3S}	$V_{OLM3S} = V_{DD1} - 0.2$ V (V_{DD1} level)		—	—	–4		
	I_{OL3}	$V_{OL3} = V_{SS} + 0.2$ V (V_{SS} level)		4	—	—		
Output Current 4 (OSC1)	I_{OH4R}	$V_{OH4R} = V_{DDE} - 0.5$ V (RC oscillation)	V_{DDE} = 3.0 V	–2.50	–1.30	–0.25	mA	
	I_{OL4R}	V_{OL4R} = 0.5 V (RC oscillation)	V_{DDE} = 3.0 V	0.25	1.50	2.50		
	I_{OH4C}	$V_{OH4C} = V_{DDE} - 0.5$ V (ceramic oscillation)	V_{DDE} = 3.0 V	–300	–120	–60	µA	
	I_{OL4C}	V_{OL4C} = 0.5 V (ceramic oscillation)	V_{DDE} = 3.0 V	60	120	300		
Output Leakage Current (P2.0 to P2.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	I_{OOH}	$V_{OH} = V_{DDI}$		—	—	0.3	µA	
	I_{OOL}	$V_{OL} = V_{SS}$		–0.3	—	—		

DC Characteristics (5)

(V_{DD} = 6.0 V, V_{DDI} = V_{DDE} = 3.0 V, V_{DD1} = 1.0 V, V_{DD2} = 2.0 V, V_{DD3} = 3.0 V, V_{DD4} = 4.0 V, V_{DD5} = 5.0 V, V_{DD6} = 6.0 V, Ta = –20 to +70°C unless otherwise specified)

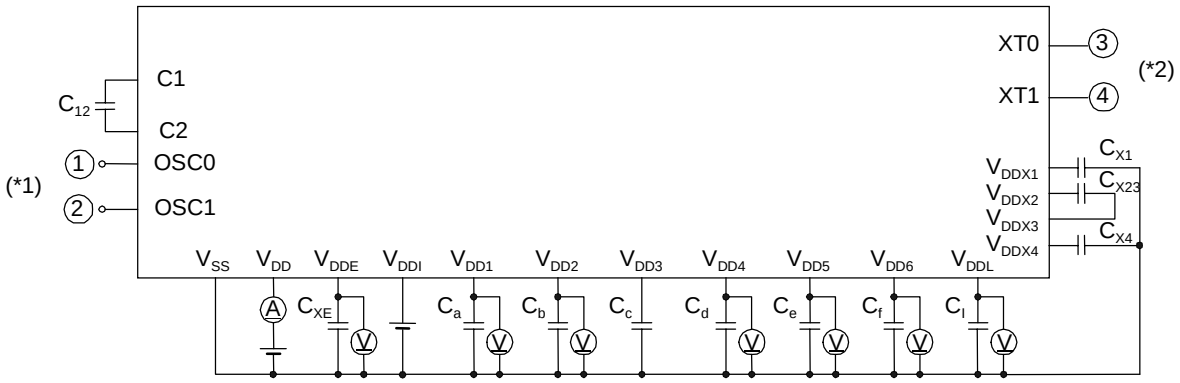
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	I_{IH1}	V_{IH1} = V_{DDI} (when pulled down)	V_{DDI} = 3.0 V	10	20	40	μA	3
			V_{DDI} = 5.0 V	20	60	120		
	I_{IL1}	V_{IL1} = V_{SS} (when pulled up)	V_{DDI} = 3.0 V	–40	–20	–10		
			V_{DDI} = 5.0 V	–120	–60	–20		
	I_{IH1Z}	V_{IH1} = V_{DDI} (in a high impedance state)		0	—	1.0		
	I_{IL1Z}	V_{IL1} = V_{SS} (in a high impedance state)		–1.0	—	0		
Input Current 2 (OSC0)	I_{IL2}	V_{IL2} = V_{SS} (when pulled up)	V_{DDE} = 3.0 V	–350	–170	–30		
	I_{IH2R}	V_{IH2R} = V_{DDE} (RC oscillation)		0	—	1.0		
	I_{IL2R}	V_{IL2R} = V_{SS} (RC oscillation)		–1.0	—	0		
	I_{IH2C}	V_{IH2R} = V_{DDE} (ceramic oscillation)		0.1	0.5	1.0		
	I_{IL2C}	V_{IL2R} = V_{SS} (ceramic oscillation)		–1.0	–0.5	–0.1		
Input Current 3 (RESET)	I_{IH3}	V_{IH3} = V_{DD}	V_{DD} = 6.0 V	40	60	150		
	I_{IL3}	V_{IL3} = V_{SS}		–1.0	—	0		
Input Current 4 (TST1, TST2)	I_{IH4}	V_{IH4} = V_{DD}	V_{DD} = 6.0 V	4.0	12.0	16.0	mA	
	I_{IL4}	V_{IL4} = V_{SS}		–1.0	—	0	μA	

DC Characteristics (6)

(V_{DD} = 6.0 V, V_{DDI} = V_{DDE} = 3.0 V, V_{DD1} = 1.0 V, V_{DD2} = 2.0 V, V_{DD3} = 3.0 V, V_{DD4} = 4.0 V, V_{DD5} = 5.0 V, V_{DD6} = 6.0 V, Ta = –20 to +70°C unless otherwise specified)

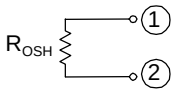
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	V_{IH1}	V_{DDI} = 3.0 V	2.3	—	3.0	V	4
		V_{DDI} = 5.0 V	3.8	—	5.0		
	V_{IL1}	V_{DDI} = 3.0 V	0	—	0.7		
		V_{DDI} = 5.0 V	0	—	1.2		
Input Voltage 2 (OSC0)	V_{IH2}	V_{DDE} = 3.0 V	2.4	—	3.0		
	V_{IL2}		0	—	0.6		
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	V_{DD} = 6.0 V	4.8	—	6.0		
	V_{IL3}		0	—	1.2		
Hysteresis Width 1 (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	ΔV_{T1}	V_{DDI} = 3.0 V	0.2	0.5	1.0		
		V_{DDI} = 5.0 V	0.25	1.00	1.50		
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV_{T2}	V_{DD} = 5.0 V	0.25	1.00	1.50		
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P8.0 to P8.3) ⋮ (PC.0 to PC.3) (PE.0 to PE.3)	C_{IN}	—	—	—	5	pF	—

Measuring circuit 1

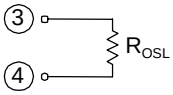


C_{X1}, C_{X23}, C_{X4}, C_{XE}	: 1.0 µF
C_a, C_b, C_c, C_d, C_e, C_f, C_{12}	: 1.0 µF
C_I	: 0.1 µF
C_G	: 15 pF
C_{L0}	: 30 pF
C_{L1}	: 30 pF
Ceramic resonator	: CSA2.00MG (2 MHz)
	: CSB1000J (1 MHz)
	(Murata MFG-.make)

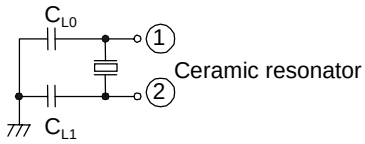
*1 RC Oscillator



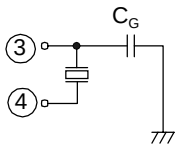
*2 RC Oscillator



Ceramic Oscillator

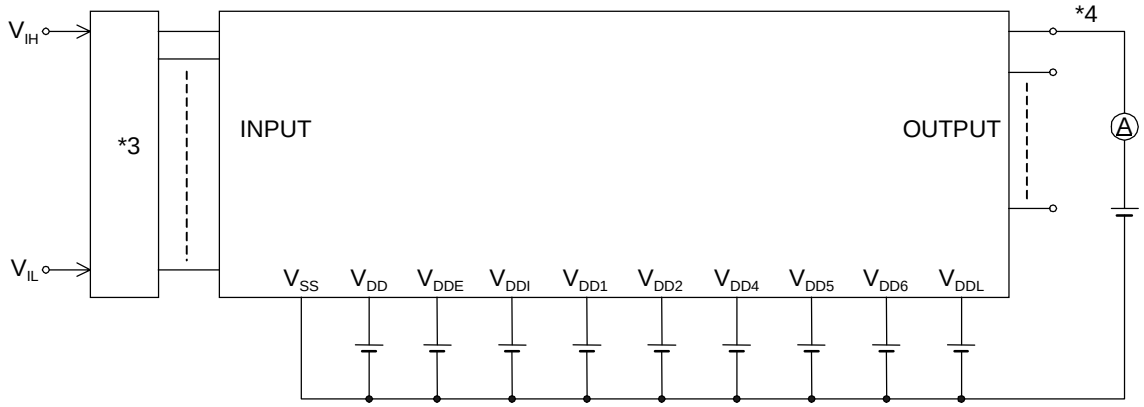


Crystal Oscillator



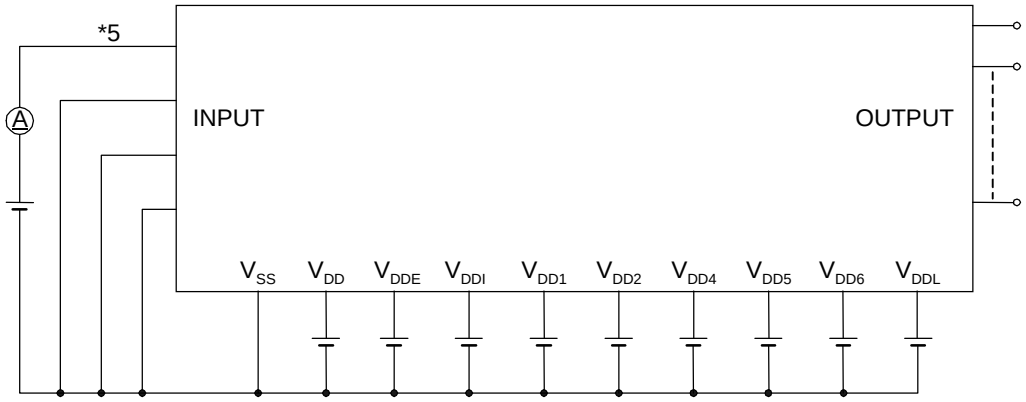
32.768 kHz
crystal

Measuring circuit 2

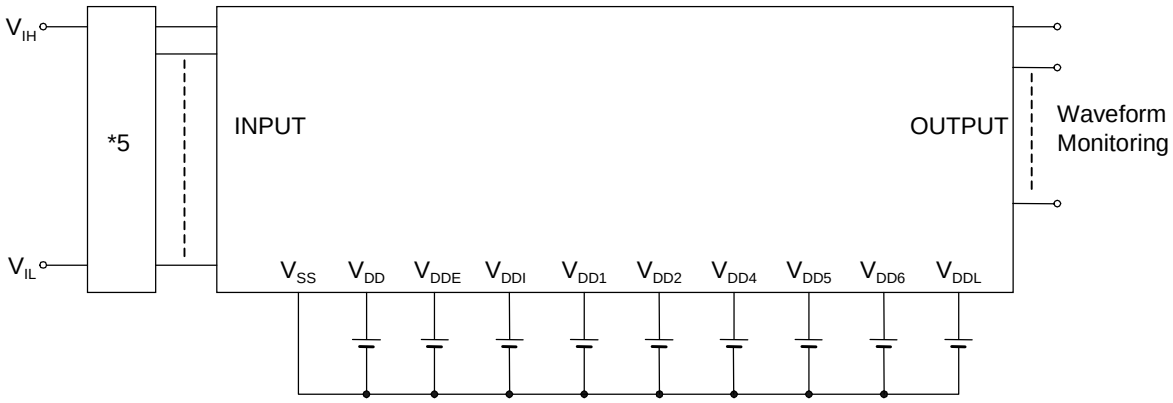


*3 Input logic circuit to determine the specified measuring conditions.
*4 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*5 Measured at the specified input pins.

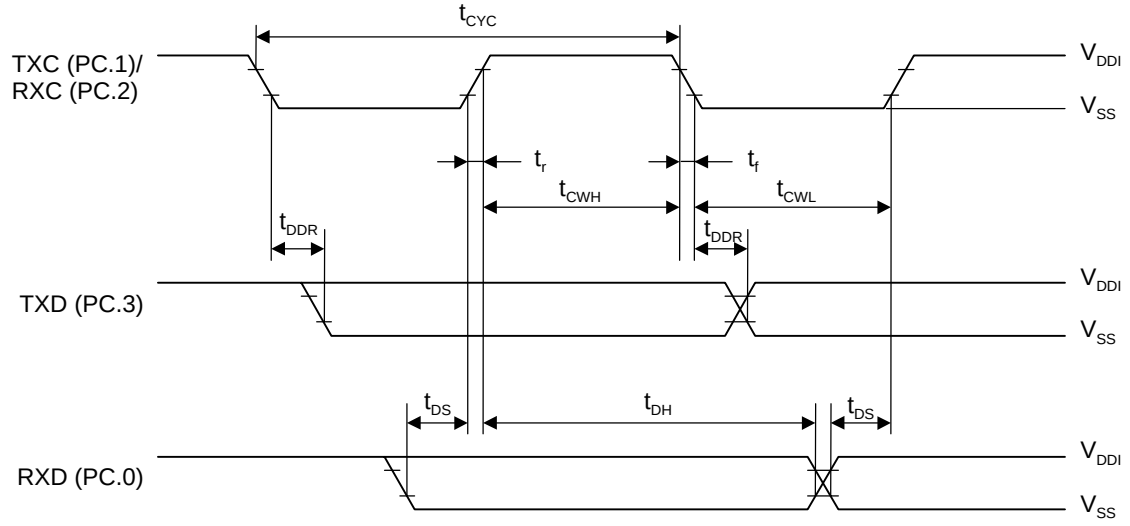
AC Characteristics (Serial Interface, Serial Port)

(1) Synchronous Communication

(V_{DD} = 3.5 to 7.2 V,V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	
TXC/RXC Output Cycle Time	$t_{CYC1\ (O)}$	CPU operating at 32.768 kHz	—	30.5	—	
	$t_{CYC2\ (O)}$	CPU operating at 2 MHz	—	0.5	—	
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	
RXD Input Setup Time	t_{DS}	—	0.5	—	—	
RXD Input Hold Time	t_{DH}	—	0.8	—	—	

Synchronous communication timing
("H" level = 4.0 V, "L" level = 1.0 V)

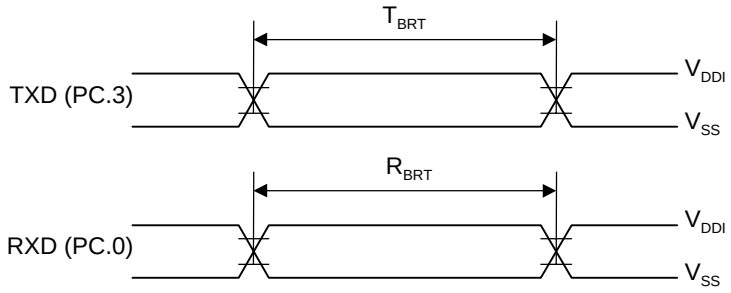


(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	

f_{BRT}: Baud rates (1200, 2400, 4800, 9600 bps)

UART communication timing
("H" level = 4.0 V, "L" level = 1.0 V)

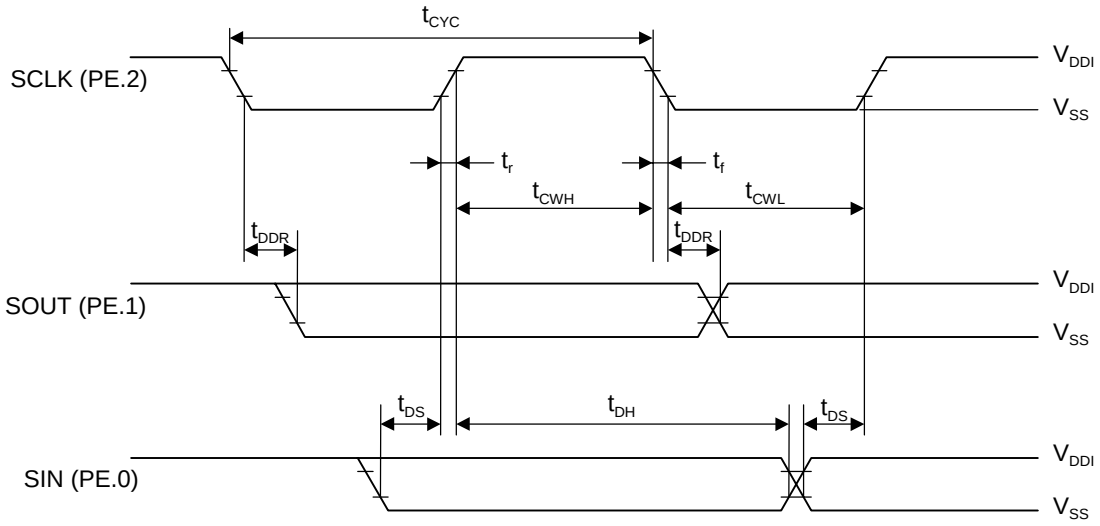


AC Characteristics (Serial Interface, Shift Register)

(V_{DD} = 3.5 to 7.2 V, V_{DDI} = 5.0 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t_f	—	—	—	1.0	µs
SCLK Input Rise Time	t_r	—	—	—	1.0	
SCLK Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	
SCLK Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	
SCLK Input Cycle Time	t_{CYC}	V_{DDI} = V_{DDE} to 5.5 V	1.8	—	—	
SCLK Output Cycle Time	$t_{CYC1(O)}$	CPU operating at 32.768 kHz	—	30.5	—	
	$t_{CYC2(O)}$	CPU operating at 2 MHz	—	0.5	—	
SOUT Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	
SIN Input Setup Time	t_{DS}	—	0.5	—	—	
SIN Input Hold Time	t_{DH}	—	0.8	—	—	

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



AC Characteristics (External Memory Interface)

(V_{DD} = 3.5 to 7.2 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) For Reading from External Memory

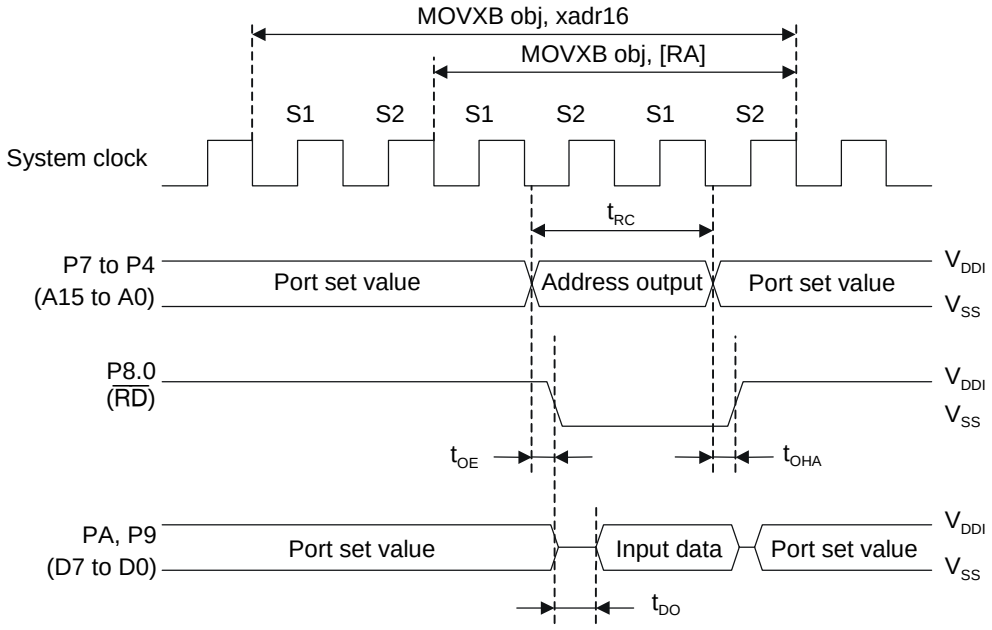
(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61.0	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	5.0	
Output Enable Time	t_{OHA}	—	—	—	5.0	
External Memory Output Delay Time	t_{DO}	—	—	—	5.0	

(b) When the CPU operates at 2 MHz (V_{DD} = 3.5 to 7.2 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1.0	—	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	100	ns
Output Enable Time	t_{OHA}	—	—	—	100	
External Memory Output Delay Time	t_{DO}	—	—	—	150	

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



(2) For Writing to External Memory

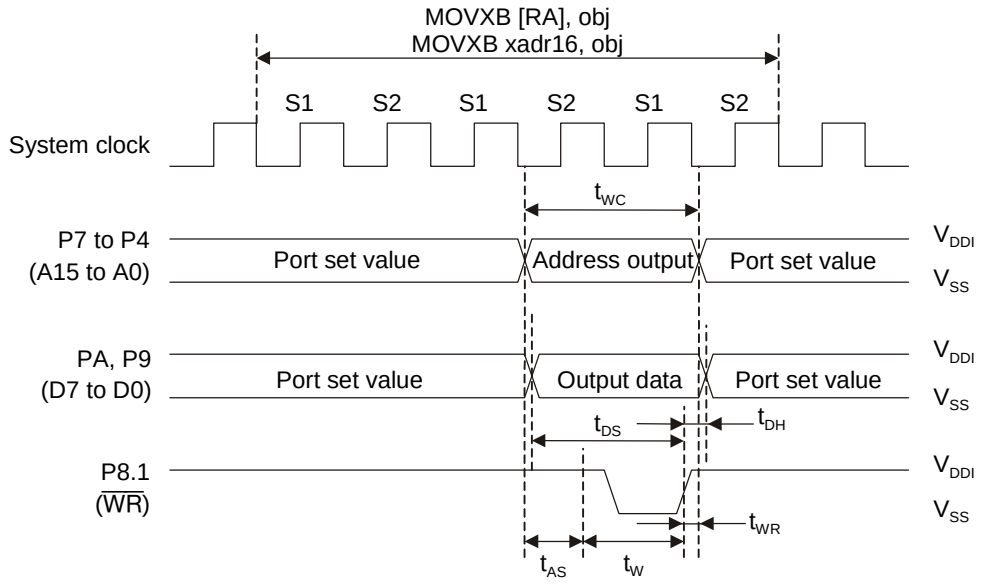
(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61.0	—	µs
Address Setup Time	t_{AS}	—	—	30.5	—	
Write Time	t_{W}	—	—	15.3	—	
Write Recovery Time	t_{WR}	—	—	15.3	—	
Data Setup Time	t_{DS}	—	—	45.8	—	
Data Hold Time	t_{DH}	—	—	15.3	—	

(b) When the CPU operates at 2 MHz (V_{DD} = 3.5 to 7.2 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1.0	—	—	µs
Address Setup Time	t_{AS}	—	0.4	—	—	
Write Time	t_{W}	—	0.2	—	—	
Write Recovery Time	t_{WR}	—	0.2	—	—	
Data Setup Time	t_{DS}	—	0.7	—	—	
Data Hold Time	t_{DH}	—	0.2	—	—	

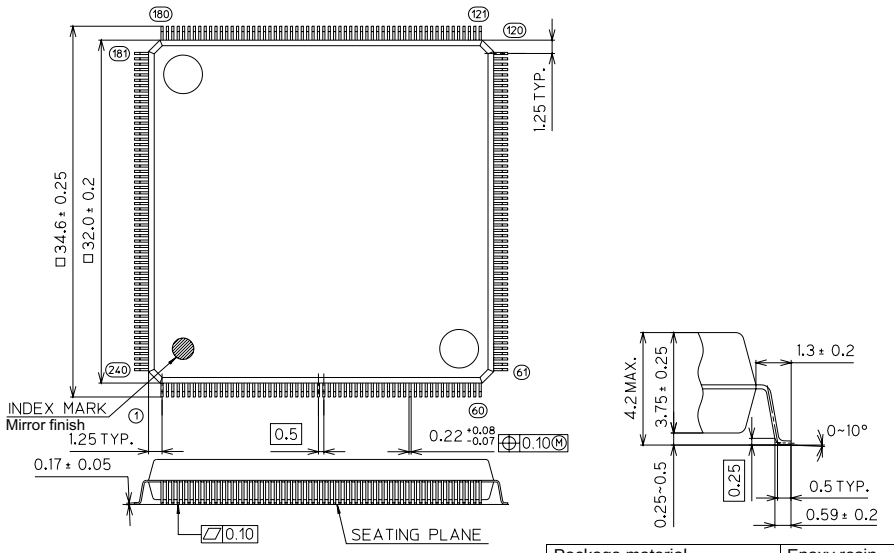
AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



PACKAGE DIMENSIONS

(Unit: mm)

QFP240-P-3232-0.50-BK4



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	7.82 TYP.
Rev. No./Last Revised	2/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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