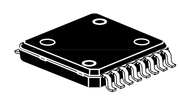
MHVIC2114R2

The Wideband IC Line
RF LDMOS Wideband Integrated Power Amplifier

**2100 MHz, 27 V, 23 dBm
SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIER**



**CASE 978-03
PFP-16**

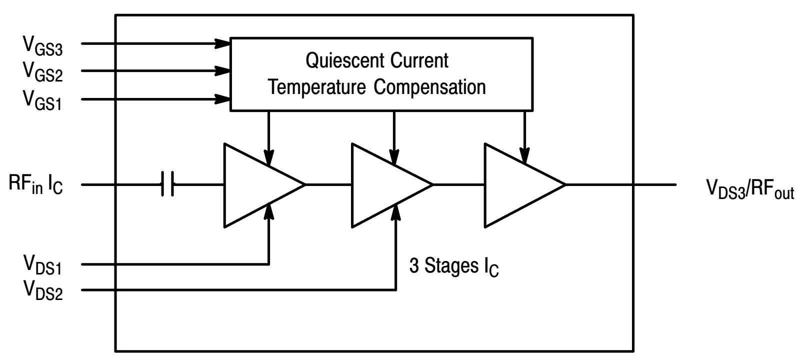
The MHVIC2114R2 wideband integrated circuit is designed for base station applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On-Chip matching design makes it usable from 1600 to 2600 MHz. The linearity performances cover all modulation formats for cellular applications: CDMA and W-CDMA. The device is in a PFP-16 flat pack package that provides excellent thermal performance through a solderable backside contact.

Final Application

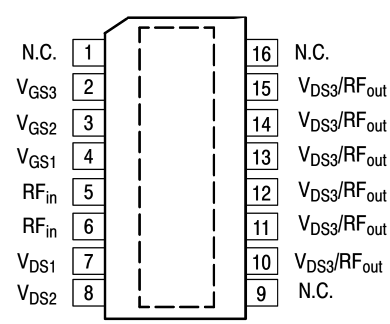
- Typical Two-Tone Performance: V_{DD} = 27 Volts, I_{DQ1} = 95 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, P_{out} = 15 Watts PEP, Full Frequency Band
  Power Gain — 32 dB
  IMD — -30 dBc

Driver Application

- Typical Single-Channel W-CDMA Performance: V_{DD} = 27 Volts, I_{DQ1} = 96 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, P_{out} = 23 dBm, 2110-2170 MHz, 3GPP Test Model 1, Measured in a 3.84 MHz BW @ 5 MHz Offset, 64 DTCH, Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 32 dB
  ACPR — -58 dBc
- P1dB = 14 Watts, Gain Flatness = 0.2 dB from 2110 to 2170 MHz
- Capable of Handling 3:1 VSWR, @ 27 Vdc, 2140 MHz, 15 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Temperature Compensation with Enable/Disable Function
- Integrated ESD Protection
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.



PIN CONNECTIONS



(Top View)

NOTE: Exposed backside flag is source terminal for transistors.

MOTOROLA intelligence everywhere™ digital dna™

**For More Information On This Product,
Go to: www.freescale.com**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Input Power	P_{in}	5	dBm

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Driver Application (P_{out} = +0.2 W CW)	Stage 1, 27 Vdc, I_{DQ1} = 96 mA		11.5	
	Stage 2, 27 Vdc, I_{DQ2} = 204 mA		7.52	
	Stage 3, 27 Vdc, I_{DQ3} = 111 mA		5.52	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

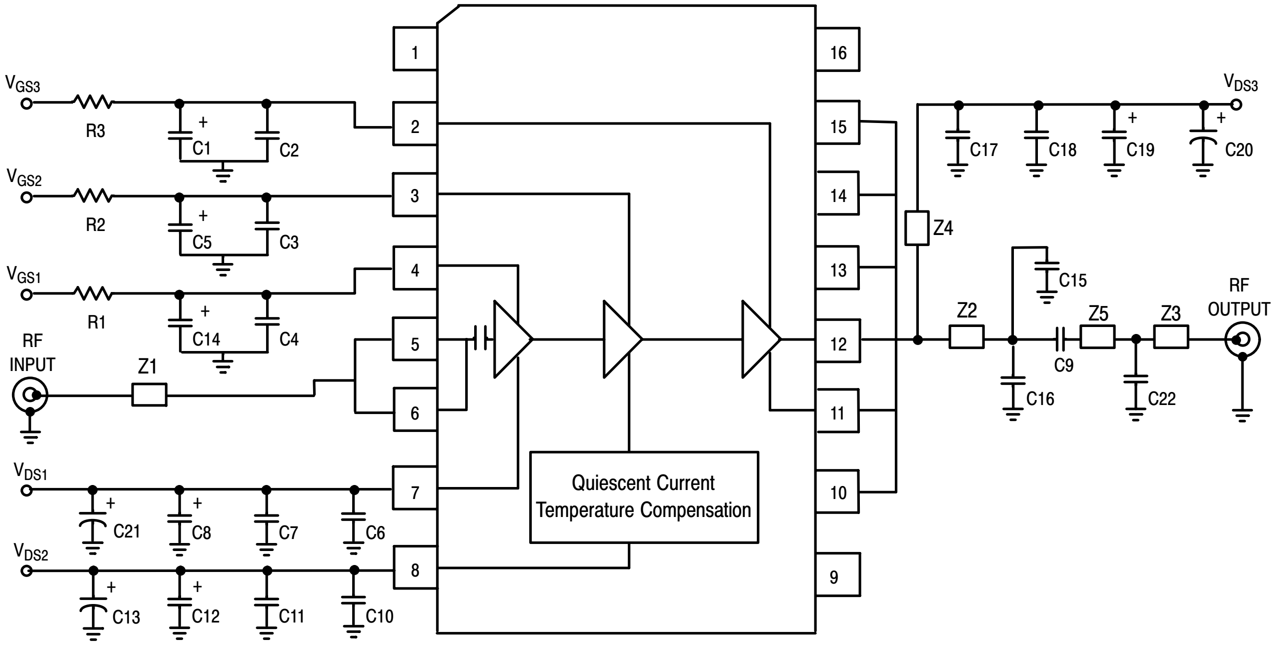
Test Methodology	Rating
Per JESD 22-A113	3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

W-CDMA CHARACTERISTICS (In Motorola Test Fixture, 50 ohm system) V_{DD} = 27 Vdc, I_{DQ1} = 96 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, P_{out} = 23 dBm, 2110-2170 MHz, Single-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carrier. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	29	32	36	dB
Gain Flatness	G_F	—	0.3	0.5	dB
Input Return Loss	IRL	—	-13	-10	dB
Adjacent Channel Power Ratio	ACPR	—	-60	-57	dBc
Group Delay	Delay	—	1.7	—	ns
Phase Linearity	—	—	0.2	—	°

(1) Refer to AN1955/D, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.motorola.com/semiconductors/rf. Select Documentation/Application Notes - AN1955.



Z1	0.323″ x .055″ 50 Ω Microstrip
Z2	0.196″ x .176″ Microstrip
Z3	0.286″ x .055″ Microstrip
Z4	0.150″ x .018″ Microstrip
Z5	0.363″ x .055″ Microstrip
PCB	Arlon, 0.021″, ε_r = 2.55

Figure 1. MHVIC2114R2 Test Circuit Schematic

Table 1. MHVIC2114R2 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C5, C8, C12, C14, C19	1 μF Tantalum Chip Capacitors	TAJA105K035R	Kemet
C2, C3, C4, C7, C11, C18	0.01 μF Chip Capacitors	0805C103K5RACTR	Vishay
C6, C10, C17	6.8 pF Chip Capacitors (ACCU-P)	AVX08051J6R8BBT	AVX
C9	1.5 pF Chip Capacitor (ACCU-P)	AVX08051J1R5BBT	AVX
C15, C16	2.2 pF Chip Capacitors (ACCU-P)	AVX08051J2R2BBT	AVX
C22	1.0 pF Chip Capacitor (ACCU-P)	AVX08051J1R0BBT	AVX
C13, C20, C21	330 μF Electrolytic Capacitors	MCR35V337M10X16	Multicomp
R1, R2, R3	1 kΩ Chip Resistors (0805)	P1.00KCCT-ND	Panasonic

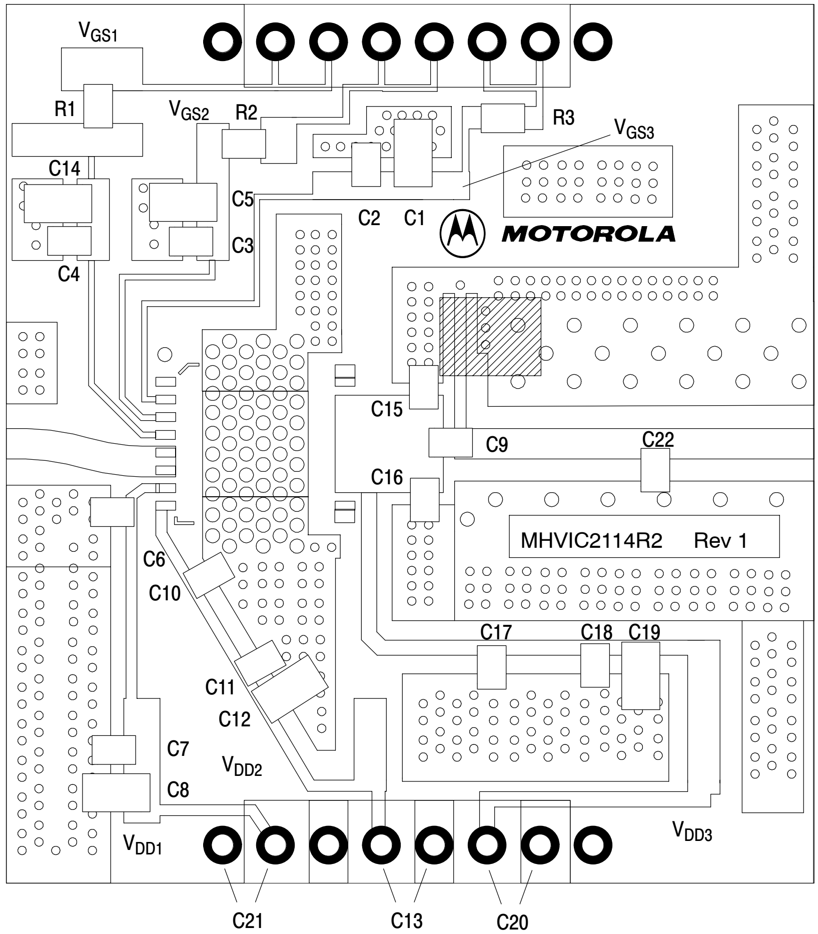


Figure 2. MHVIC2114R2 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

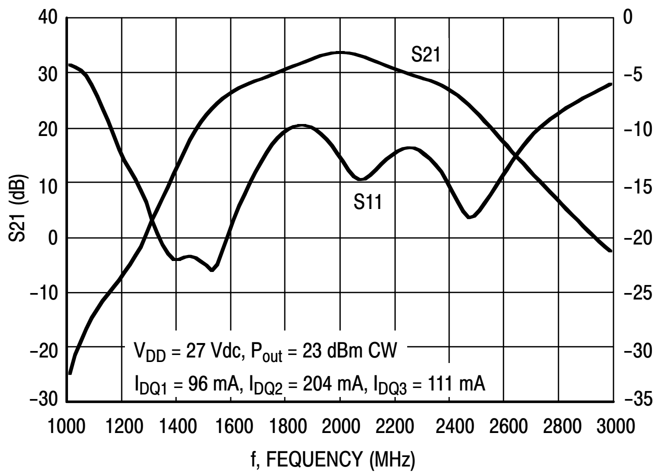


Figure 3. Broadband Frequency Response

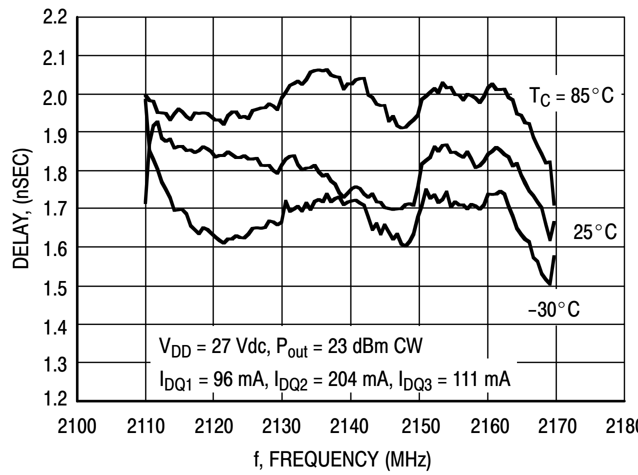


Figure 4. Delay versus Frequency

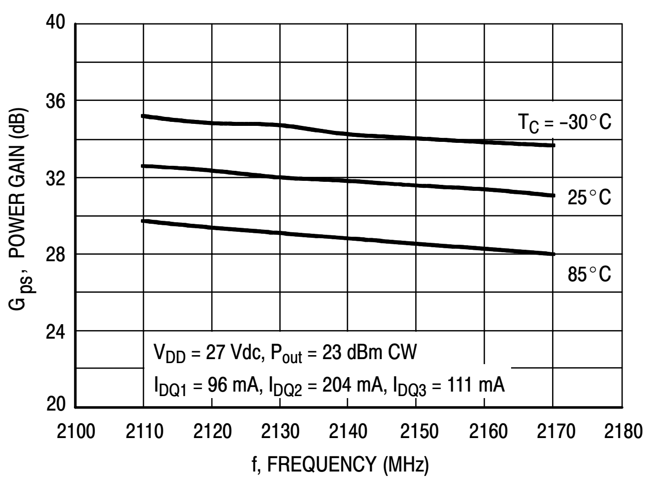


Figure 5. Power Gain versus Frequency

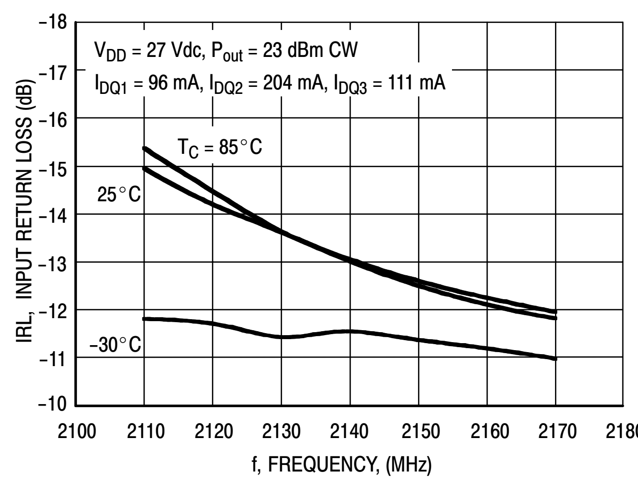


Figure 6. Input Return Loss versus Frequency

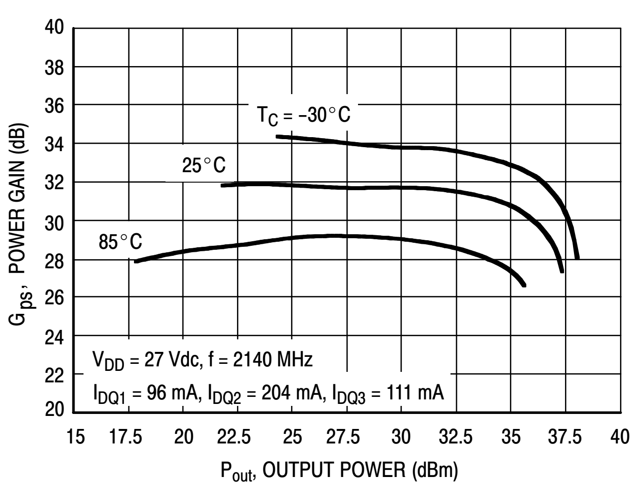


Figure 7. Power Gain versus Output Power

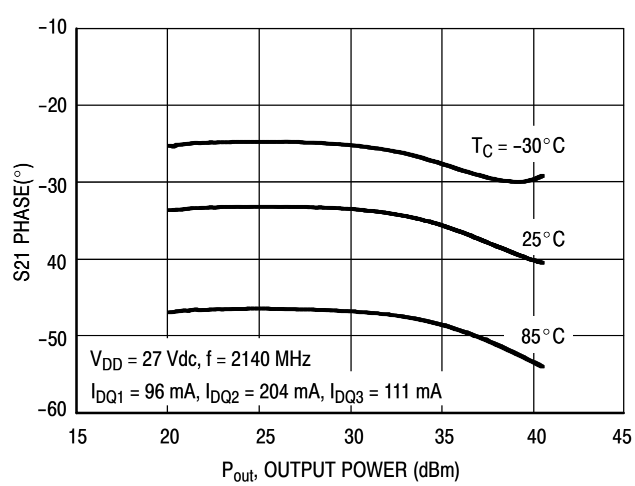


Figure 8. S21 Phase versus Output Power

TYPICAL CHARACTERISTICS

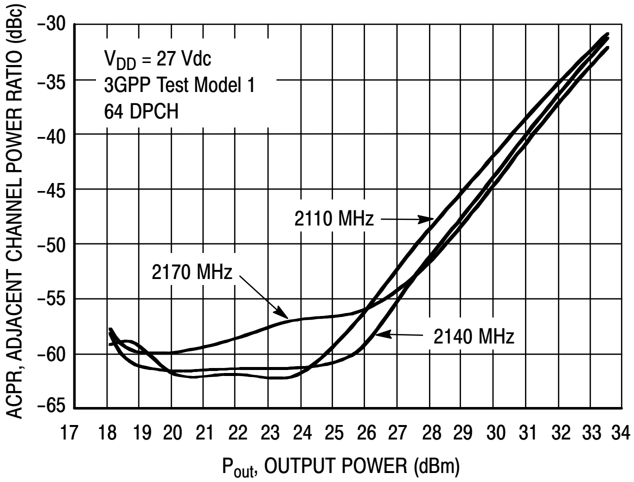


Figure 9. W-CDMA ACPR versus Output Power

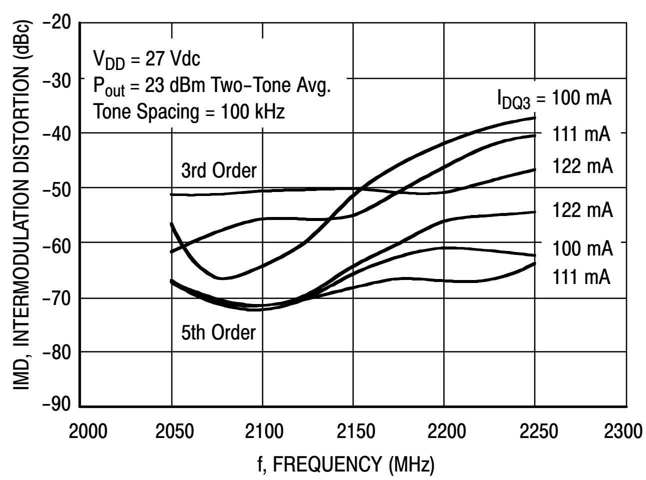


Figure 10. Two-Tone Intermodulation Distortion Products versus Frequency

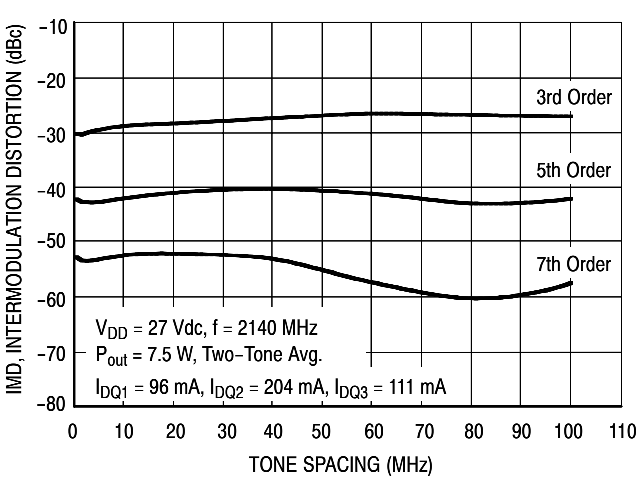


Figure 11. Two-Tone Intermodulation Distortion Products versus Tone Spacing

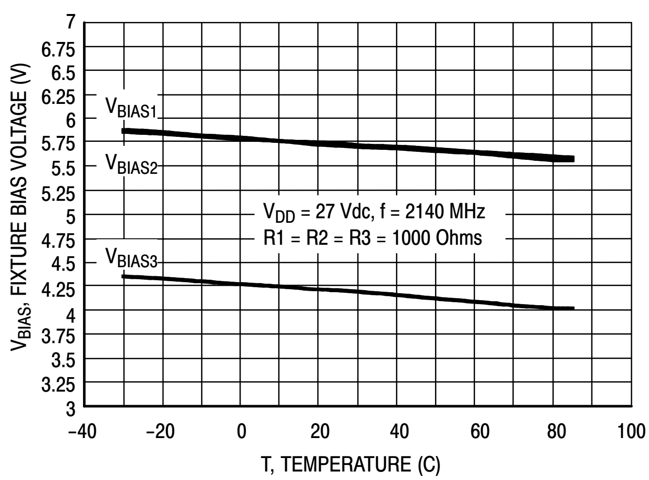


Figure 12. Fixture Bias versus Temperature

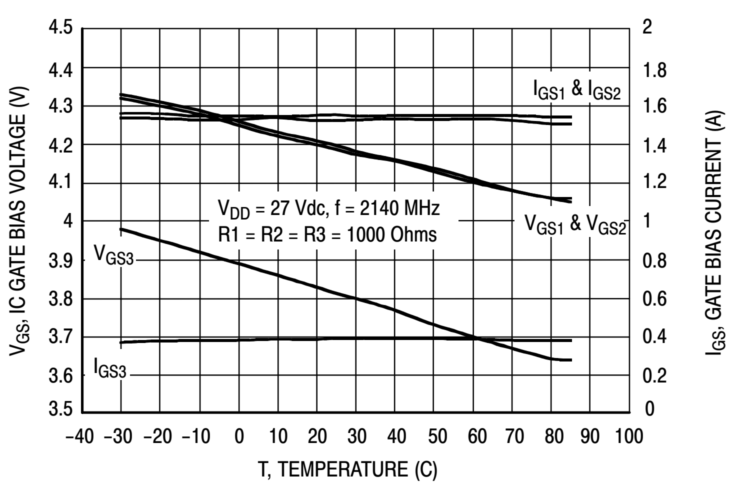
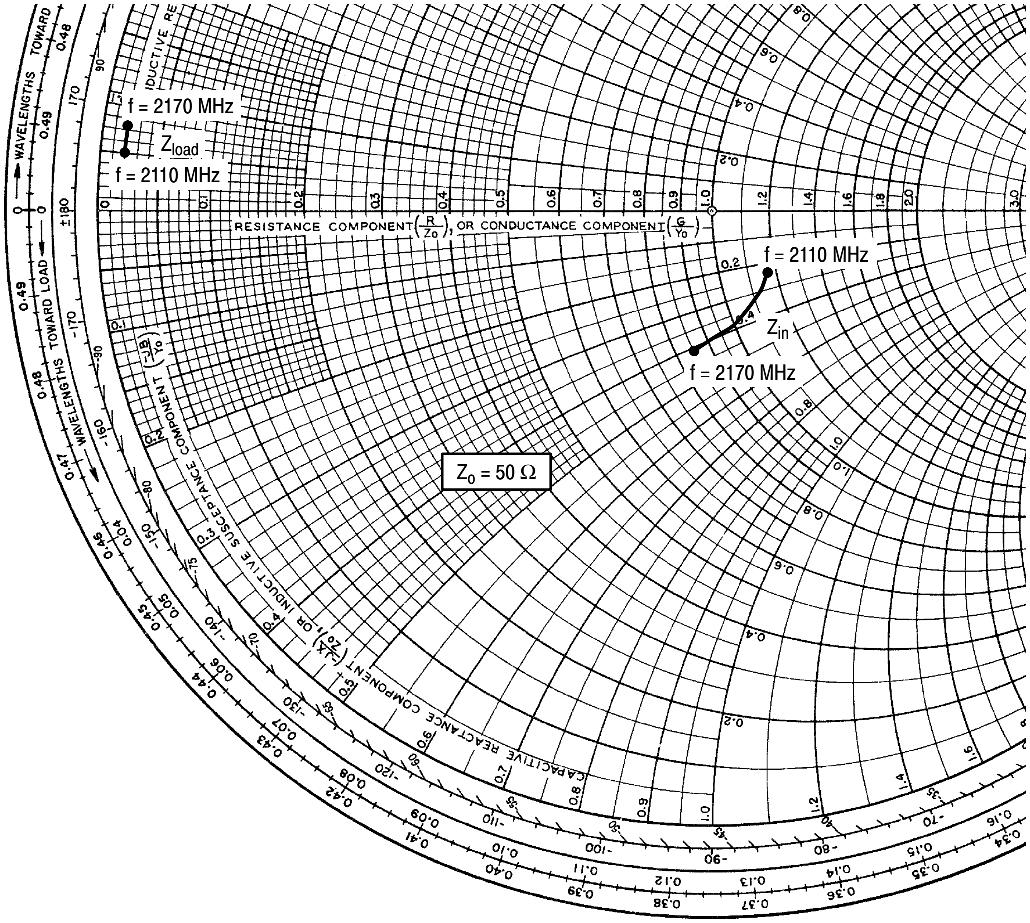


Figure 13. Gate Bias versus Temperature



V_{DD} = 27 Vdc, I_{DQ1} = 96 mA, I_{DQ2} = 204 mA, I_{DQ3} = 111 mA, P_{out} = 23 dBm

f MHz	Z_{in} Ω	Z_{load} Ω
2110	57.9 - j12.1	1.1 + j2.7
2140	50.6 - j18.9	1.1 + j3.4
2170	42.3 - j21.1	1.2 + j3.7

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

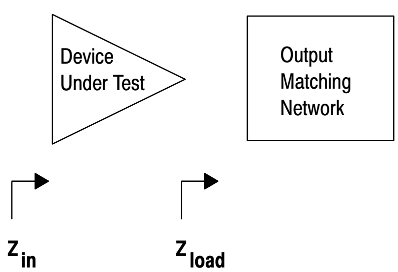
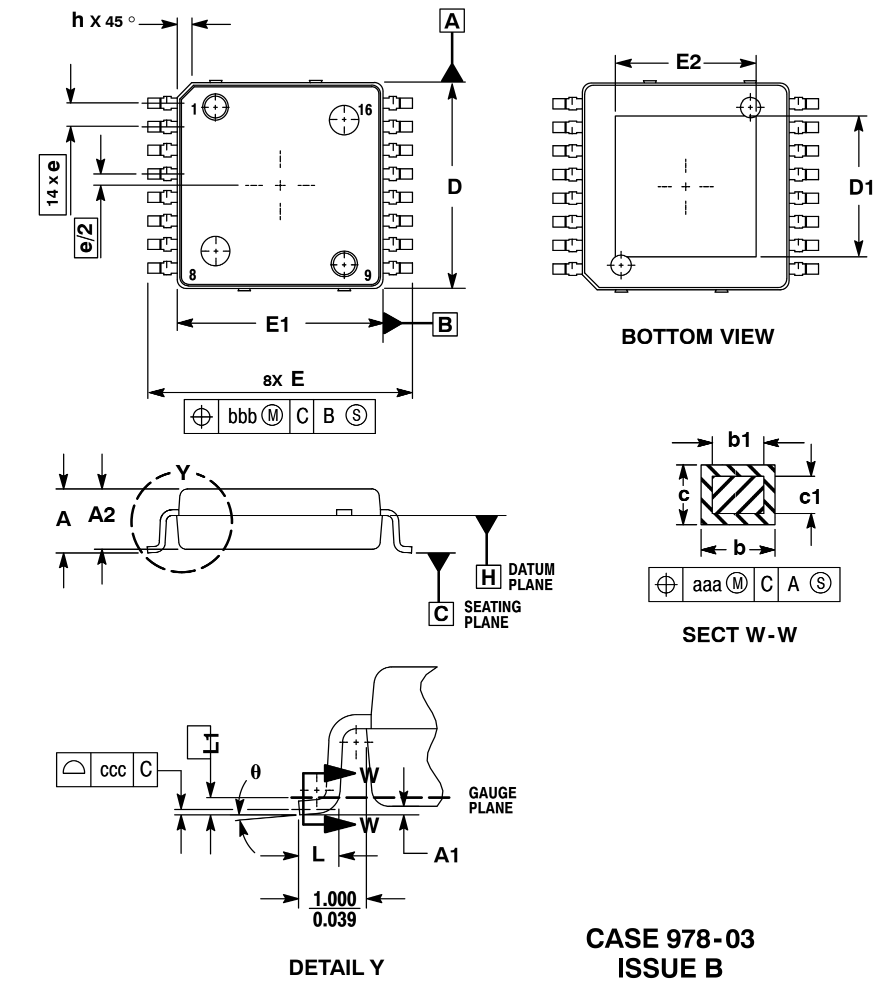


Figure 14. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978-03
ISSUE B
PFP-16

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