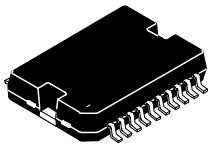
5.0 A H-Bridge

33886

H-BRIDGE



VW SUFFIX (PB-FREE)
DH SUFFIX
98ASH70702A
20-PIN HSOP

The 33886 is a monolithic H-Bridge ideal for fractional horsepower DC-motor and bi-directional thrust solenoid control. The IC incorporates internal control logic, charge pump, gate drive, and low $R_{DS(ON)}$ MOSFET output circuitry. The 33886 is able to control continuous inductive DC load currents up to 5.0 A. Output loads can be pulse width modulated (PWM-ed) at frequencies up to 10 kHz.

A Fault Status output reports undervoltage, short circuit, and overtemperature conditions. Two independent inputs control the two half-bridge totem-pole outputs. Two disable inputs force the H-Bridge outputs to tri-state (exhibit high impedance).

The 33886 is parametrically specified over a temperature range of -40°C ≤ T_A ≤ 125°C, 5.0 V ≤ V+ ≤ 28 V. The IC can also be operated up to 40 V with derating of the specifications. The IC is available in a surface mount power package with exposed pad for heatsinking.

Features

- 5.0 V to 40 V Continuous Operation
- 120 mΩ $R_{DS(ON)}$ H-Bridge MOSFETs
- TTL/CMOS Compatible Inputs
- PWM Frequencies up to 10 kHz
- Active Current Limiting via Internal Constant OFF-Time PWM (with Temperature-Dependent Threshold Reduction)
- Output Short Circuit Protection
- Undervoltage Shutdown
- Fault Status Reporting
- Pb-Free Packaging Designated by Suffix Code VW

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33886DH/R2	-40°C to 125°C	20 HSOP
MC33886VW/R2		

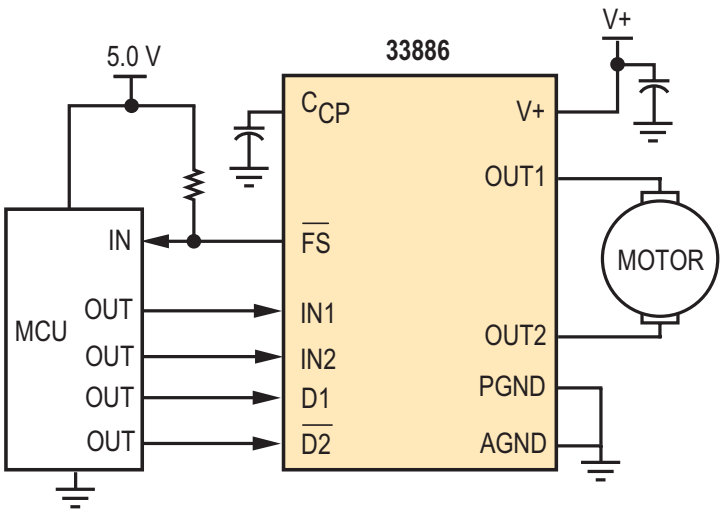


Figure 1. 33886 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

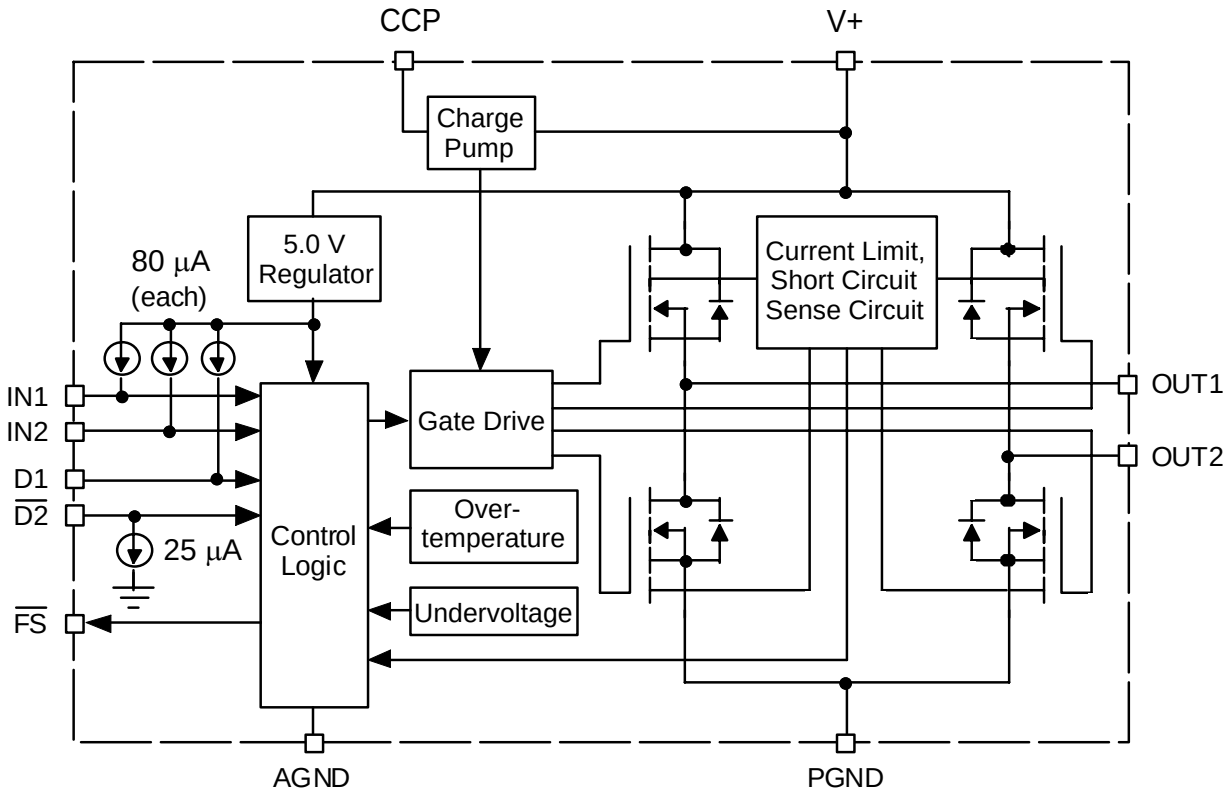


Figure 2. 33886 Simplified Internal Block Diagram

PIN CONNECTIONS

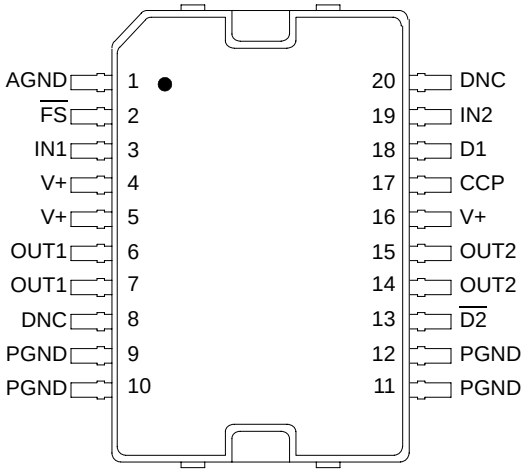


Figure 3. 33886 Pin Connections

Table 1. 33886 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 15.

Pin Number	Pin Name	Formal Name	Definition
1	AGND	Analog Ground	Low-current analog signal ground.
2	$\overline{FS}$	Fault Status for H-Bridge	Open drain active Low Fault Status output requiring a pull-up resistor to 5.0 V.
3	IN1	Logic Input Control 1	True logic input control of OUT1 (i.e., IN1 logic High = OUT1 logic High).
4, 5, 16	V+	Positive Power Supply	Positive supply connections.
6, 7	OUT1	H-Bridge Output 1	Output 1 of H-Bridge.
8, 20	DNC	Do Not Connect	Either do not connect (leave floating) or connect these pins to ground in the application. They are test mode pins used in manufacturing only.
9–12	PGND	Power Ground	Device high-current power ground.
13	$\overline{D2}$	Disable 2	Active Low input used to simultaneously tri-state disable both H-Bridge outputs. When $\overline{D2}$ is logic Low, both outputs are tri-stated.
14, 15	OUT2	H-Bridge Output 2	Output 2 of H-Bridge.
17	CCP	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump capacitor.
18	D1	Disable 1	Active High input used to simultaneously tri-state disable both H-Bridge outputs. When D1 is logic High, both outputs are tri-stated.
19	IN2	Logic Input Control 2	True logic input control of OUT2 (i.e., IN2 logic High = OUT2 logic High).

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Supply Voltage	V+	40	V
Input Voltage (1)	V_{IN}	-0.1 to 7.0	V
$\overline{FS}$ Status Output (2)	$V_{\overline{FS}}$	7.0	V
Continuous Current (3)	I_{OUT}	5.0	A
ESD Voltage for DH Package Human Body Model (4) Machine Model (5)	 V_{ESD1} V_{ESD2}	 ±2000 (6) ±200	V
ESD Voltage for VW Package Human Body Model (4) Machine Model (5)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Storage Temperature	T_{STG}	-65 to 150	°C
Ambient Operating Temperature (7)	T_A	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Peak Package Reflow Temperature During Reflow (8), (9)	T_{PPRT}	Note 8.	°C
Approximate Junction-to-Board Thermal Resistance (and Package Dissipation = 6.0 W) (10)	$R_{\theta JB}$	~5.0	°C/W

Notes

1. Exceeding the input voltage on IN1, IN2, D1, or $\overline{D2}$ may cause a malfunction or permanent damage to the device.
2. Exceeding the pull-up resistor voltage on the open drain $\overline{FS}$ pin may cause permanent damage to the device.
3. Continuous current capability so long as junction temperature is ≤ 150°C.
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
5. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
6. All pins are capable of Human Body Model ESD voltages of ±2000 V with two exceptions pertaining only to the DH suffix package: (1) $\overline{D2}$ to PGND is capable of ±1500 V and (2) OUT1 to AGND is capable of ±1000 V.
7. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heatsinking.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
10. Exposed heatsink pad plus the power and ground pins comprise the main heat conduction paths. The actual $R_{\theta JB}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (11)	V+	5.0	–	40	V
Standby Supply Current V_{EN} = 5.0 V, I_{OUT} = 0 A	$I_{Q(standby)}$	–	–	20	mA
Threshold Supply Voltage Switch-OFF Switch-ON Hysteresis	 $V+_{(thres-OFF)}$ $V+_{(thres-ON)}$ $V+_{(hys)}$	 4.15 4.5 150	 4.4 4.75 –	 4.65 5.0 –	 V V mV
CHARGE PUMP					
Charge Pump Voltage V+ = 5.0 V 8.0 V ≤ V+ ≤ 40 V	V_{CP} - V+	 3.35 –	 – –	 – 20	V
CONTROL INPUTS					
Input Voltage (IN1, IN2, D1, $\overline{D2}$) Threshold High Threshold Low Hysteresis	 V_{IH} V_{IL} V_{HYS}	 3.5 – 0.7	 – – 1.0	 – 1.4 –	V
Input Current (IN1, IN2, D1) (12) V_{IN} = 0 V	I_{IN}	-200	-80	–	µA
$\overline{D2}$ Input Current (13) $V_{\overline{D2}}$ = 5.0 V	$I_{\overline{D2}}$	–	25	100	µA

Notes

11. Specifications are characterized over the range of 5.0 V ≤ V+ ≤ 28 V. Operation >28 V will cause some parameters to exceed listed min/max values. Refer to typical operating curves to extrapolate values for operation >28 V but ≤ 40 V.
12. Inputs IN1, IN2, and D1 have independent internal pull-up current sources.
13. The $\overline{D2}$ input incorporates an active internal pull-down current sink.

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUTS (OUT1, OUT2)					
Output-ON Resistance (14)	$R_{DS(ON)}$				mΩ
5.0 V ≤ V+ ≤ 28 V, T_J = 25°C		–	120	–	
8.0 V ≤ V+ ≤ 28 V, T_J = 150°C		–	–	225	
5.0 V ≤ V+ ≤ 8.0 V, T_J = 150°C		–	–	300	
Active Current Limiting Threshold (via Internal Constant OFF-Time PWM) (15)	I_{LIM}	5.2	6.5	7.8	A
High-Side Short Circuit Detection Threshold	I_{SCH}	11	–	–	A
Low-Side Short Circuit Detection Threshold	I_{SCL}	8.0	–	–	A
Leakage Current (16)	$I_{OUT(leak)}$				μA
V_{OUT} = V+		–	100	200	
V_{OUT} = GND		–	30	60	
Output FET Body Diode Forward Voltage Drop (17)	V_F				V
I_{OUT} = 3.0 A		–	–	2.0	
Switch-OFF					°C
Thermal Shutdown	T_{LIM}	175	–	–	
Hysteresis	T_{HYS}	–	15	–	
FAULT STATUS (18)					
Fault Status Leakage Current (19)	$I_{\overline{FS}(leak)}$				μA
$V_{\overline{FS}}$ = 5.0 V		–	–	10	
Fault Status Set Voltage (20)	$V_{\overline{FS}(LOW)}$				V
$I_{\overline{FS}}$ = 300 μA		–	–	1.0	

Notes

14. Output-ON resistance as measured from output to V+ and ground.
15. Product with date codes of December 2002, week 51, will exhibit the values indicated in this table. Product with earlier date codes may exhibit a minimum of 6.0 A and a maximum of 8.5 A.
16. Outputs switched OFF with D1 or $\overline{D2}$.
17. Parameter is guaranteed by design but not production tested.
18. Fault Status output is an open drain output requiring a pull-up resistor to 5.0 V.
19. Fault Status Leakage Current is measured with Fault Status High and *not* set.
20. Fault Status Set Voltage is measured with Fault Status Low and set with $I_{\overline{FS}}$ = 300 μA.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 5.0 V ≤ V+ ≤ 28 V and -40°C ≤ T_A ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TIMING CHARACTERISTICS					
PWM Frequency (21)	f_{PWM}	–	–	10	kHz
Maximum Switching Frequency During Active Current Limiting (22)	f_{MAX}	–	–	20	kHz
Output ON Delay (23) V+ = 14 V	$t_{d(ON)}$	–	–	18	µs
Output OFF Delay (23) V+ = 14 V	$t_{d(OFF)}$	–	–	18	µs
Output Rise and Fall Time (24) V+ = 14 V, I_{OUT} = 3.0 A	t_f, t_r	2.0	5.0	8.0	µs
Output Latch-OFF Time	t_a	15	20.5	26	µs
Output Blanking Time	t_b	12	16.5	21	µs
Output FET Body Diode Reverse Recovery Time (25)	t_{rr}	100	–	–	ns
Disable Delay Time (26)	$t_{d(disable)}$	–	–	8.0	µs
Short Circuit/Overtemperature Turn-OFF Time (27)	t_{FAULT}	–	4.0	–	µs
Power-OFF Delay Time	t_{pod}	–	1.0	5.0	ms

Notes

21. The outputs can be PWM controlled from an external source. This is typically done by holding one input high while applying a PWM pulse train to the other input. The maximum PWM frequency obtainable is a compromise between switching losses and switching frequency. Refer to Typical Switching Waveforms, Figures 10 through 17, pp. 10–11.
22. The Maximum Switching Frequency during active current limiting is internally implemented. The internal control produces a constant OFF-time PWM of the output. The output load current effects the Maximum Switching Frequency.
23. Output Delay is the time duration from the midpoint of the IN1 or IN2 input signal to the 10% or 90% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning High-to-Low, the delay is from the midpoint of the input signal to the 90% point of the output response signal. If the output is transitioning Low-to-High, the delay is from the midpoint of the input signal to the 10% point of the output response signal. See Figure 4, page 8.
24. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal. See Figure 6, page 8.
25. Parameter is guaranteed by design but not production tested.
26. Disable Delay Time is the time duration from the midpoint of the D (disable) input signal to 10% of the output tri-state response. See Figure 5, page 8.
27. Increasing currents will become limited at I_{LIM}. Hard shorts will breach the I_{SCH} or I_{SCL} limit, forcing the output into an immediate tri-state latch-OFF. See Figures 8 and 9, page 9. Active current limiting will cause junction temperatures to rise. A junction temperature above 160°C will cause the active current limiting to progressively “fold-back” (or decrease) to 2.5 A typical at 175°C where thermal latch-OFF will occur. See Figure 7, page 8.

TIMING DIAGRAMS

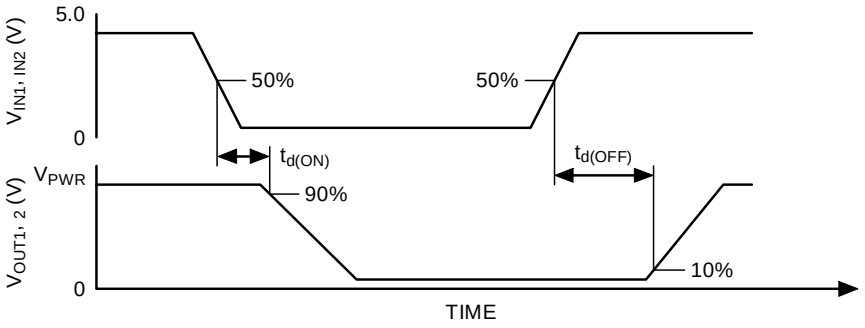


Figure 4. Output Delay Time

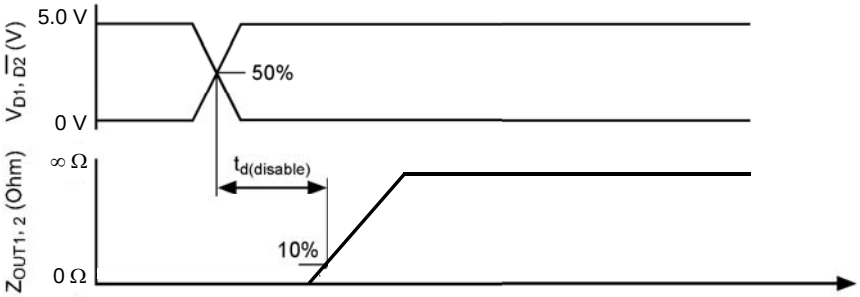


Figure 5. Disable Delay Time

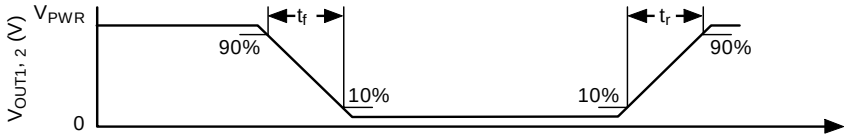


Figure 6. Output Switching Time

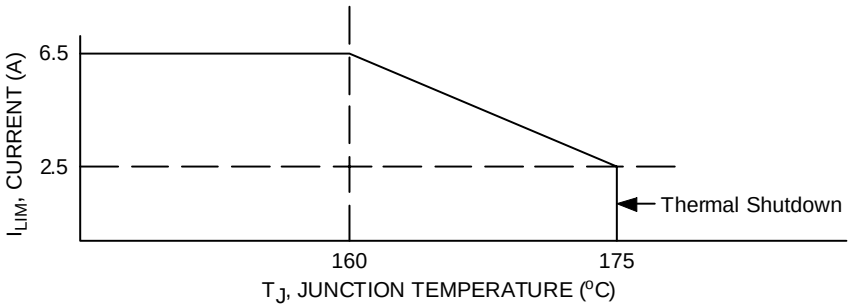


Figure 7. Active Current Limiting Versus Temperature (Typical)

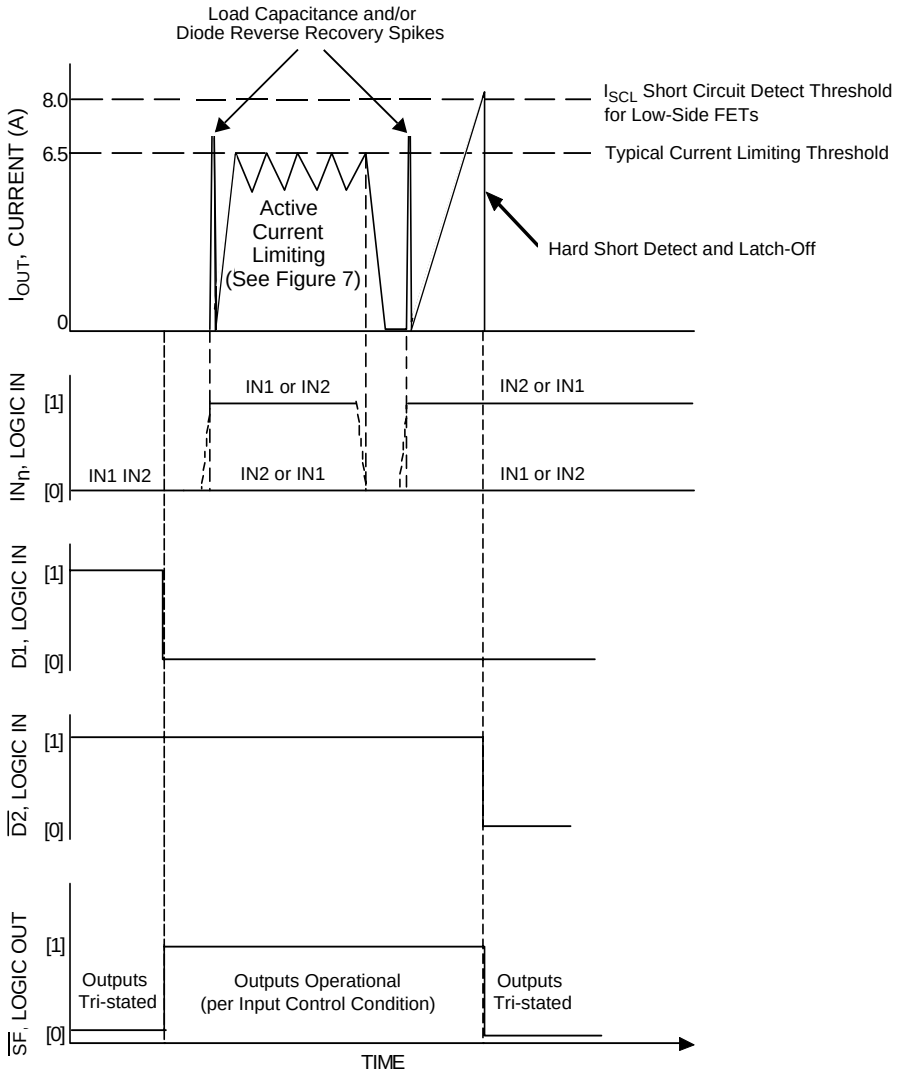


Figure 8. Active Current Limiting Versus Time

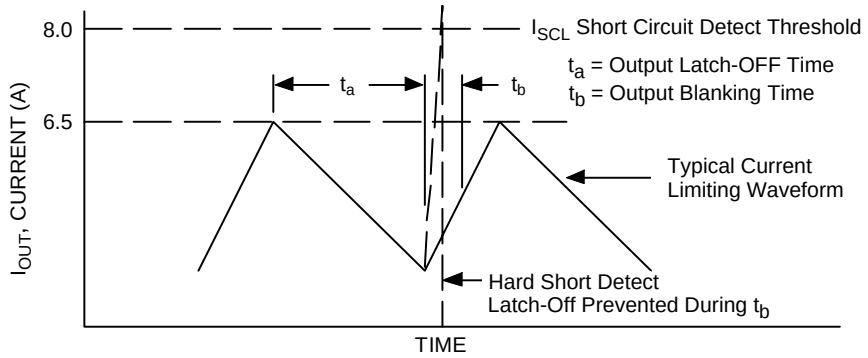


Figure 9. Active Current Limiting Detail

TYPICAL SWITCHING WAVEFORMS

Important For all plots, the following applies:

- Ch2=2.0 A per division
- L_{LOAD}=533 µH @ 1.0 kHz
- L_{LOAD}=530 µH @ 10.0 kHz
- R_{LOAD}=4.0 Ω

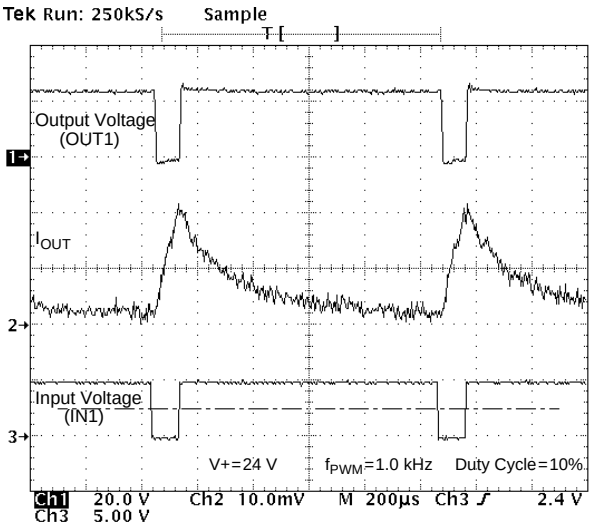


Figure 10. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 10%

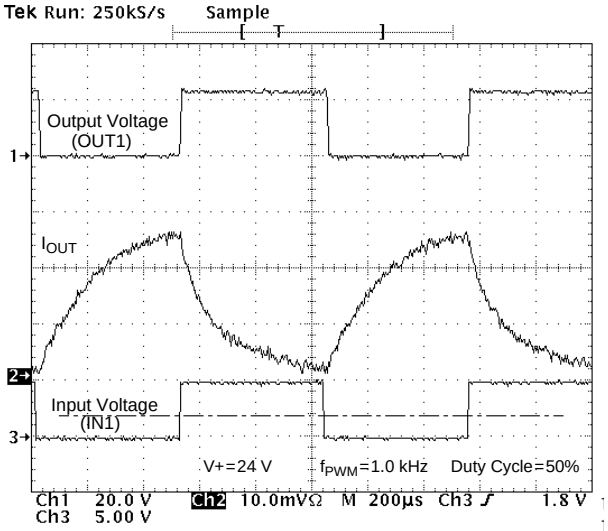


Figure 11. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 50%

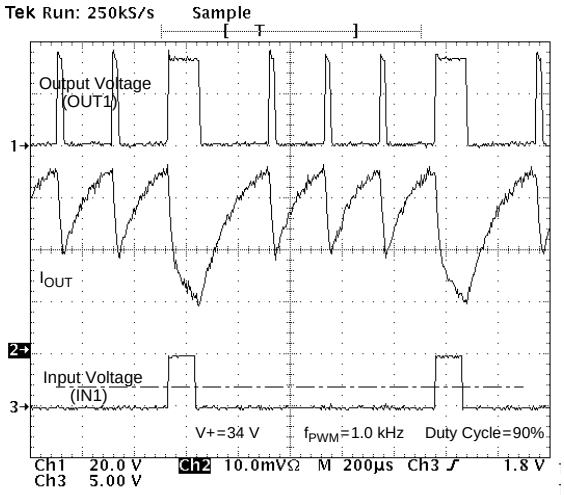


Figure 12. Output Voltage and Current vs. Input Voltage at V+ = 34 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%, Showing Device in Current Limiting Mode

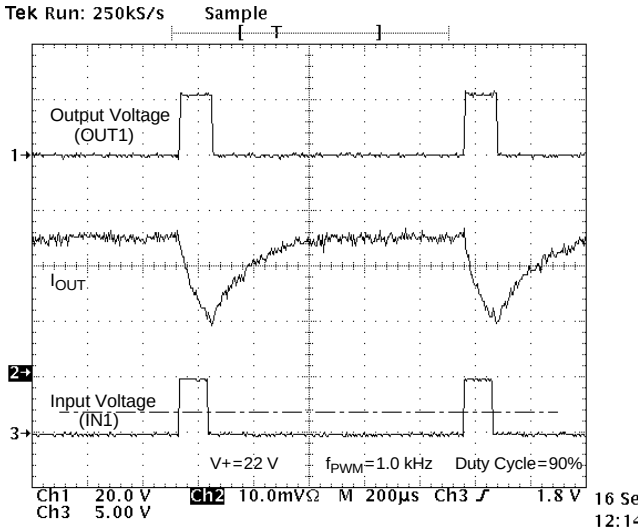


Figure 13. Output Voltage and Current vs. Input Voltage at V+ = 22 V, PMW Frequency of 1.0 kHz, and Duty Cycle of 90%

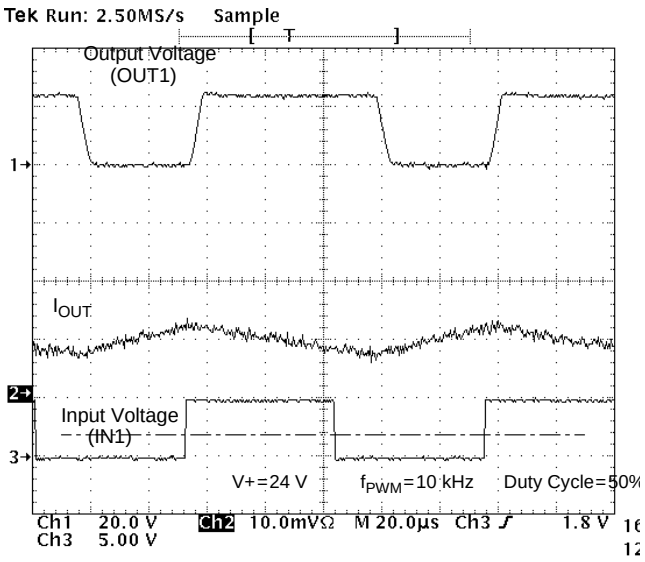


Figure 14. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 10 kHz, and Duty Cycle of 50%

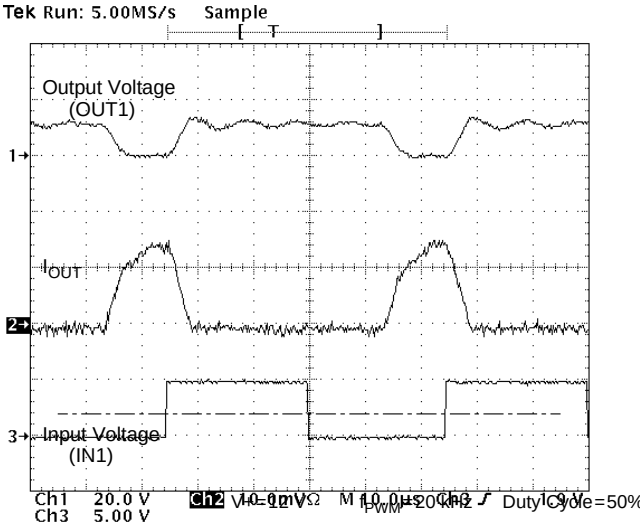


Figure 16. Output Voltage and Current vs. Input Voltage at V+ = 12 V, PMW Frequency of 20 kHz, and Duty Cycle of 50% for a Purely Resistive Load

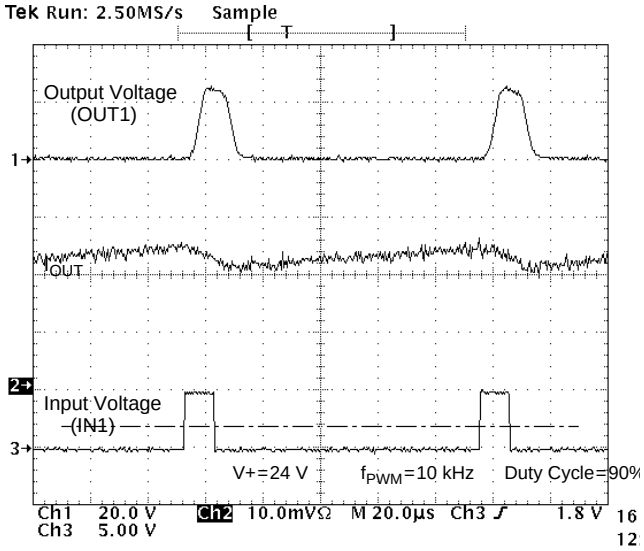


Figure 15. Output Voltage and Current vs. Input Voltage at V+ = 24 V, PMW Frequency of 10 kHz, and Duty Cycle of 90%

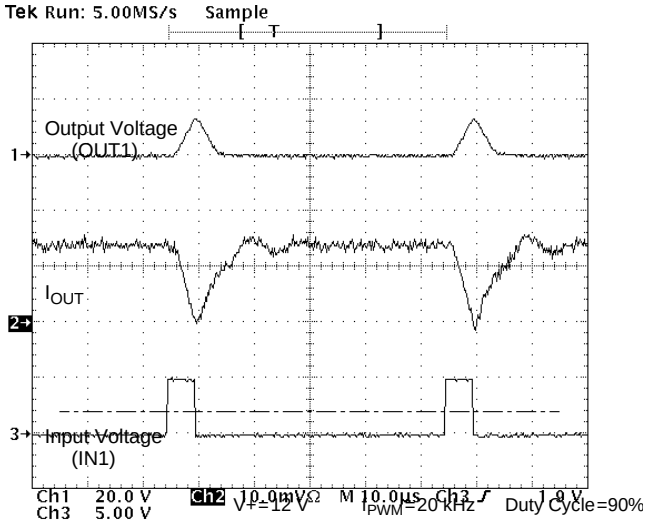


Figure 17. Output Voltage and Current vs. Input Voltage at V+ = 12 V, PMW Frequency of 20 kHz, and Duty Cycle of 90% for a Purely Resistive Load

Table 5. Truth Table

The tri-state conditions and the fault status are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = Low, H = High, X = High or Low, and Z = High impedance (all output power transistors are switched off).

Device State	Input Conditions				Fault Status Flag	Output States	
	D1	$\overline{D2}$	IN1	IN2	$\overline{FS}$	OUT1	OUT2
Forward	L	H	H	L	H	H	L
Reverse	L	H	L	H	H	L	H
Freewheeling Low	L	H	L	L	H	L	L
Freewheeling High	L	H	H	H	H	H	H
Disable 1 (D1)	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	X	L	X	X	L	Z	Z
IN1 Disconnected	L	H	Z	X	H	H	X
IN2 Disconnected	L	H	X	Z	H	X	H
D1 Disconnected	Z	X	X	X	L	Z	Z
$\overline{D2}$ Disconnected	X	Z	X	X	L	Z	Z
Undervoltage (28)	X	X	X	X	L	Z	Z
Overtemperature (29)	X	X	X	X	L	Z	Z
Short Circuit (29)	X	X	X	X	L	Z	Z

Notes

28. In the case of an undervoltage condition, the outputs tri-state and the fault status is set logic Low. Upon undervoltage recovery, fault status is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
29. When a short circuit or overtemperature condition is detected, the power outputs are tri-state latched-OFF independent of the input signals and the fault status flag is set logic Low.

ELECTRICAL PERFORMANCE CURVES

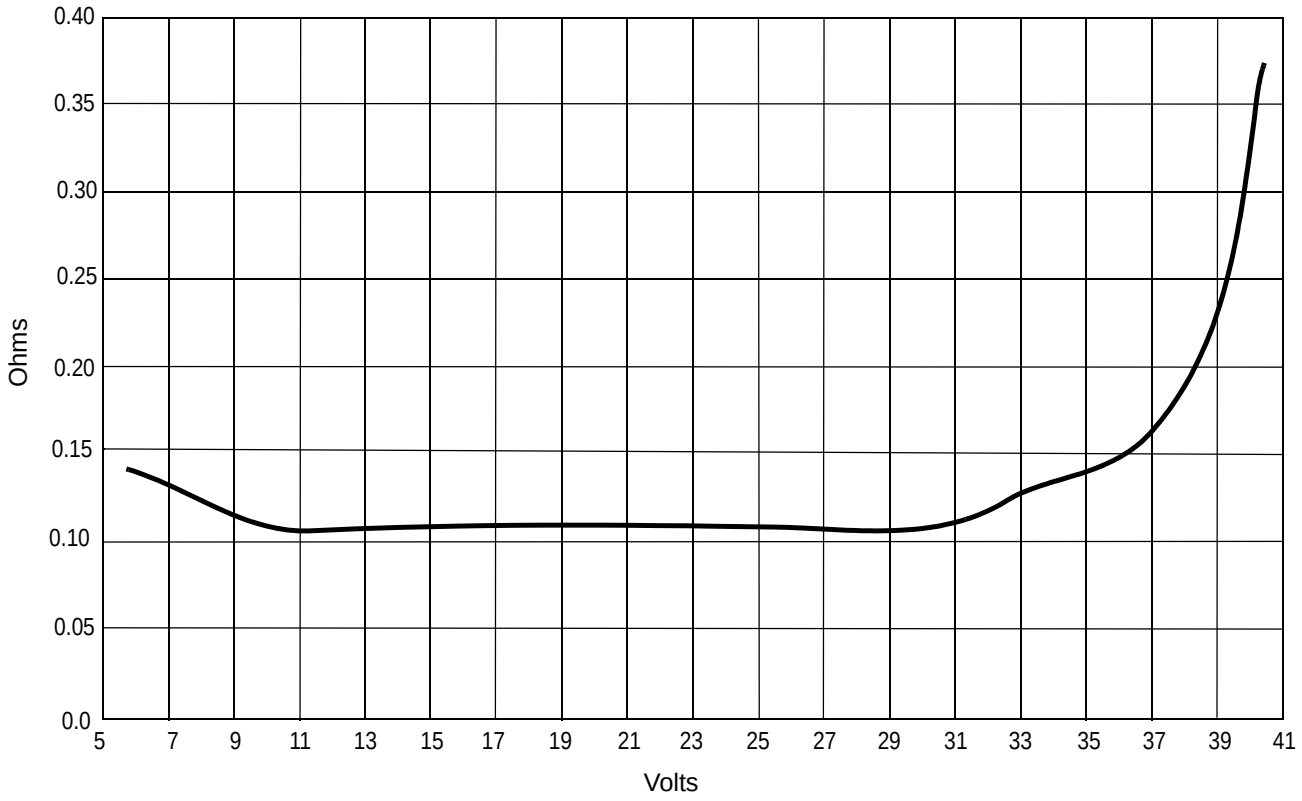


Figure 18. Typical High-Side $R_{DS(ON)}$ Versus V+

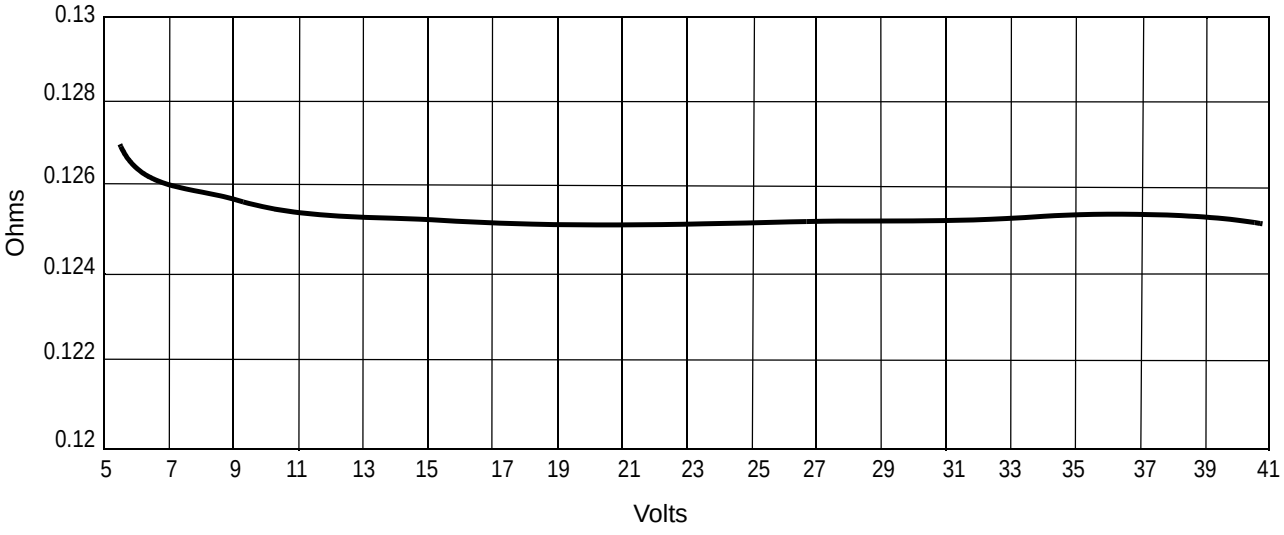


Figure 19. Typical Low-Side $R_{DS(ON)}$ Versus V+

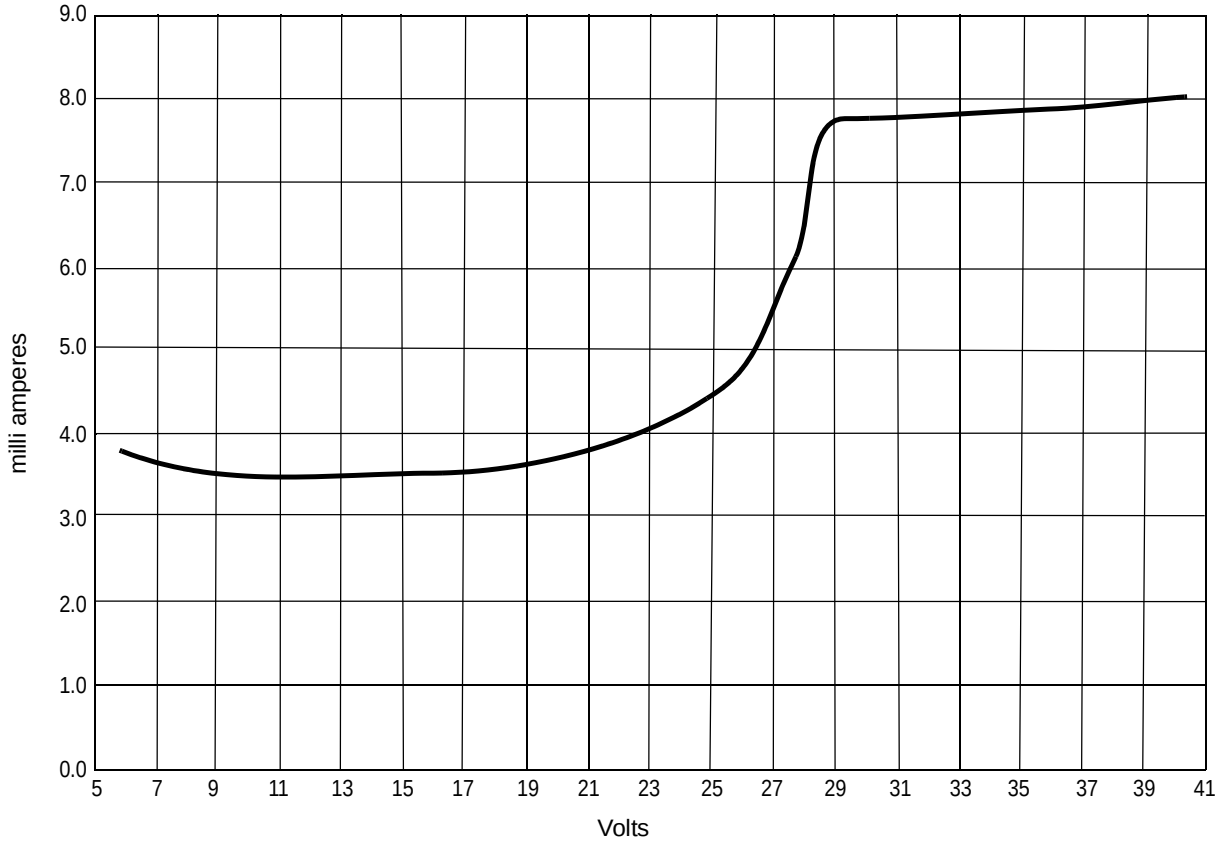


Figure 20. Typical Quiescent Supply Current Versus V+

FUNCTIONAL DESCRIPTION

INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic braking, and PWM control), in addition to the 5.0 A current capability, make the 33886 a very attractive, cost-effective solution for controlling a broad range of fractional horsepower DC motors. A pair of 33886 devices can be used to control bipolar stepper motors in both directions. In addition, the 33886 can be used to control permanent magnet solenoids in a push-pull variable force fashion using PWM control. The 33886 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 2, Simplified Internal Block Diagram, page 2, the 33886 is a fully protected monolithic H-Bridge with Fault Status reporting. For a DC motor to run the input conditions need be as follows: D1 input logic Low, $\overline{D2}$ input logic High, $\overline{FS}$ flag cleared (logic High), with one IN logic Low and the other IN logic High to define output polarity. The 33886 can execute dynamic braking by simultaneously turning on either both high-side MOSFETs or both low-side MOSFETs in the output H-Bridge; e.g., IN1 and IN2 logic High or IN1 and IN2 logic Low.

The 33886 outputs are capable of providing a continuous DC load current of 5.0 A from a 40 V V+ source. An internal charge pump supports PWM frequencies up to 10 kHz. An external pull-up resistor is required for the open drain $\overline{FS}$ pin for fault status reporting.

Two independent inputs (IN1 and IN2) provide control of the two totem-pole half-bridge outputs. Two disable inputs (D1 and $\overline{D2}$) are for forcing the H-Bridge outputs to a high impedance state (all H-Bridge switches OFF).

The 33886 has undervoltage shutdown with automatic recovery, active current limiting, output short-circuit latch-OFF, and overtemperature latch-OFF. An undervoltage shutdown, output short circuit latch-OFF, or overtemperature latch-OFF fault condition will cause the outputs to turn OFF (i.e., become high impedance or tri-stated) and the fault output flag to be set Low. Either of the Disable inputs or V+ must be “toggled” to clear the fault flag.

The short circuit/overtemperature shutdown scheme is unique and best described as using a junction temperature-dependent active current “fold back” protection scheme. When a short circuit condition is experienced, the current limited output is “ramped down” as the junction temperature increases above 160°C, until at 175°C the current has decreased to about 2.5 A. Above 175°C, overtemperature shutdown (latch-OFF) occurs. This feature allows the device to remain in operation for a longer time with unexpected loads, while still retaining adequate protection for both the device and the load.

FUNCTIONAL PIN DESCRIPTION

POWER/ANALOG GROUNDS (PGND AND AGND)

Power and analog ground pins. The power and analog ground pins should be connected together with a very low impedance connection.

POSITIVE POWER SUPPLY (V+)

V+ pins are the power supply inputs to the device. All V+ pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

V+ pins have an undervoltage threshold. If the supply voltage drops below a V+ undervoltage threshold, the output power stage switches to a tri-state condition and the fault status flag is set and the Fault Status pin voltage switched to a logic Low. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins and the fault status flag is automatically reset logic High.

FAULT STATUS ($\overline{FS}$)

This pin is the device fault status output. This output is an active Low open drain structure requiring a pull-up resistor to 5.0 V. Refer to Table 5, Truth Table, page 12.

LOGIC INPUT 1, 2 AND DISABLE1, 2 (IN1, IN2, D1, AND D2)

These pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complimentary inputs used to tri-state disable the H-Bridge outputs.

When either D1 or $\overline{D2}$ is set (D1 = logic High or $\overline{D2}$ = logic Low) in the disable state, outputs OUT1 and OUT2 are both tri-state disabled; however, the rest of the device circuitry is fully operational and the supply $I_{Q(standby)}$ current is reduced to a few milliamperes. Refer to Table 5, Truth Table, and Static Electrical Characteristics table, page 5.

H-BRIDGE OUTPUT 1, 2 (OUT1 AND OUT2)

These pins are the outputs of the H-Bridge with integrated output FET body diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The outputs have active current limiting above 6.5 A. The outputs also have thermal shutdown (tri-state latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time t_b) incorporated to detect currents that are higher than active current limit is activated at each output activation to facilitate detecting hard output short conditions (see Figure 9, page 9).

CHARGE PUMP CAPACITOR (CCP)

Charge pump output pin. A filter capacitor (up to 33 nF) can be connected from the C_{CP} pin and PGND. The device can operate without the external capacitor, although the C_{CP} capacitor helps to reduce noise and allows the device to perform at maximum speed, timing, and PWM frequency.

FUNCTIONAL DEVICE OPERATION

SHORT CIRCUIT PROTECTION

If an output short circuit condition is detected, the power outputs tri-state (latch-OFF) independent of the input (IN1 and IN2) states, and the fault status output flag is set logic Low. If the D1 input changes from logic High to logic Low, or if the $\overline{D2}$ input changes from logic Low to logic High, the output bridge will become operational again and the fault status flag will be reset (cleared) to a logic High state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature.

ACTIVE CURRENT LIMITING

The maximum current flow under normal operating conditions is internally limited to I_{LIM} (5.2 A to 7.8 A). When the maximum current value is reached, the output stages are tri-stated for a fixed time (t_a) of 20 μs typical. Depending on the time constant associated with the load characteristics, the current decreases during the tri-state duration until the next output ON cycle occurs (see Figures 9 and 12, page 9 and page 10, respectively).

The current limiting threshold value is dependent upon the device junction temperature. When -40°C < T_J < 160°C, I_{LIM} is between 5.2 A and 7.8 A. When T_J exceeds 160°C, the I_{LIM} current decreases linearly down to 2.5 A typical at 175°C. Above 175°C the device overtemperature circuit detects T_{LIM} and overtemperature shutdown occurs (see Figure 7, page 8). This feature allows the device to remain operational for a longer time but at a regressing output performance level at junction temperatures above 160°C.

OVERTEMPERATURE SHUTDOWN AND HYSTERESIS

If an overtemperature condition occurs, the power outputs are tri-state (latched-OFF) independent of the input signals and the fault status flag is set logic Low.

To reset from this condition, D1 must change from logic High to logic Low, or $\overline{D2}$ must change from logic Low to logic High. When reset, the output stage switches ON again, provided that the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Note Resetting from the fault condition will clear the fault status flag.

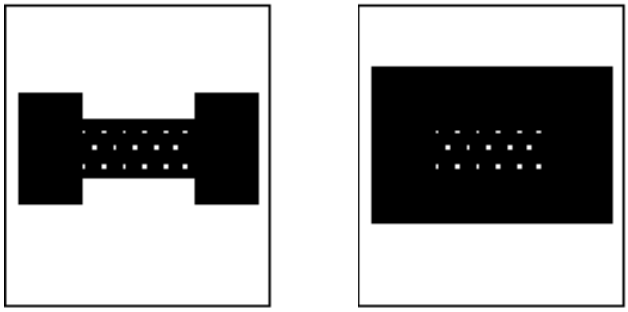
MAIN DIFFERENCES COMPARED TO MC33186DH1

- COD pin has been removed. Pin 8 is now a Do Not Connect (DNC) pin.
- Pin 20 is no longer connected in the 20 HSOP package. It is now a DNC pin.
- $R_{DS(ON)}$ max at T_J = 150°C is now 225 mΩ per each output transistor.
- Maximum temperature operation is now 160°C, as minimum thermal shutdown temperature has increased.
- Current regulation limiting foldback is implemented above 160°C T_J.
- Thermal resistance junction to case has been increased from ~2.0°C/W to ~5.0°C/W.

PERFORMANCE

The 33886 is designed for enhanced thermal performance. The significant feature of this device is the exposed copper pad on which the power die is soldered. This pad is soldered on a PCB to provide heat flow to ambient and also to provide thermal capacitance. The more copper area on the PCB, the better the power dissipation and transient behavior will be.

Example Characterization on a double-sided PCB: bottom side area of copper is 7.8 cm^2; top surface is 2.7 cm^2 (see Figure 21); grid array of 24 vias 0.3 mm in diameter.



Top Side Bottom Side

Figure 21. PCB Test Layout

Figure 22 shows the thermal response with the device soldered on to the test PCB described in Figure 21.

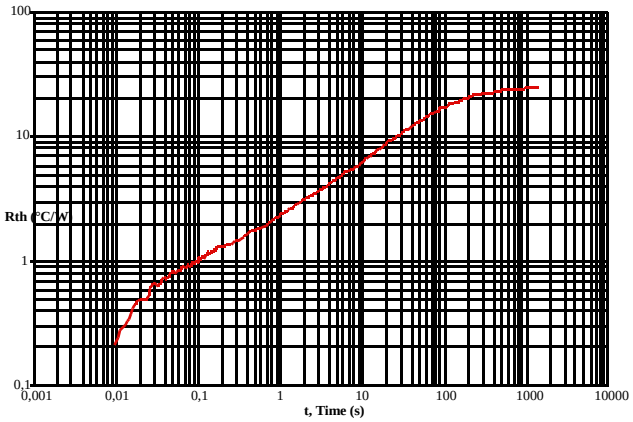


Figure 22. 33886 Thermal Response

TYPICAL APPLICATIONS

A typical application schematic is shown in Figure 23. For precision high-current applications in harsh, noisy environments, the V+ by-pass capacitor may need to be substantially larger.

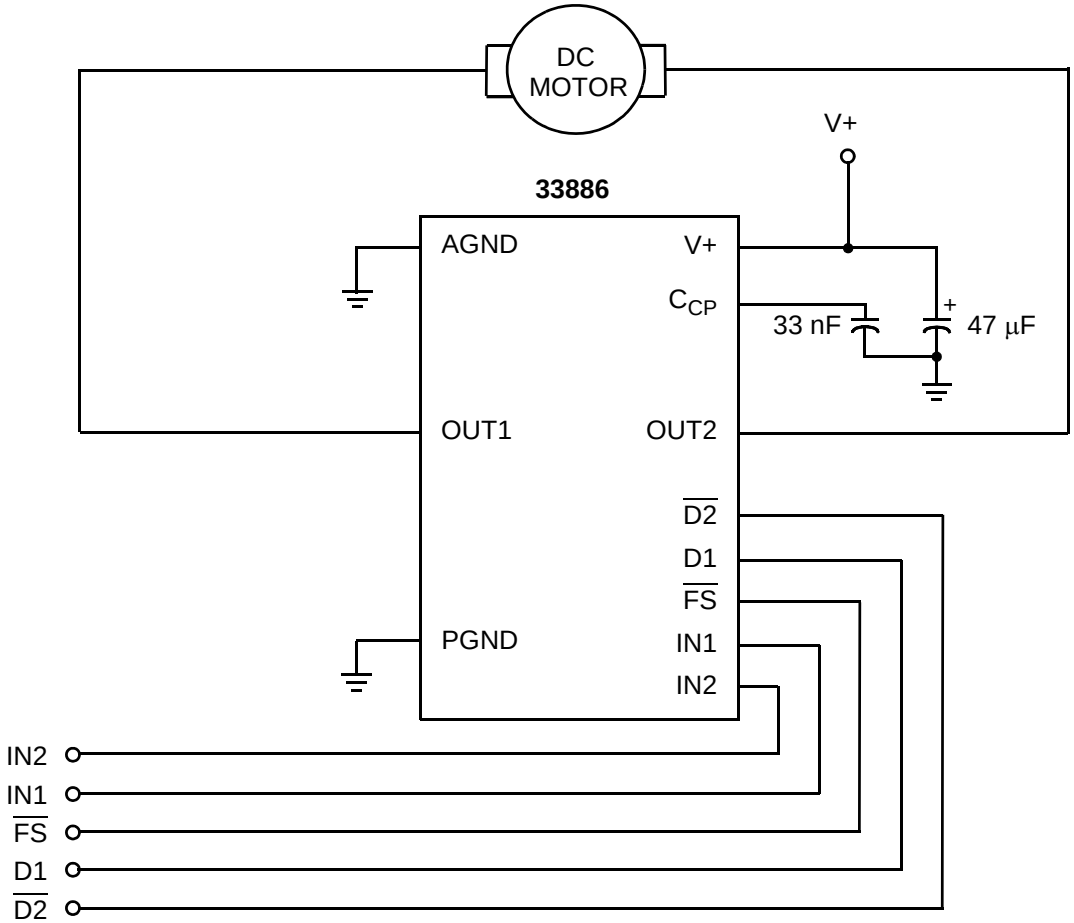


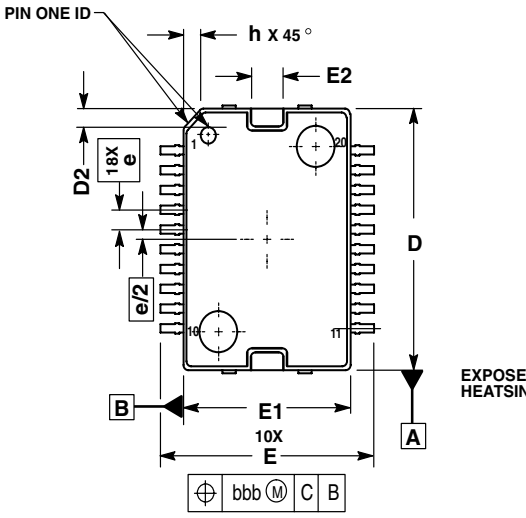
Figure 23. 33886 Typical Application Schematic

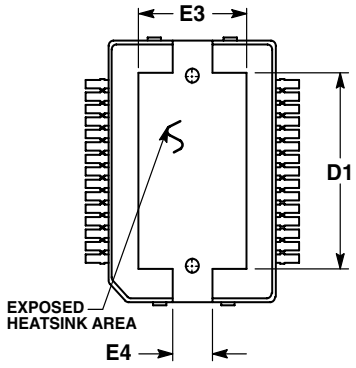
PACKAGING

PACKAGE DIMENSIONS

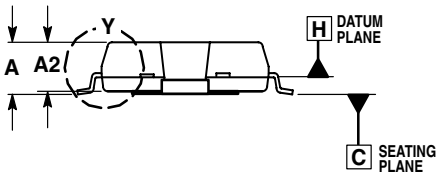
Important For the most current revision of the package, visit www.freescale.com and perform a keyword search on **98ASH70702A** listed below.

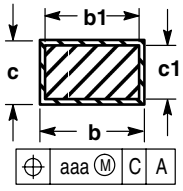
DH SUFFIX
VW (Pb-FREE) SUFFIX
20-PIN HSOP
PLASTIC PACKAGE
98ASH70702A
ISSUE A



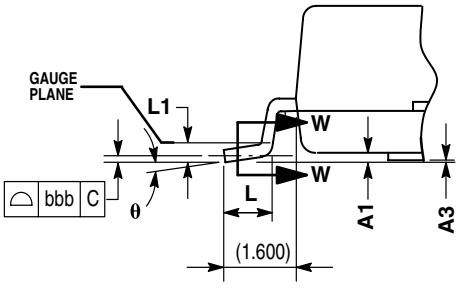


BOTTOM VIEW





SECTION W–W



DETAIL Y

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

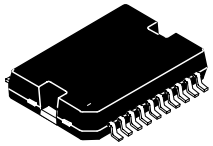
	MILLIMETERS	
DIM	MIN	MAX
A	3.000	3.400
A1	0.100	0.300
A2	2.900	3.100
A3	0.00	0.100
D	15.800	16.000
D1	11.700	12.600
D2	0.900	1.100
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	6.400	7.200
E4	2.700	2.900
L	0.840	1.100
L1	0.350 BSC	
b	0.400	0.520
b1	0.400	0.482
c	0.230	0.320
c1	0.230	0.280
e	1.270 BSC	
h	—	1.100
θ	0 °	8 °
aaa	0.200	
bbb	0.100	

33886

5.0 A H-BRIDGE

33886

**20-PIN
HSOP-EP**



**DH SUFFIX
VW (Pb-FREE) SUFFIX
98ASH70702A
20-PIN HSOP-EP**

Note For package dimensions, refer to the 33886 device data sheet.

THERMAL ADDENDUM - REVISION 2.0

Introduction

This thermal addendum is provided as a supplement to the MC33186 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the data sheet.

Packaging and Thermal Considerations

The MC33186 is offered in a 20 pin HSOP exposed pad, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$$\{ T_J \} = [R_{\theta JA}] \cdot \{ P \}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 6. Thermal Performance Comparison

Thermal Resistance	[°C/W]
$R_{\theta JA}$ (1)(2)	20
$R_{\theta JB}$ (2)(3)	6.0
$R_{\theta JA}$ (1)(4)	52
$R_{\theta JC}$ (5)	1.0

NOTES:

1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad surface; cold plate attached to the package bottom side, remaining surfaces insulated.

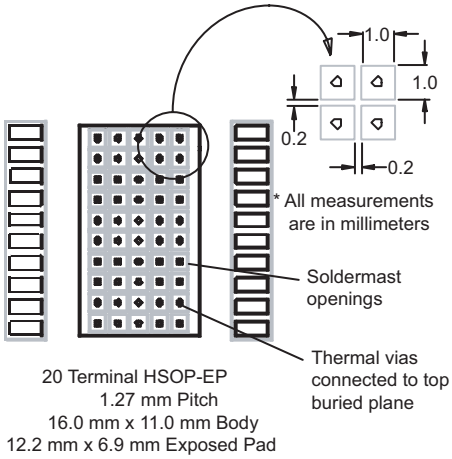


Figure 24. Thermal Land Pattern for Direct Thermal Attachment According to JESD51-5

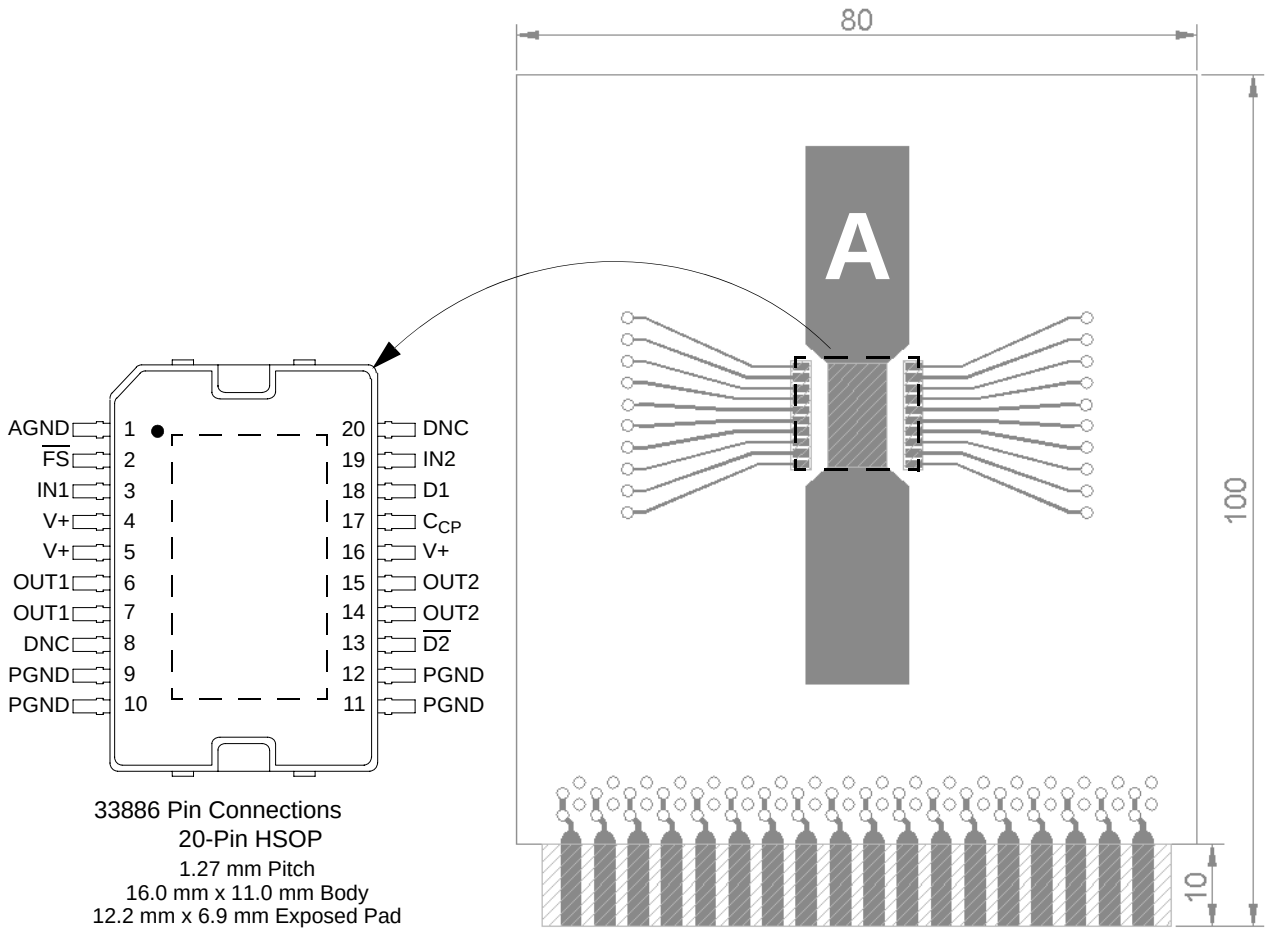


Figure 25. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 7. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	°C/W
$R_{\theta JA}$	0.0	52
	300	36
	600	32
$R_{\theta JS}$	0.0	10
	300	7.0
	600	6.0

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JS}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package (see Figure 25).

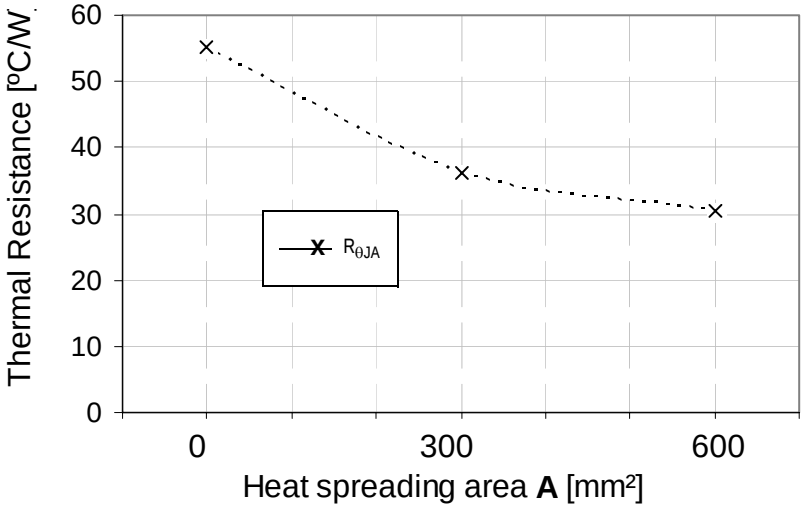


Figure 26. Device on Thermal Test Board $R_{\theta JA}$

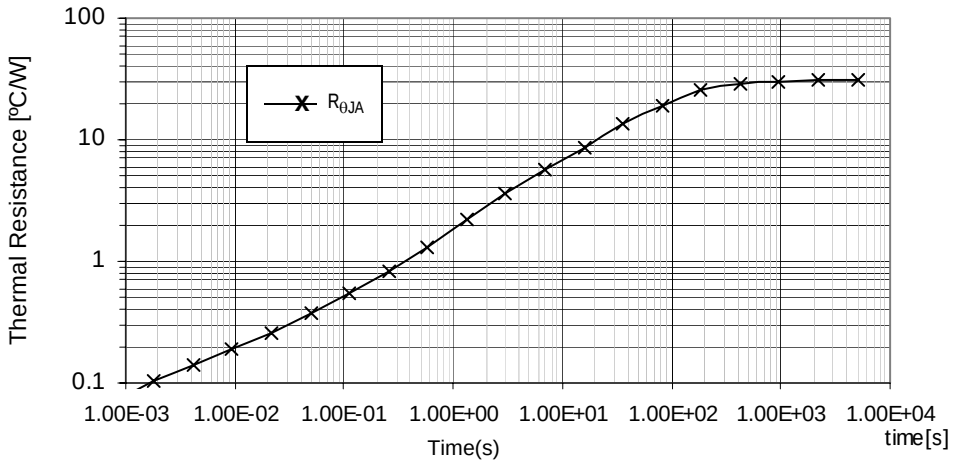


Figure 27. Transient Thermal Resistance $R_{\theta JA}$
Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	7/2005	• Implemented Revision History page • Added Thermal Addendum • Converted to Freescale format
8.0	2/2007	• Updated data sheet format • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. Added note with instructions to obtain this information from www.freescale.com.

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