

FUJITSU SEMICONDUCTOR

FR50
32-BIT MICROCONTROLLER
MB91F367GA/F368GA
Datasheet

Release 1.0 10-Apr-2001

Revision History

| Revision | Date | Item |
|-----------------|-------------|---|
| 1.0 | 10-Apr-2001 | First revision of preliminary datasheet for MB91F367GA and MB91F368GA |

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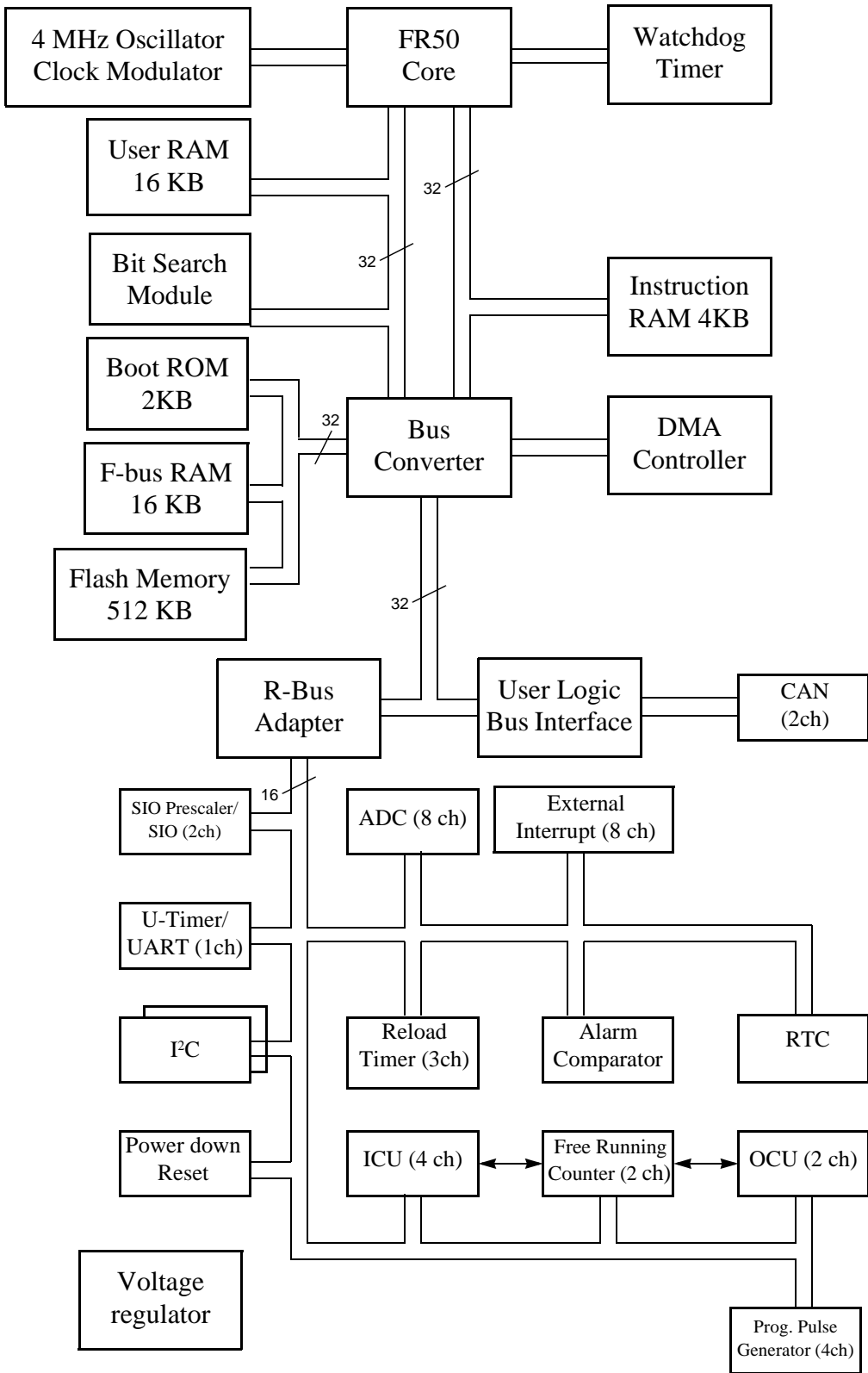
CHAPTER 1 MB91F367GA/F368GA Overview

This device is available in two options. The difference between these options is as follows:

| Feature | MB91F367GA | MB91F368GA |
|------------|-------------------------------|--|
| RTC module | connected to 4 MHz oscillator | connected to 32kHz oscillator at pins 27, 28 calibration unit available |

See the following chapters for more details:

1.1 MB91F367GA Block Structure



1.3 Core Functionality

| Function | Feature | Remarks |
|--|--|---|
| FR50 Core | 32-bit Fujitsu RISC Core FR30 software compatible | |
| Clock module (clock control, clock divider, PLLs) | Setting of frequencies for CPU and peripherals (see MB91FV360GA) Low power consumption modes: <u>RTC mode</u> : only the Real Time Clock and the selected oscillator are active (= STOP mode and bit 0 of STCR is set to 0) <u>STOP mode</u> : all internal circuits and the oscillation circuits are halted | |
| Watchdog | adjustable watchdog timer interval (between 2^{20} and 2^{26} system clock cycles) | |
| I-RAM 4 kB | I-RAM | see remark below table |
| D-bus RAM 16 kB | RAM for user data | see remark below table |
| F-bus RAM 16 kB | RAM for data and code | see remark below table |
| Flash Memory 512 kB | sector architecture: sector 0: 64 kB sector 7: 64 kB sector 1: 64 kB sector 8: 64 kB sector 2: 64 kB sector 9: 64 kB sector 3: 32 kB sector 10: 32 kB sector 4: 8 kB sector 11: 8 kB sector 5: 8 kB sector 12: 8 kB sector 6: 16 kB sector 13: 16 kB V V 16 bit 16 bit write access is 16 bit wide, read access can be 16 or 32 bit wide | connected to F-Bus Minimum 10000 program/erase cycles Minimum 10 years data retention Net read cycle time to the memory is 40nS. For overall access time see settings in Chapter 2.1 |
| Boot ROM 2 kB | | |
| DMA | 5 channels up to 16 DMA sources can be used transfer modes: single/block, burst, continuous | |

| | | |
|----------------------|--|------------------------|
| Interrupt Controller | 8 external interrupt channels, 38 internal interrupts, 16 programmable priority levels | |
| Bit Search Module | Searches a word for the position of the first "1" and "0" change bit, starting from the MSB. Performs the search in 1 cycle. | |
| Fixed Reset Vector | Hardwired reset and mode vector | Code start at 0F:4000H |
| Voltage Regulator | Generates internal voltage of 3.3 V | |

Remark:

Set bit 9 (SYNCR) of TBCR to 1 to enable the synchronisation of the reset signal; a reset will be generated only after all bus accesses have been done. This avoids that erroneous data are written into the RAMs during reset.

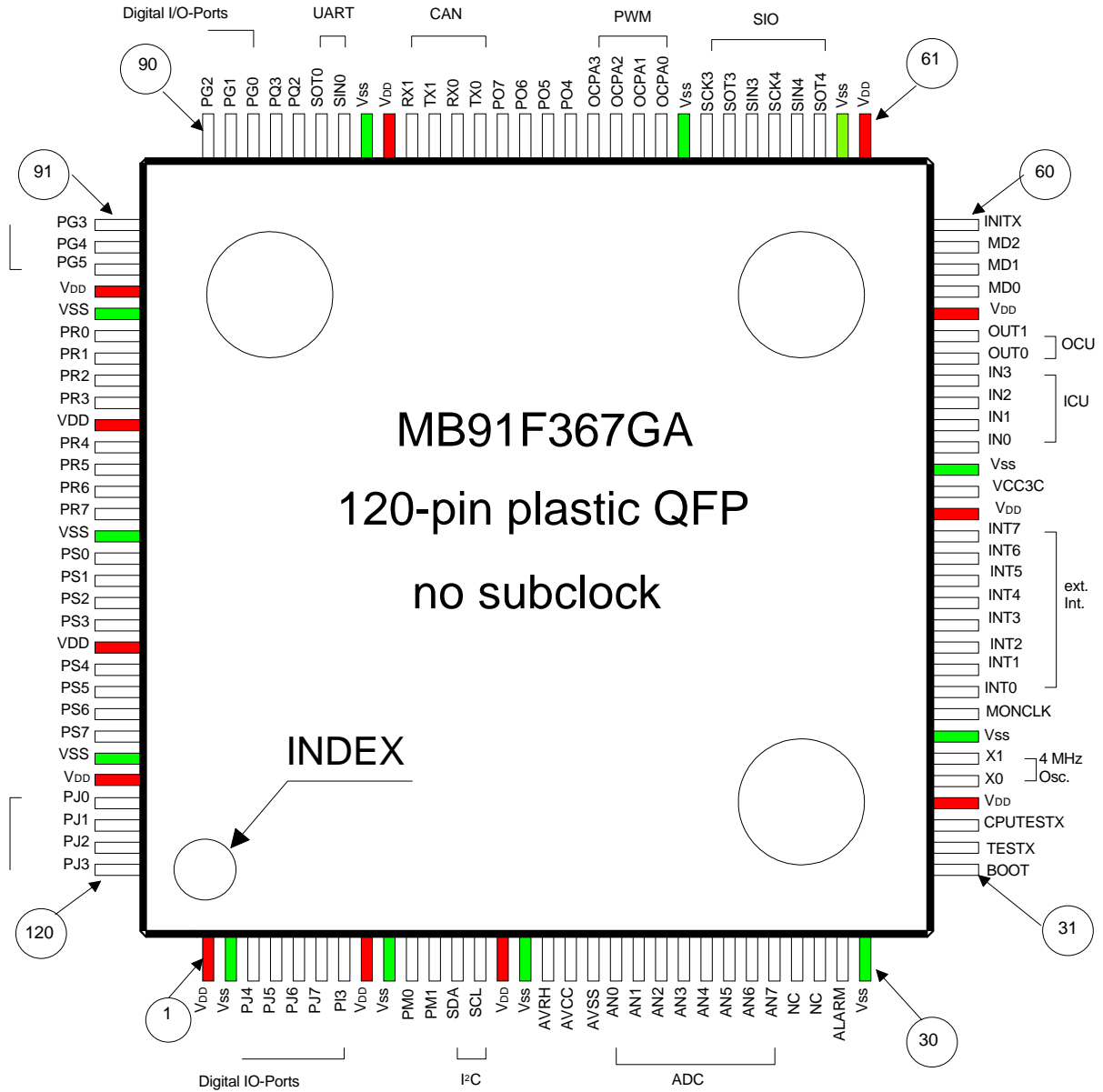
1.4 Features

| Function | Feature | Remarks |
|--------------------------------------|---|------------------------------------|
| PPG for dimmer (4 channels) | <p>16-bit PWM Timer 16 bit down counter, cycle and duty setting registers interrupt at triggering, cycle or duty match can be triggered by software or reload timer PWM operation and one-shot operation</p> <p>Clock disable</p> <p>internal prescaler allows $f_{RES}/1$, $f_{RES}/4$, $f_{RES}/16$, $f_{RES}/64$ as counter clock</p> | required frequencies are 90-300 Hz |
| ADC (8 channels) | <p>successive approximation, internal sample and hold circuit 10-bit resolution, 5 V operation, (conversion time: 178 cycles of CLKP) program selectable analogue input channels: single conversion mode continuous conversion mode stop conversion mode</p> <p>interrupt at the end of a conversion can be used to activate DMA transfer</p> <p>activation by software</p> <p>Prescaling is done internally</p> <p>Clock disable</p> | |
| Basic Interval Timer (3 channels) | 16-bit reload timer, includes clock prescaler ($f_{RES}/2^1$, $f_{RES}/2^3$, $f_{RES}/2^5$) | |
| CAN (2 channels) | <p>conforms to CAN specification version 2.0 A and B automatic re-transmission in case of error automatic transmission responding to remote frame prioritized 16 message buffers for data and IDs supports multiple messages flexible configuration of acceptance filtering: full bit compare / full bit mask / two partial bit masks supports up to 1 Mb/s Clock Disable</p> | CAN allows TSEG2 = RSJW setting |

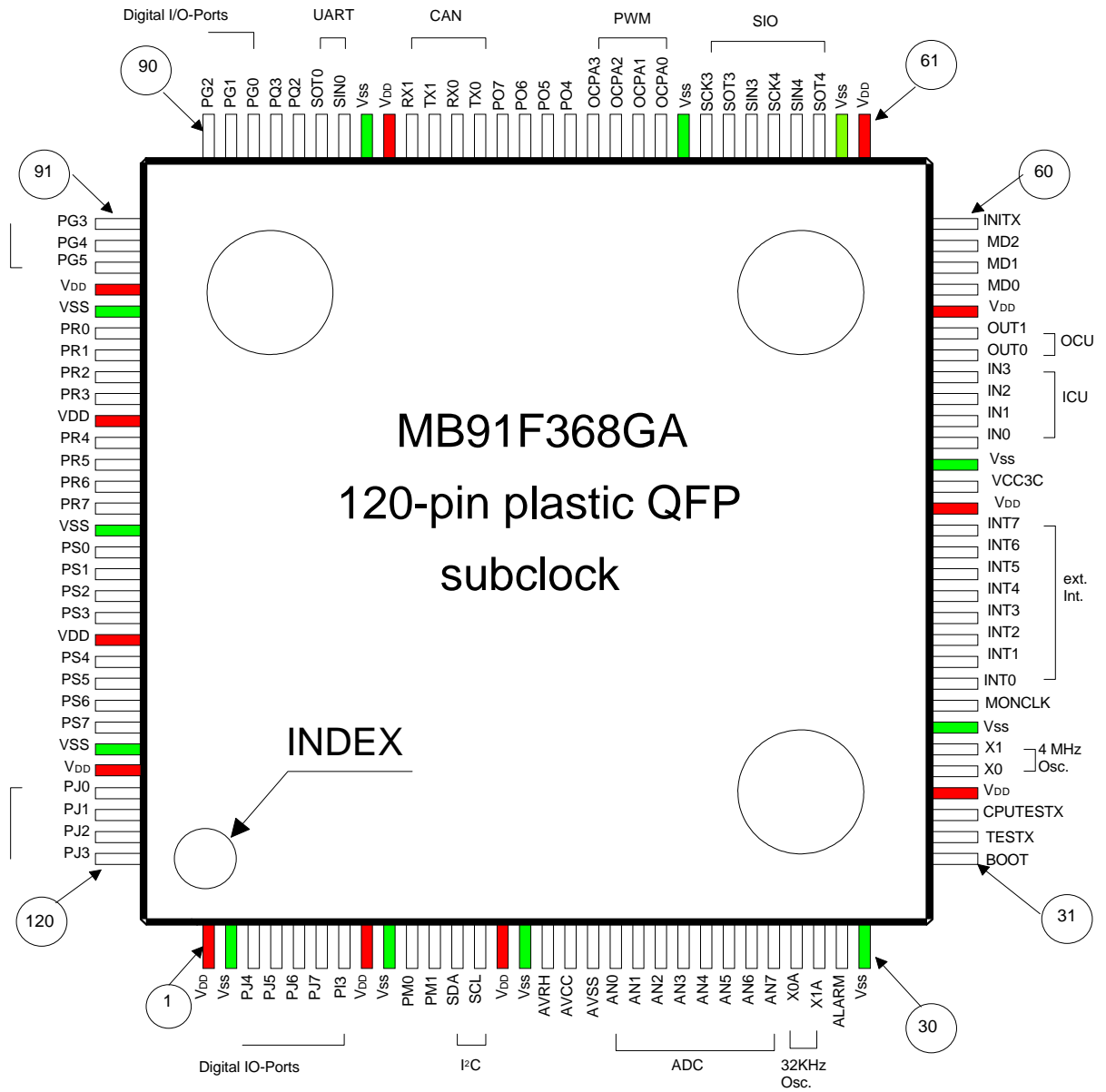
| | | |
|---|--|--|
| External Interrupt (8 channels) | can be programmed to be edge sensitive or level sensitive interrupt masking and request pending bits per channel | |
| I ² C-1 for standard mode | master or slave transmission arbitration function clock synchronization function slave address and general call address detect function transfer direction detect function start condition repeat generation and detection function bus error detect function compatible to I ² C standard mode specifi- cation (operation up to 100 kHz, 7 bit addressing) includes clock divider functionality Clock disable | Only I ² C-1 or I ² C-2 can be used, not both in parallel. Bit 0 of F362MD will be used to decide which module is connected to the SCL and SDA pads. By default it is I ² C-1. |
| I ² C-2 for standard and fast mode | master or slave transmission arbitration function clock synchronization function slave address and general call address detect function transfer direction detect function start condition repeat generation and detection function bus error detect function compatible to I ² C standard and fast mode specification (operation up to 400 kHz, 10 bit addressing) includes clock divider functionality Clock disable | Only I ² C-1 or I ² C-2 can be used, not both in parallel. Bit 0 of F362MD will be used to decide which module is connected to the SCL and SDA pads. By default it is I ² C-1. SCL and SDA lines include optional noise filter. The noise filter allows the suppression of spikes in the range of 1 to 1.5 cycles of CLKP. Communication on the I2C bus between other connected devices is not possible if MB91F36xGA is not connected to the power supply. |
| 16-bit Input Capture (ICU) (4 channels) | rising edge, falling edge or rising & falling edge sensitive two 16-bit capture registers signals an interrupt at external event Clock disable | |
| 16-bit Output Compare OCU (2 channels) | signals an interrupt when a match with of 16-bit IO timer occurs an output signal can be generated Clock disable | |

| | | |
|--|---|--|
| <p>Real Time Clock (RTC) (Watch Timer)</p> | <p>facility to correct oscillation deviation read/write accessible second/minute/ hour registers can signal interrupts every second/ minute/hour/day</p> <p>internal clock divider and prescaler provide exact 1s clock this clock is based on the 4 MHz oscillator or if the subclock option is selected on the 32 kHz subclock</p> <p>Clock disable</p> | <p>prescaler values are 1E847FH , and 4000H for 4MHz and 32.768KHz respectively.</p> |
| <p>32KHz subclock + calibration unit</p> | <p>In RTC mode, the RTC module can be driven by either 4MHz or 32KHz oscillator, depending on the configuration.</p> <p>Additional hardware which allows calibration of the 32KHz clock based on the 4MHz clock is built in.</p> | <p>This function is only available on MB91F368GA.</p> |

1.5 Pin Assignment MB91F367GA



1.6 Pin Assignment MB91F368GA



1.7 I/O Pins and Their Functions

Table 1.7a Pinning

| Pin No. QFP120 | Pin Name | I/O | General Purpose I/O Port | Circuit Type | Function |
|-------------------|-----------|-----|--------------------------------|-----------------|------------------------------------|
| 1 | VDD | | | | |
| 2 | VSS | | | | |
| 3 | PJ4 | I/O | PJ4 | A | Digital IO-Port |
| 4 | PJ5 | I/O | PJ5 | A | Digital IO-Port |
| 5 | PJ6 | I/O | PJ6 | A | Digital IO-Port |
| 6 | PJ7 | I/O | PJ7 | A | Digital IO-Port |
| 7 | PI3 | I/O | PI3 | A | Digital IO-Port |
| 8 | VDD | | | | |
| 9 | VSS | | | | |
| 10 | PM0 | I/O | PM0 | A | Digital IO-Port |
| 11 | PM1 | I/O | PM1 | A | Digital IO-Port |
| 12 | SDA | I/O | PM2 | Y | I2C SDA (no internal pull-up!) |
| 13 | SCL | I/O | PM3 | Y | I2C SCL (no internal pull-up!) |
| 14 | VDD | | | | |
| 15 | VSS | | | | |
| 16 | AVRH | | | R | Analog Voltage Ref. high |
| 17 | AVCC | | | | Analog VCC |
| 18 | AVSS/AVRL | | | | Ana.Volt.Ref.low/An.VSS |
| 19 | AN0 | I/O | PH0 | B | ADC input |
| 20 | AN1 | I/O | PH1 | B | ADC input |
| 21 | AN2 | I/O | PH2 | B | ADC input |
| 22 | AN3 | I/O | PH3 | B | ADC input |
| 23 | AN4 | I/O | PH4 | B | ADC input |
| 24 | AN5 | I/O | PH5 | B | ADC input |
| 25 | AN6 | I/O | PH6 | B | ADC input |
| 26 | AN7 | I/O | PH7 | B | ADC input |
| 27 | X0A | I | | I | 32 KHz Oscillator Pin (MB91F368GA) |
| | N.C. | | | | not connected (MB91F367GA) |
| 28 | X1A | O | | I | 32 KHz Oscillator Pin (MB91F368GA) |
| | N.C. | | | | not connected (MB91F367GA) |
| 29 | ALARM | I | | D | Alarm Comparator Input |
| 30 | VSS | | | | |
| 31 | BOOT | I/O | P93 | A | BOOT pin |
| 32 | TESTX | I | | E | Test mode pin |
| 33 | CPUTESTX | I | | E | Test mode pin |
| 34 | VDD | | | | |
| 35 | X0 | I | | H | 4 MHz Oscillator Pin |
| 36 | X1 | O | | H | 4 MHz Oscillator Pin |
| 37 | VSS | | | | |
| 38 | MONCLK | O | | G | Clock output |
| 39 | INT0 | I/O | PK0 | A | Ext. Interrupt |
| 40 | INT1 | I/O | PK1 | A | Ext. Interrupt |
| 41 | INT2 | I/O | PK2 | A | Ext. Interrupt |
| 42 | INT3 | I/O | PK3 | A | Ext. Interrupt |

Table 1.7a Pinning

| Pin No. QFP120 | Pin Name | I/O | General Purpose I/O Port | Circuit Type | Function |
|-------------------|----------|-----|--------------------------------|-----------------|---|
| 43 | INT4 | I/O | PK4 | A | Ext. Interrupt |
| 44 | INT5 | I/O | PK5 | A | Ext. Interrupt |
| 45 | INT6 | I/O | PK6 | A | Ext. Interrupt |
| 46 | INT7 | I/O | PK7 | A | Ext. Interrupt |
| 47 | VDD | | | A | supply pin for internal voltage regulator |
| 48 | VCC3/C | | | | Capacitor pin for V. reg. |
| 49 | VSS | | | | |
| 50 | IN0 | I/O | PL0 | A | ICU input |
| 51 | IN1 | I/O | PL1 | A | ICU input |
| 52 | IN2 | I/O | PL2 | A | ICU input |
| 53 | IN3 | I/O | PL3 | A | ICU input |
| 54 | OUT0 | I/O | PL4 | A | OCU Output |
| 55 | OUT1 | I/O | PL5 | A | OCU Output |
| 56 | VDD | | | | supply pin for internal voltage regulator |
| 57 | MD0 | I | | T | Mode Pin |
| 58 | MD1 | I | | T | Mode Pin |
| 59 | MD2 | I | | T | Mode Pin |
| 60 | INITX | I | | U | Initial |
| 61 | VDD | | | | supply pin for internal voltage regulator |
| 62 | VSS | | | | |
| 63 | SOT4 | I/O | PN0 | A | SIO output |
| 64 | SIN4 | I/O | PN1 | A | SIO input |
| 65 | SCK4 | I/O | PN2 | A | SIO clock |
| 66 | SIN3 | I/O | PN3 | A | SIO input |
| 67 | SOT3 | I/O | PN4 | A | SIO output |
| 68 | SCK3 | I/O | PN5 | A | SIO clock |
| 69 | VSS | | | | |
| 70 | OCPA0 | I/O | PO0 | A | PPG output |
| 71 | OCPA1 | I/O | PO1 | A | PPG output |
| 72 | OCPA2 | I/O | PO2 | A | PPG output |
| 73 | OCPA3 | I/O | PO3 | A | PPG output |
| 74 | PO4 | I/O | PO4 | A | Digital IO-Port |
| 75 | PO5 | I/O | PO5 | A | Digital IO-Port |
| 76 | PO6 | I/O | PO6 | A | Digital IO-Port |
| 77 | PO7 | I/O | PO7 | A | Digital IO-Port |
| 78 | TX0 | I/O | PP0 | Q | CAN TX output |
| 79 | RX0 | I/O | PP1 | Q | CAN RX output |
| 80 | TX1 | I/O | PP2 | Q | CAN TX output |
| 81 | RX1 | I/O | PP3 | Q | CAN RX output |
| 82 | VDD | | | | |
| 83 | VSS | | | | |
| 84 | SIN0 | I/O | PQ0 | A | UART input |
| 85 | SOT0 | I/O | PQ1 | A | UART output |
| 86 | PQ2 | I/O | PQ2 | A | Digital IO-Port |
| 87 | PQ3 | I/O | PQ3 | A | Digital IO-Port |
| 88 | PG0 | I/O | PG0 | A | Digital IO-Port |
| 89 | PG1 | I/O | PG1 | A | Digital IO-Port |

Table 1.7a Pinning

| Pin No. QFP120 | Pin Name | I/O | General Purpose I/O Port | Circuit Type | Function |
|-------------------|----------|-----|--------------------------------|-----------------|-----------------------|
| 90 | PG2 | I/O | PG2 | A | Digital IO-Port |
| 91 | PG3 | I/O | PG3 | A | Digital IO-Port |
| 92 | PG4 | I/O | PG4 | A | Digital IO-Port |
| 93 | PG5 | I/O | PG5 | A | Digital IO-Port |
| 94 | VDD | | | | |
| 95 | VSS | | | | |
| 96 | PR0 | I/O | PR0 | K1 | Digital IO-Port |
| 97 | PR1 | I/O | PR1 | K1 | Digital IO-Port |
| 98 | PR2 | I/O | PR2 | K1 | Digital IO-Port |
| 99 | PR3 | I/O | PR3 | M1 | Digital IO-Port |
| 100 | HVDD | | | | VDD for ports R and S |
| 101 | PR4 | I/O | PR4 | K1 | Digital IO-Port |
| 102 | PR5 | I/O | PR5 | K1 | Digital IO-Port |
| 103 | PR6 | I/O | PR6 | K1 | Digital IO-Port |
| 104 | PR7 | I/O | PR7 | M1 | Digital IO-Port |
| 105 | VSS | | | | |
| 106 | PS0 | I/O | PS0 | K1 | Digital IO-Port |
| 107 | PS1 | I/O | PS1 | K1 | Digital IO-Port |
| 108 | PS2 | I/O | PS2 | K1 | Digital IO-Port |
| 109 | PS3 | I/O | PS3 | M1 | Digital IO-Port |
| 110 | HVDD | | | | VDD for ports R and S |
| 111 | PS4 | I/O | PS4 | K1 | Digital IO-Port |
| 112 | PS5 | I/O | PS5 | K1 | Digital IO-Port |
| 113 | PS6 | I/O | PS6 | K1 | Digital IO-Port |
| 114 | PS7 | I/O | PS7 | M1 | Digital IO-Port |
| 115 | VSS | | | | |
| 116 | VDD | | | | |
| 117 | PJ0 | I/O | PJ0 | A | Digital IO-Port |
| 118 | PJ1 | I/O | PJ1 | A | Digital IO-Port |
| 119 | PJ2 | I/O | PJ2 | A | Digital IO-Port |
| 120 | PJ3 | I/O | PJ3 | A | Digital IO-Port |

Remark: Pin 31 (BOOT) should be low by default (pull down resistor).

To avoid disturbances in case of reset/boot it should preferably only be used as output by any application.

Table 1.7b Circuit Types

| Circuit Type | Description |
|--------------|---|
| A | I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Schmitt-Trigger Input, STOP control |
| B | I/O, IOH=4 mA / IOL=4 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control |
| D | Analog Input |
| E | CMOS Schmitt-Trigger Input, 50K Pull-up |
| G | Tristate Output, IOH=4 mA / IOL=4 mA |
| H | 4 MHz Oscillator Pin |
| I | 32KHz Oscillator Pin |
| K1 | I/O, IOH=30 mA / IOL=30 mA, CMOS Automotive Schmitt-Trigger Input, STOP control |
| M1 | I/O, IOH=30 mA / IOL=30 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control |
| Q | I/O, IOH=4 mA / IOL=4 mA, CMOS Input, STOP control |
| R | AVRH Input |
| T | CMOS Input, can withstand VID for flash programming |
| U | CMOS Schmitt-Trigger Input, 50K Pull-up |
| Y | I/O, IOH=3mA / IOL=3mA (I2C), CMOS Input, STOP control |

1.8 Flash Memory Mode of MB91F367GA/F368GA

To enter the flash memory mode set mode pins MD0 to MD2 to “111”. Assert INITX for at least 500 ns to enter this mode.

The following tables show the pins which are required for the programming procedure and also describe the states for the pins not used in flash memory mode. Most of the not used pins are in their reset state (high-Z outputs, enabled inputs). To prevent misbehavior or damage these pins must be tied to VDD or VSS through resistors - see following tables for details.

Aside from the functional pins described below all power pins should be connected to a power supply in the specified range, capacitances should be connected to the VCC3C pin as recommended.

Table 1: Flash Control Signals

| MB91F367GA/F368GA | | | MBM29LV400C | Notes |
|-------------------|-----------------|---------------------|--------------------------|---------|
| Pin number | Normal function | Flash Memory mode | | |
| 31 | BOOT | \overline{WE} | \overline{WE} | |
| 32 | TESTX | \overline{BYTE} | \overline{BYTE} | |
| 33 | CPUTESTX | TMODX | | pull up |
| 38 | MONCLK | RY/ \overline{BY} | RY/ \overline{BY} | |
| 39-46 | INT0-INT7 | D24 to D31 | DQ8 to DQ15 | |
| 50 | IN0 | \overline{CE} | \overline{CE} | |
| 51 | IN1 | \overline{OE} | \overline{OE} | |
| 52 | IN2 | D20 | DQ4 | |
| 53 | IN3 | D21 | DQ5 | |
| 54 | OUT0 | D22 | DQ6 | |
| 55 | OUT1 | D23 | DQ7 | |
| 57 | MD0 | VDA9 | A9 (VID) | |
| 58 | MD1 | VDRS | \overline{RESET} (VID) | |
| 59 | MD2 | VDOE | \overline{OE} (VID) | |
| 60 | INITX | \overline{RESET} | \overline{RESET} | |
| 91-93 | PG3-PG5 | A16-A18 | A15-A17 | |
| 96 | PR0 | A0 | A-1 | |
| 97 | PR1 | A1 | A0 | |
| 98 | PR2 | A2 | A1 | |
| 99 | PR3 | A3 | A2 | |

Table 1: Flash Control Signals

| MB91F367GA/F368GA | | | MBM29LV400C | Notes |
|-------------------|-----------------|-------------------|-------------|-------|
| Pin number | Normal function | Flash Memory mode | | |
| 101 | PR4 | A4 | A3 | |
| 102 | PR5 | A5 | A4 | |
| 103 | PR6 | A6 | A5 | |
| 104 | PR7 | A7 | A6 | |
| 106 | PS0 | A8 | A7 | |
| 107 | PS1 | A9 | A8 | |
| 108 | PS2 | A10 | A9 | |
| 109 | PS3 | A11 | A10 | |
| 111 | PS4 | A12 | A11 | |
| 112 | PS5 | A13 | A12 | |
| 113 | PS6 | A14 | A13 | |
| 114 | PS7 | A15 | A14 | |
| 117 to 120 | PJ0-PJ3 | D16 to D19 | DQ0 to DQ3 | |

Table 2: Pins not used in Flash Memory Mode

| MB91F367GA/F368GA | | | |
|-------------------|-----------------|-----------|------------|
| Pin number | Normal function | Pin State | Notes |
| 35 | X0 | input | pull up |
| 36 | X1 | output | leave open |
| 66 | SIN3 | output | leave open |
| 67 | SOT3 | output | leave open |
| 68 | SCK3 | output | leave open |
| 27 | X0A | input | pull up |
| 28 | X1A | output | leave open |
| 29 | ALARM | input | pull up |
| all other signals | | input | pull up |

CHAPTER 2 Additional information

2.1 Flash Interface

2.1.2 Flash Control Status Register (FMCS)

| address | bit 7 | bit6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|----------------------|--------|------|-------|-------|-------|-------|-------|-------|
| 00007000H | FACCEN | ---- | ---- | RDYEG | RDY | RDYI | WE | LPM |
| access | R/W | R/W | R/W | R | R | R/W | R/W | R/W |
| initial value | 1 | 1 | 1 | 0 | X | 0 | 0 | 0 |
| value after Boot ROM | 0 | 1 | 1 | 0 | X | 0 | 0 | 0 |

Bit 7: FACCEN: Controls read access mode to flash

- 0: Synchronous read access using ATDIN and EQIN signals - recommended setting
- 1: Asynchronous read access

Bits 6,5: reserved

when writing to these bits always write "11"

Bit 4: RDYEG:

When the auto algorithm of flash memory is finished, this bit is set to '1'.

This bit is cleared by reading it.

0: Auto algorithm not yet finished

1: Auto algorithm finished

Bit 3: RDY:

The state of auto algorithm

0: The state of the auto algorithm is WRITE/READ. Can't accept WRITE/READ/DELETE.

1: It is possible to accept WRITE/READ/DELETE.

Bit 2: RDYI: Reserved bit

Bit 1: WE: This bit is used to control writing and reading to flash memory in CPU mode

0: writing to flash memory is disabled, read access is 32 bit wide

1: writing enabled, read access 16 bit wide, auto algorithm can be used

This bit can only be written to if RDY is 1.

Bit 0: LPM:

0: normal mode

1: low power mode, can be used when CPU frequency is below 5 MHz

2.1.3 Flash Wait Control Register (FMWT)

| address | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0000700 4H | ---- | ---- | FAC1 | FAC0 | EQINH | WTC2 | WTC1 | WTC0 |
| access | | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| initial value | | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| value after Boot ROM | | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

Bit 6: This bit is reserved, always set this bit to "0" when writing to this register.

Bits 5,4: These bits control the length of the high pulse for the ATDIN signal

| FAC1 | FAC0 | length of high pulse for ATDIN |
|------|------|--------------------------------|
| 0 | 0 | 0.5 cycles of CLKB |
| 0 | 1 | 1 cycle of CLKB |
| 1 | 0 | 1.5 cycles of CLKB |
| 1 | 1 | 2 cycles of CLKB |

Bit 3: EQINH: This bit controls the falling edge of the EQIN signal.

0: falling edge of EQIN at falling edge of FWAITR;

1: falling edge of EQIN half cycle after falling edge of FWAITR;

Bit 2,1,0: WTC2,1,0: Wait Cycle bits

WTC2-0 are used to insert auto wait cycles for flash memory access.

| WTC2 | WTC1 | WTC0 | wait cycles |
|------|------|------|-------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |

| WTC2 | WTC1 | WTC0 | wait cycles |
|------|------|------|-------------|
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

Recommended settings for FAC1, FAC0 and WTC2 to WTC0 for **read** access to the flash memory:

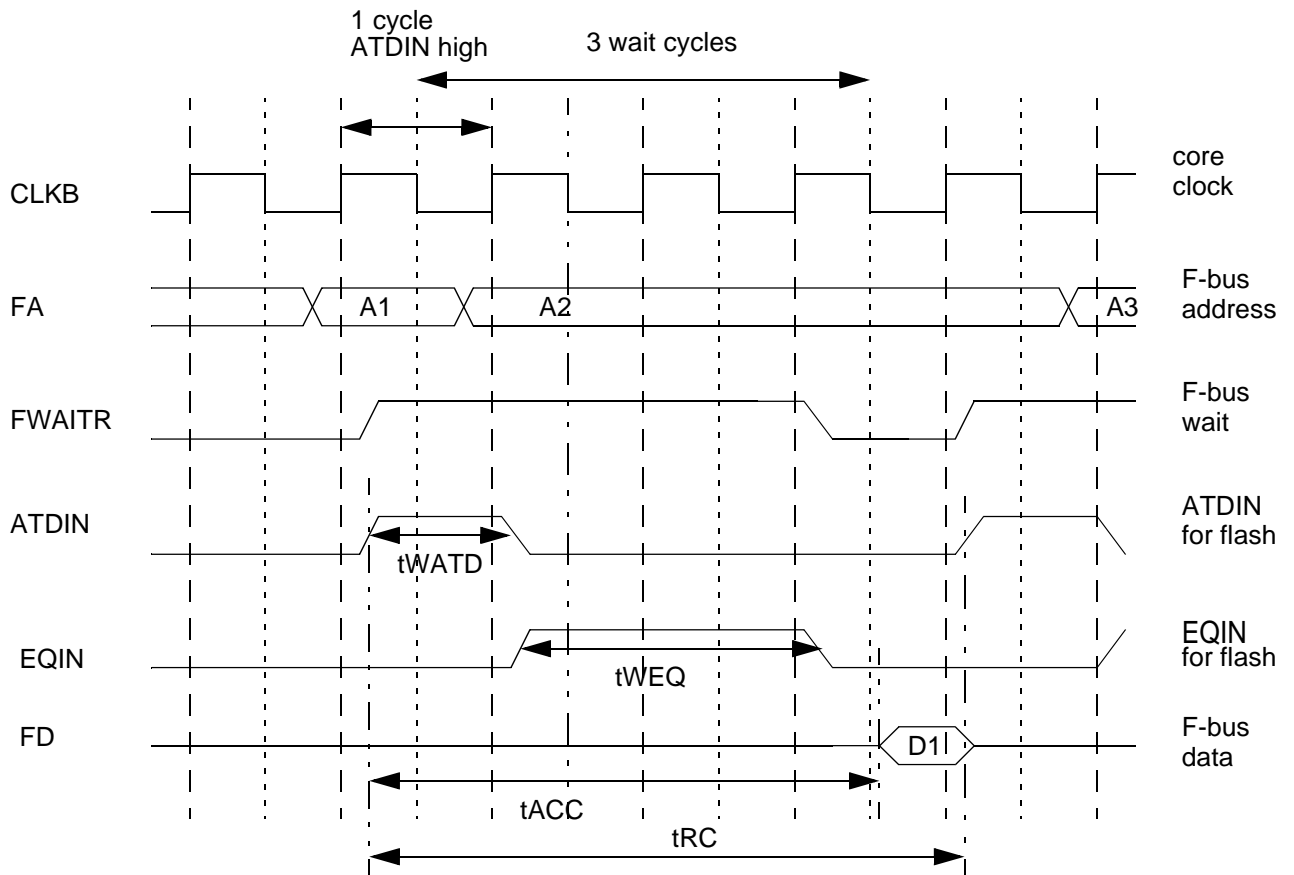
- Without applying clock modulation:

| CLKB unmodulated core clock frequency [MHz] | FAC1 | FAC0 | EQINH | WTC2 | WTC1 | WTC0 | ATDIN high cycles/wait cycles | FMWT |
|---|------|------|-------|------|------|------|-------------------------------|------|
| 32 | 0 | 0 | 1 | 0 | 0 | 1 | 0.5 / 1 | 09H |
| 24 | 0 | 0 | 0 | 0 | 0 | 1 | 0.5 / 1 | 01H |
| 16 | 0 | 0 | 0 | 0 | 0 | 1 | 0.5 / 1 | 01H |

- When applying clock modulation:

| CLKB core clock frequency [MHz] | Peak max. frequency | FAC1 | FAC0 | EQINH | WTC2 | WTC1 | WTC0 | ATDIN high cycles/wait cycles | FMWT |
|---------------------------------|---------------------|------|------|-------|------|------|------|-------------------------------|------|
| 32 | 64 | 0 | 1 | 0 | 0 | 1 | 1 | 1 / 3 | 13H |
| 32 | 48 | 0 | 0 | 0 | 0 | 1 | 0 | 0.5 / 2 | 02H |
| 24 | 40 | 0 | 0 | 0 | 0 | 1 | 0 | 0.5 / 2 | 02H |
| 24 | 32 | 0 | 0 | 1 | 0 | 0 | 1 | 0.5 / 1 | 09H |
| 16 | 24 | 0 | 0 | 0 | 0 | 0 | 1 | 0.5 / 1 | 01H |

Example for flash memory read access with 1 cycle for the high time of ATDIN and 3 wait cycles:



The minimum value for t_{WATD} is 10 ns, the minimum value for t_{WEQ} is 20 ns.

The minimum value for t_{RC} is 40 ns.

The maximum value for t_{ACC} is $t_{WATD} + t_{WEQ} + 5$ ns.

Recommended settings for WTC2 to WTC0 for **write** access to the flash memory, FACCEN of FMCS should be set to 1 for writing, so FAC1, FAC0, EQINH register settings then have no meaning for the write operation

:

- Without applying clock modulation:

| CLKB unmodulated core clock frequency [MHz] | WTC2 | WTC1 | WTC0 | Wait cycles | FMWT |
|---|------|------|------|-------------|------|
| 32 | 0 | 1 | 0 | 2 | X2H |
| 24 | 0 | 1 | 0 | 2 | X2H |
| 16 | 0 | 0 | 1 | 1 | X1H |

- When applying clock modulation:

| CLKB core clock frequency [MHz] | Peak max. frequency | WTC2 | WTC1 | WTC0 | Wait cycles | FMWT |
|---------------------------------|---------------------|---------------------------------|------|------|-------------|------|
| 32 | 64 | setting not allowed for writing | | | | |
| 32 | 48 | 1 | 0 | 0 | 4 | X4H |
| 24 | 40 | 1 | 0 | 0 | 4 | X4H |
| 24 | 32 | 0 | 1 | 0 | 2 | X2H |
| 16 | 24 | 0 | 1 | 0 | 2 | X2H |

2.2 F362 Mode Register (F362MD)

| address | bit 15 | bit14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |
|---------------|--------|-------|--------|--------|--------|--------|-------|--------|
| 00001FEH | ---- | --- | ---- | ---- | ---- | ---- | ---- | IICSEL |
| access | | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| initial value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 15-9: reserved, when writing to bits 15-9, always write "0000000"

Bit 8: IICSEL

0: selection of 100 kHz I2C interface (I2C-1)

1: selection of 400 kHz I2C interface (I2C-2)

2.3 Oscillation stabilization time

For a mode setting of MD[2:0] = "000" the following settings of OS1 and OS0 bits in the standby control register (STCR) will be implemented:

| OS1 | OS0 | Oscillation stabilization wait time | time based on 4 MHz oscillator (ϕ) |
|-----|-----|-------------------------------------|---|
| 0 | 0 | $\phi * 2^{16}$ | 32 ms (initial value) |
| 0 | 1 | $\phi * 2^{11}$ | 1 ms |
| 1 | 0 | $\phi * 2^{16}$ | 32 ms |
| 1 | 1 | $\phi * 2^1$ | 1 μ s |

2.4 Subclock RTC32 (CLKR2)

This register is used to control the RTC32 mode bit for use in subclock system.

| address | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |
|---------------|--------|--------|--------|--------|--------|--------|-------|-------|
| 000046H | ---- | ---- | ---- | ---- | ---- | ---- | ---- | RTC32 |
| access | | | | | | R/W | R/W | R/W |
| initial value | | | | | | 0 | 0 | 0 |

Bit [15:11]: reserved

Bit [10:9]: reserved, always write 0 back when writing to these bits.

Bit 8: RTC32

0: RTC32KHI mode, high power mode of internal voltage regulator used in RTC mode

1: RTC32KLO mode, low power mode of internal voltage regulator used in RTC mode

Always set this bit to 1 when using the RTC mode based on the 32 kHz subclock. This is only available for MB91F368GA.

2.5 Boot ROM

The following settings have been implemented in the BOOT ROM of MB91F367GA/F368GA:

- Flash area: 08:0000 to 0F:FFF7
- Security Vector at 0F:FEF4
- Security vector valid in ranges 08:0000-0F:FFFF
- Program entry at 0F:4000
- ROM stamp at 05:0500
- Flash registers initialized to FMCS=0x60, FMWT=0x13

CHAPTER 3 IO-Map

see appendix A.

The addresses shown in this table for CAN registers are based on the settings for CS7 done in the Boot ROM.

CHAPTER 4 Interrupt Vector Table

see appendix B

CHAPTER 5 Power-on-sequence

All VDD pins should be connected to the same potential. The analogue supply voltage (AVCC) must not be turned on before the digital supply voltage.

Immediately after power on always execute INIT at the INITX pin (input a low level to the INITX pin). Hold this low level at the INITX pin long enough so that after release of the low level at INITX and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. INITX must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

CHAPTER 6 Handling of Unused Input Pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be tied to VDD or VSS through resistors. In this case those resistors should be more than 2 KOhm.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

The resistor of more than 2 KOhm is used to limit currents through the protection diodes. In case of voltages at the unused pin of 0.3 V or more below VSS or 0.3 V or more above VDD currents which could cause latch-up will flow through those diodes. It is possible to use one resistor to connect several pins to VDD or VSS. Care should be taken not to connect pins from different supply voltage domains to one resistor.

CHAPTER 7 Emulation Device

MB91FV360GA can be used as an emulation device for MB91F367GA/F368GA. MB91F367GA/F368GA use the following resources of MB91FV360GA (see MB91FV360GA IO-Map):

- Reload Timer 0 - Reload Timer 2
- UART 0 / U-Timer 0
- SIO 0 - SIO 1 and their Prescalers
- I²C (100KHz and 400KHz)
- A/D Converter (channels 0 - 7)
- Input Capture 0 - Input Capture 3
- Output Compare 0 - Output Compare 1
- Free Running Counter 0 - Free Running Counter 1
- Real Time Clock
- 32 kHz subclock and calibration unit - MB91F368GA only
- Programmable Pulse Generators: PWM Control 0, PWM channels 0 - 3
- Power down reset
- Alarm Comparator
- CAN0 - CAN 1
- User RAM 16KB: address range: 03C000-03FFFF
- F-Bus RAM 16KB: address range: 040000-043FFF
- I-RAM 4KB: address range: 011000-011FFF

Note: Because reload timers 3 to 5 are not available on this device, the ADC cannot be triggered by a reload timer - on MB91FV360GA and other devices reload timer 4 is connected to the ADC

CHAPTER 8 Package

A QFP-120 package called FPT-120P-M21 (0.5 mm pin pitch) will be used for MB91F367GA/F368GA. The thermal resistance of this package is 30 degr. C/W.

| Thermal resistance [degr. C/W] | | | |
|--------------------------------|-------|-------|-----------------------------|
| theta-ja (junction to ambient) | | | theta-jc (junction to case) |
| 0 m/s | 1 m/s | 3 m/s | |
| 30 | 27 | 25 | 5 |

The maximum allowed ambient temperature is 85 degr. C, the maximum allowed junction temperature is 125 degr.C. Under these conditions a maximum power consumption of $(125 \text{ degr. C} - 85 \text{ degr. C}) / 30 \text{ C/W} = 1.33 \text{ W}$ is allowed. The user must make sure that the maximum ambient temperature is not exceeded.

For other details about the package see Fujitsu Semiconductor Package Data Book.

CHAPTER 9 Electrical specification

9.1 Absolute maximum ratings

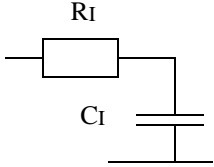
| Parameter | Symbol | min. | max. | Unit | Condition |
|------------------------------------|--------------------|--------|------|------|-------------------------------------|
| Digital supply voltage | VDD-VSS | -0.3 | 6.0 | V | |
| Storage temperature | ϑ_{ST} | -55 | 125 | °C | |
| Power consumption | PTOT | | 1330 | mW | $\vartheta_{ambient} = 25^{\circ}C$ |
| Digital input voltage | VIDIG | -0.3 * | 5.8 | V | VSS=0V, VDD=5V |
| Analog input voltage | VIA | -0.3 | 5.8 | V | VSSA=0V, VDDA=5V |
| Analog supply voltage | VDDA-VSSA | -0.3 | 5.8 | V | VSSA=0V |
| Analog reference voltage | VREFH/L - VSSA | -0.3 | 5.8 | V | VSSA=0V |
| Static DC current into digital I/O | I _{I/ODC} | -2 | 2 | mA | $\sum I_{I/ODC} < I_{Soperation}$ |

* Making full use of the allowed static DC current into digital I/Os will lead to lower values here.

9.2 Operating conditions

| Parameter | Symbol | min. | typ. | max. | Unit | Condition |
|-----------------------------------|---|--------------------|------------|-------------|----------|---|
| Operating temperature | ϑ_{OP} | -40 | | 85 | °C | |
| Supply voltage | | | | | | |
| - Digital supply | VDD-VSS | 4.25 ¹⁾ | 5 | 5.25 | V | Internal voltage reg. VDDCORE=3.3V |
| - Analog supply | VDDA-VSSA | 4.9 | 5 | 5.1 | V | VSSA=0V |
| Current consumption | | | | | | |
| -run mode ³⁾ | I _{srn} | | see | below | mA | |
| -RTC mode | I _{sRTC4} I _{sRTC32} | | 0.5 TBD | 1.25 0.5 | mA mA | f _{clk} =4MHz@ ϑ_{op} =25°C f _{clk} =32KHz@ ϑ_{op} =25°C |
| -stop mode | I _{sstop} | | 10 | 200 | μA | f _{clk} =0 @ ϑ_{op} =25°C |
| RAM data retention voltage | VDD-VSS | 3.0 | | | V | |

| | | | | | | |
|--|----------------------|------------------------------|-----------------------|------------------------------|----|--|
| Alarm comparator - Threshold voltages - overvoltage - undervoltage - Switching hysteresis - Alarm sense time - Input resistance | V _{TAH} | $\frac{4}{5} V_{DDA}$ -5% | $\frac{4}{5} V_{DDA}$ | $\frac{4}{5} V_{DDA}$ +5% | V | (external 4:1 divider) at V _{TAH} , V _{TAL} |
| | V _{TAL} | $\frac{2}{5} V_{DDA}$ -5% | $\frac{2}{5} V_{DDA}$ | $\frac{2}{5} V_{DDA}$ +5% | V | |
| | V _{TAHYS} | 12.5 | 25 | 50 | mV | |
| | t _{AS} | | | 10 | μs | |
| | R _{in} | 5 | | | MΩ | |
| Power down Reset - Threshold voltage - Switching hysteresis - Reset sense time | V _{TPOR} | 3.5 | 4.0 | 4.5 | V | |
| | V _{TPORHYS} | 20 | 50 | 80 | mV | |
| | t _{RS} | | | 10 | μs | |
| Digital Inputs ²⁾ CMOS (Type: Q) - High voltage range - Low voltage range CMOS Schmitt-Trigger (Types: E, U) - High voltage range - Low voltage range CMOS Automotive Schmitt-Trigger (Types: A, B, W, X) - High voltage range - Low voltage range - Hysteresis voltage - Input capacitance - Input leakage current - Pull up resistor | V _{IH} | 0.65*VDD | | VDD | V | V _{min} =4.25V V _{min} =4.75V Types: E, U θ _{op} =25°C |
| | V _{IL} | VSS | | 0.25*VDD | V | |
| | V _{IH} | 0.8*VDD | | VDD | V | |
| | V _{IL} | VSS | | 0.2*VDD | V | |
| | V _{IH} | 0.8*VDD | | VDD | V | |
| | V _{IL} | VSS | | 0.5*VDD | V | |
| | | | 0.5 | 0.6*VDD | V | |
| | C _{IN} | | | 16 | pF | |
| | I _{IL} | -1 | | 1 | μA | |
| | R _{up1} | | 50 | | kΩ | |
| Digital outputs - Output "H" voltage - Output "L" voltage | V _{OH} | VDD-0.5 | | VDD | V | I _{load} = 4mA |
| | V _{OL} | VSS | | VSS+0.4 | V | I _{load} = -4mA |

| | | | | | |
|---|---|--|---|--|--|
| ADC inputs ⁴⁾ - Reference voltage input - Input voltage range - Input resistance - Input capacitance - Impedance of external output driving the ADC input - Input leakage current | VREFH VREFL V _{imax} V _{imin} R _I C _I I _{IL} | VREFL+3 VSSA VREFL -1 | 3.6 30 4.0 1 | V V V V kΩ pF kΩ μA |  @ sampling time of 1.6 μs @op=25°C |
| PPG - Output voltage - Output current | V _{outHIGH} V _{outLOW} I _{out} | VDD-0.5 VSS 4 | VDD VSS+0.4 | V V mA | |
| I²C Bus Interface - Output voltage - Output current - Input threshold voltage | V _{outHIGH} V _{outLOW} I _{out} V _{IH} V _{IL} | VSS 3 0.65*VDD VSS | VDD VSS+0.4 VDD 0.25*VDD | V V mA V V | Open Drain Output I _{outLOW} = 3mA |
| Lock-up time PLL1 (4MHz->16...64MHz) | | | 1 | ms | |
| ESD Protection (Human body model MIL883-B compliant) | V _{surge} | 2 | | kV | R _{discharge} =1.5kΩ C _{discharge} = 100pF |

¹⁾ this is only valid if the integrated power-down reset circuit is switched-off, else a reset can be triggered at voltages less or equal than 4.5 V (see spec items for power-down reset)

²⁾ valid for bidirectional tristate I/O PAD cell

³⁾ I_{ISRUN} describes the current consumption of the MCU core only and has been determined by setting the clock frequencies shown below and running an endless loop from internal flash memory which generates activity on all internal buses. A procedure to calculate the overall power consumption is also shown below.

⁴⁾ The protection diodes at the analog inputs are connected to the digital supply voltage

9.3 Run Mode Current/Power consumption

The power dissipation during normal operation is determined by the total power dissipation of the internal logic P_C , the dissipation from analog modules P_A and the power dissipation P_{IO} of the I/O buffers. Among the I/O buffers the dissipation caused by the stepper motor drivers P_{SMC} should be taken into special consideration.

So the overall power consumption P_D will be calculated as a sum of $P_C + P_A + P_{IO}$.

9.3.1 Logic Power Consumption

The following formula can be used to calculate the maximum core current consumption when the PLL is used depending on the frequency settings for the internal clocks:

$$I_{CC} = 3.45[\text{mA/MHz}] * CLKB[\text{MHz}] + 2.52[\text{mA/MHz}] * CLKP[\text{MHz}] + 0.72[\text{mA/MHz}] * CLKT[\text{MHz}] + 35.5 \text{ mA.}$$

If clock modulation is used the following value must be added to this result: $0.24[\text{mA/MHz}] * CLKB[\text{MHz}]$.

This results in the following values:

| Clock frequencies [MHz] | | | Maximum Core Current Consumption [mA] | Logic Power Consumption P_C at 5.25 V [mW] | Remarks |
|-------------------------|-------|-------|---------------------------------------|--|-----------------------------|
| CLKB | CLKP | CLKT | | | |
| 32 | 16 | 16 | 205 | 1.08 | |
| 24 | 24 | 24 | 202 | 1.06 | |
| 24 | 12 | 12 | 163 | 0.86 | |
| 16 | 16 | 16 | 146 | 0.77 | |
| 2 | 2 | 2 | 40 | 0.21 | no PLL, no clock modulation |
| 0.125 | 0.125 | 0.125 | 30 | 0.16 | no PLL, no clock modulation |

Note: Higher frequency settings cannot be allowed in the package currently used. For higher frequency settings the maximum power consumption would exceed the maximum allowed value of 1.33W.

In addition to this power consumption of the MCU core logic the following contributions to the overall power consumption have to be considered:

9.3.2 Analog Power Consumption

| Module | Maximum Current Consumption | Remarks |
|------------------|-----------------------------|---------|
| DAC | 1 mA / channel | |
| ADC | 7 mA | |
| Power down reset | 0.5 mA | |
| Alarm Comparator | 0.5 mA | |

To calculate the analog power consumption P_A , the current contributions of the active modules have to be multiplied by the maximum analog supply voltage of 5.1 V.

9.3.3 I/O Power Consumption

I/O Buffers:

The power dissipation (P_{IO}) (at 5.25 V) of the I/O buffers is represented as the sum of the dynamic power dissipation (P_{AC}) and the static power consumption (P_{DC}).

$$P_{IO} = P_{AC} * 1.1 + P_{DC}$$

The following table lists values for P_{AC} :

| Buffer Type | Power Consumption | Unit |
|---------------------------|-------------------|------------------------------------|
| Normal Input | 12.4 | $\mu\text{W}/\text{MHz}$ @ 5.0V |
| Bidirectional Input | | |
| 4 mA Bidirectional Output | 194 + 25 CL | |
| 4 mA Output | | |
| 8 mA Bidirectional Output | 353 + 25 CL | |
| 8 mA Output | | |

$$P_{AC} = P_{IB} * I_n * f * \text{operating rate} + P_{OB} * O_n * f * \text{operating rate}$$

- PIB:** Power Consumption of Input Buffers and Bidirectional Inputs
POB: Power Consumption of Output Buffers and Bidirectional Outputs
In: Total number of input buffers and bidirectional buffer inputs
On: Total number of output buffers and bidirectional buffer outputs
f: System frequency
Operating rate: 1.0 if all buffers are switched simultaneously at system frequency

P_{DC} is the caused by off chip loads which are drawing static currents.

$$P_{DC} = V_O * I_O * DCN$$

VO: Output voltage drop - usually 0.4 V
IO: Output current - usually 4 mA
DCN: Number of output buffers and bidirectional buffers driving off chip loads causing static currents.

9.4 Converter Characteristics

- A/D Converter

| Parameter | Symbol | Rating | | | Unit | Remark |
|----------------------------|------------------|-----------|----------|----------|------|---------------|
| | | Minimum | Typical | Maximum | | |
| Resolution | | | | 10 | Bit | |
| Conversion error | | | | +/- 5.0 | LSB | overall error |
| Non-linearity | | | | +/-2.5 | LSB | |
| Differential Non-linearity | | | | +/-1.9 | LSB | |
| Zero Reading voltage | V _{0T} | AVRL -3.5 | AVRL+0.5 | AVRL+4.5 | LSB | |
| Full scale reading voltage | V _{FST} | AVRH-5.5 | AVRH-1.5 | AVRH+2.5 | LSB | |
| Input current (VDDA) | I _A | | 3.0 | 7.0 | mA | |
| Reference voltage current | I _R | | 1.6 | 2.6 | mA | |

9.5 Clock settings

| Clock domain | Clock name | Max. frequency | Remark |
|---------------|------------|----------------|--|
| Core | CLKB | 64 MHz | for supply voltage between 4.25 and 5.25 V |
| | | 32 MHz | for supply voltage between 4.25 and 3.5 V |
| Resource bus | CLKP | 32 MHz | |
| Ext. Bus | CLKT | 32 MHz | |
| Clock for CAN | CANCLK | 32 MHz | |

Note: Because of the maximum allowed current consumption setting all clocks to their maximum values is not possible in the current package. See calculation of power consumption above. However, clock modulation up to the frequencies specified above is still possible. In the case of modulation over 58 MHz no odd division factor (3,5,7,9,11,13) for CLKT must be selected.

9.6 Clock modulator settings

The clock modulator is a module to reduce EME (Electromagnetic Emission) problems by spreading the energy of the system over a wide range of the frequency spectrum. In order to allow optimization of system performance versus EME reduction, the modulator is programmable over a wide modulation range.

| Clock Modulator | Input Frequency [MHz] | Number of operational settings for Clock Modulator |
|------------------------|------------------------------|---|
| ON | 32 | 8 |
| ON | 24 | 11 |
| ON | 16 | 14 |

Detailed information about Clock Modulator operation and settings is available from Fujitsu on request.

Appendix A I/O Map

Version 1.3, 2000/02/28

Table A lists the addresses for the registers used by the internal peripheral functions of the MB91F367GA/F368GA.

- How to Read the I/O Map

| Address | Register | | | | Internal peripheral |
|---------|------------------------|------------------------|------------------------|----|---------------------|
| | +0 | +1 | +2 | +3 | |
| 000014H | PDRG [R/W] XXXXXXXX | PDRH [R/W] XXXXXXXX | PDRI [R/W] ----XXXX | — | Port data register |

Read/write attribute

Register initial value after a reset (bit initial values)

“1”: initial value “1”, “0”: initial value “0”,

“x”: initial value “X” (indeterminate),

“—” indicates non-existent bits

Register name (The register in column 1 is at location 4n, the register in column 2 at 4n+1, and so on.)

Location of far left of register (+0). +1, +2, and +3 each increment the location by one. When performing word access, the register in column 1 is placed at the MSB end of the data.

Precautions:

- Do not use RMW instructions on registers containing write-only (W) bits.

RMW instructions(RMW:read-modify-write)

AND Rj, @Ri OR Rj, @Ri EOR Rj, @Ri

ANDH Rj, @Ri ORH Rj, @Ri EORH Rj, @Ri

ANDB Rj, @Ri ORB Rj, @Ri EORB Rj, @Ri

BANDL #u4, @Ri BORL #u4, @Ri BEORL #u4, @Ri

BANDH #u4, @Ri BORH #u4, @Ri BEORH #u4, @Ri

- The data in reserved areas and areas marked “—” is indeterminate. Do not use those areas!

| Address | Register | | | | Block |
|---------|----------|----|----|----|---------------------------------|
| | +0 | +1 | +2 | +3 | |
| 000000H | Reserved | | | | T-unit Port Data Register |
| 000004H | Reserved | | | | |
| 000008H | Reserved | | | | |
| 00000CH | Reserved | | | | |

| Address | Register | | | | Block |
|-------------------------|---|--------------------------|--------------------------------------|------------------------------|--------------------------------|
| | +0 | +1 | +2 | +3 | |
| 000010H | PDRG [R/W] XXXXXXXX | PDRH [R/W] XXXXXXXX | PDRJ [R/W] X --- X --- | PDRJ [R/W] XXXXXXXX | R-bus Port Data Register |
| 000014H | PDRK [R/W] XXXXXXXX | PDRL [R/W] XXXXXXXX | PDRM [R/W] ---- XXXX | PDRN [R/W] -- XXXXXX | |
| 000018H | PDRO [R/W] XXXXXXXX | PDRP [R/W] -- XXXXXX | PDRQ [R/W] -- XXXXXX | PDRR [R/W] XXXXXXXX | |
| 00001CH | PDRS [R/W] XXXXXXXX | | | | |
| 000020H 00003CH | | | | | Reserved |
| 000040H | EIRR [R/W] 00000000 | ENIR [R/W] 00000000 | ELVR [R/W] 00000000 00000000 | | Ext int/NMI |
| 000044H | DICR [R/W] ----- 0 | HRCL [R/W] 0 -- 11111 | CLKR2 [R/W] ----- 000 | reserved | DLYI/I-unit RTC |
| 000048H | TMRLR0 [W] XXXXXXXXXX XXXXXXXXX | | TMR0 [R] XXXXXXXXXX XXXXXXXXX | | Reload Timer 0 |
| 00004CH | _____ | | TMCSR0 [R/W] ---- 0000 ---- 00000 | | |
| 000050H | TMRLR1 [W] XXXXXXXXXX XXXXXXXXX | | TMR1 [R] XXXXXXXXXX XXXXXXXXX | | Reload Timer 1 |
| 000054H | _____ | | TMCSR1 [R/W] ---- 0000 ---- 00000 | | |
| 000058H | TMRLR2 [W] XXXXXXXXXX XXXXXXXXX | | TMR2 [R] XXXXXXXXXX XXXXXXXXX | | Reload Timer 2 |
| 00005CH | _____ | | TMCSR2 [R/W] ---- 0000 ---- 00000 | | |
| 000060H | SSR0 [R/W] 00001 - 00 | SIDR0 [R/W] XXXXXXXX | SCR0 [R/W] 00000100 | SMR0 [R/W] 00 -- 0 - 0 - | UART0 |
| 000064H | ULS0 [R/W] ---- 0000 | | | | |
| 000068H | UTIM0/UTIMR0 [R/W] 00000000 00000000 | | DRCL0 [W] ----- | UTIMC0 [R/W] 0 --- 0 - 01 | U-TIMER 0 |
| 00006CH | _____ | | | | Reserved |
| 000070H | | | | | |
| 000074H | | | | | |
| 000078H | | | | | |
| 00007CH | | | | | |
| 000080H | | | | | |

| Address | Register | | | | Block |
|---------|---------------------------------------|--------------------------|-------------------------------------|----------------------------|--|
| | +0 | +1 | +2 | +3 | |
| 000084H | SMCS0 [R/W] 00000010 ---- 00-0 | | SES0 [R/W] ----- 00 | SDR0 [R/W] 00000000 | SIO 0 |
| 000088H | SMCS1 [R/W] 00000010 ---- 00-0 | | SES1 [R/W] ----- 00 | SDR1 [R/W] 00000000 | |
| 00008CH | CDCR0 [R/W] 0 --- 1111 | Reserved | CDCR1 [R/W] 0 --- 1111 | Reserved | SIO 0/1 Prescaler |
| 000090H | | | | | Reserved |
| 000094H | IBCR [R/W] 00000000 | IBSR [R] 00000000 | IADR [R/W] -XXXXXXXX | ICCR [R/W] -- 0XXXXX | I2C (old) |
| 000098H | | IDAR [R/W] XXXXXXXXXX | | IDBL [R/W] -----0 | -> new I2C from address 0x184 |
| 00009CH | ADMD [R/W,W] --- X0000 | ADCH [R/W] 00000000 | | ADCS [R/W,W] 0000 -- 00 | A/D Converter |
| 0000A0H | ADCD [R/W] 000000XX XXXXXXXXX | | | ADBL [R/W] ----- 0 | |
| 0000A4H | _____ | | | | Reserved |
| 0000A8H | _____ | | | | |
| 0000ACH | IOTDBL0 [R/W] ----- 000 | ICS01 [R/W] 00000000 | IOTDBL1 [R/W] ----- 000 | ICS23 [R/W] 00000000 | Input Capture 0,1,2,3 |
| 0000B0H | IPCP0 [R] XXXXXXXXXX XXXXXXXXX | | IPCP1 [R] XXXXXXXXXX XXXXXXXXX | | |
| 0000B4H | IPCP2 [R] XXXXXXXXXX XXXXXXXXX | | IPCP3 [R] XXXXXXXXXX XXXXXXXXX | | |
| 0000B8H | OCS01 [R/W] --- 0 -- 00 0000 -- 00 | | reserved | | Output Com- pare 0,1 |
| 0000BCH | OCCP0 [R/W] XXXXXXXXXX XXXXXXXXX | | OCCP1 [R/W] XXXXXXXXXX XXXXXXXXX | | |
| 0000C0H | _____ | | | | Reserved |
| 0000C4H | _____ | | | | |
| 0000C8H | TCDT0 [R/W] XXXXXXXXXX XXXXXXXXX | | _____ | TCCS0 [R/W] - 0000000 | Free Running Counter 0 for ICU/OCU |
| 0000CCH | TCDT1 [R/W] XXXXXXXXXX XXXXXXXXX | | _____ | TCCS1 [R/W] - 0000000 | Free Running Counter 1 for ICU/OCU |
| 0000D0H | | | | | |

| Address | Register | | | | Block |
|---------|----------------------------------|--|-----------------------------------|---------------------------|------------------------------------|
| | +0 | +1 | +2 | +3 | |
| 0000D4H | _____ | | | | Reserved |
| 0000D8H | | | | | |
| 0000DCH | | | | | |
| 0000E0H | | | | | |
| 0000E4H | | | | | |
| 0000E8H | | | | | |
| 0000ECH | | | | | |
| 0000F0H | | | | | |
| 0000F4H | | WTDBL [R/W] ----- 0 | WTCR [R/W] 00000000 000 - 0000 | | Real Time Clock (WatchTimer) |
| 0000F8H | | WTBR [R/W] -- XXXXXXX XXXXXXXX XXXXXXXX | | | |
| 0000FCH | WTHR [R/W] --- 00000 | WTMR [R/W] -- 000000 | WTSR [R/W] -- 000000 | | |
| 000100H | _____ | | | | Reserved |
| 000104H | | | | | |
| 000108H | | | | | |
| 00010CH | | | | | |
| 000110H | | | | | |
| 000114H | | | | | |
| 000118H | GCN10 [R/W] 00110010 00010000 | | PDBL0 [R/W] --- 00000 | GCN20 [R/W] ---- 0000 | PWM Control 0 |
| 00011CH | _____ | | | | Reserved |
| 000120H | PTMR0 [R] 11111111 11111111 | | PCSR0 [W] XXXXXXXX XXXXXXXX | | PWM0 |
| 000124H | PDUT0 [W] XXXXXXXX XXXXXXXX | | PCNH0 [R/W] 0000000 - | PCNL0 [R/W] 000000 - 0 | |
| 000128H | PTMR1 [R] 11111111 11111111 | | PCSR1 [W] XXXXXXXX XXXXXXXX | | PWM1 |
| 00012CH | PDUT1 [W] XXXXXXXX XXXXXXXX | | PCNH1 [R/W] 0000000 - | PCNL1 [R/W] 000000 - 0 | |
| 000130H | PTMR2 [R] 11111111 11111111 | | PCSR2 [W] XXXXXXXX XXXXXXXX | | PWM2 |
| 000134H | PDUT2 [W] XXXXXXXX XXXXXXXX | | PCNH2 [R/W] 0000000 - | PCNL2 [R/W] 000000 - 0 | |

| Address | Register | | | | Block |
|---------|---------------------------------|---------------------------|----------------------------------|---------------------------|---|
| | +0 | +1 | +2 | +3 | |
| 000138H | PTMR3 [R] 11111111 11111111 | | PCSR3 [W] XXXXXXXX XXXXXXXX | | PWM3 |
| 00013CH | PDUT3 [W] XXXXXXXX XXXXXXXX | | PCNH3 [R/W] 0000000 - | PCNL3 [R/W] 000000 - 0 | |
| 000140H | | | | | Reserved |
| 000144H | | | | | |
| 000148H | | | | | |
| 00014CH | | | | | |
| 000150H | | | | | |
| 000154H | | | | | |
| 000158H | | | | | |
| 00015CH | | | | | |
| 000160H | | | | | |
| 000164H | | | | | |
| 000168H | CMLS0 [R/W] 01110111 1111111 | | CMLS1 [R/W] 01110111 1111111 | | |
| 00016CH | CMLS2 [R/W] 01110111 1111111 | | CMLS3 [R/W] 01110111 1111111 | | |
| 000170H | CMLT0 [R/W] ----100 00000010 | | CMLT1 [R/W] 11110100 00000010 | | |
| 000174H | CMLT2 [R/W] ----100 00000010 | | CMLT3 [R/W] ----100 00000010 | | |
| 000178H | CMAC [R/W] 11111111 1111111 | | CMTS [R/W] --000001 01111111 | | |
| 00017CH | | PDCRCR [R/W] ----- 000 | | | Power down reset |
| 000180H | ACCDBL[R/W] ----- 0 | ACSR [R/W] --- XXX00 | | | Alarm comparator |
| 000184H | IBCR2 [R/W] 00000000 | IBSR2 [R] 00000000 | ITBAH [R/W] ----- 00 | ITBAL [R/W] 00000000 | I2C (new) |
| 000188H | ITMKH [R/W] 00 ---- 11 | ITMKL [R/W] 11111111 | ISMK [R/W] 01111111 | ISBA [R/W] - 0000000 | (*) old and new I2C share this bit! |
| 00018CH | IDARH [-] 00000000 | IDAR2 [R/W] 00000000 | ICCR2 [R/W] - 0011111 | IDBL2(*) [R/W] ----- 0 | |
| 000190H | CUCR [R/W] ----- --- 0 --00 | | CUTD [R/W] 10000000 00000000 | | calibration unit of 32KHz oscillator (only on F368GA) |
| 000194H | CUTR1 [R] ----- 00000000 | | CUTR2 [R] 00000000 00000000 | | |

| Address | Register | | | | Block |
|-------------------------|---|----|--------------------------|----|----------------------|
| | +0 | +1 | +2 | +3 | |
| 000198H 0001F8H | -----1 | | | | Reserved |
| 0001FCH | | | F362MD [R/W] 00000000 | | F362 Mode Reg |
| 000200H | DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | DMAC |
| 000204H | DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| 000208H | DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| 00020CH | DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| 000210H | DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| 000214H | DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| 000218H | DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| 00021CH | DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| 000220H | DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX | | | | |
| 000224H | DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX | | | | |
| 000228H 00023CH | ----- | | | | |
| 000240H | DMACR [R/W] 00--0000 ----- | | | | |
| 000244H 0003ECH | ----- | | | | Reserved |
| 0003F0H | BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Bit Search Module |
| 0003F4H | BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0003F8H | BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0003FCH | BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |

| Address | Register | | | | Block |
|-------------------------|------------------------|------------------------|------------------------|------------------------|-------------------------------------|
| | +0 | +1 | +2 | +3 | |
| 000400H | DDRG [R/W] 00000000 | DDRH [R/W] 00000000 | DDRI [R/W] ---0--- | DDRJ [R/W] 00000000 | R-bus Port Direction Register |
| 000404H | DDRK [R/W] 00000000 | DDRL [R/W] 00000000 | DDRM [R/W] ----0000 | DDRN [R/W] --000000 | |
| 000408H | DDRO [R/W] 00000000 | DDRP [R/W] ----0000 | DDRQ [R/W] --000000 | DDRR [R/W] 00000000 | |
| 00040CH | DDRS [R/W] 00000000 | | | | |
| 000410H | PFRG [R/W] 00000000 | PFRH [R/W] 00000000 | PFRI [R/W] ---0--- | PFRJ [R/W] 00000000 | R-bus Port Function Register |
| 000414H | PFRK [R/W] 00000000 | PFRL [R/W] 00000000 | PFRM [R/W] ----0000 | PFRN [R/W] --000000 | |
| 000418H | PFRO [R/W] 00000000 | PFRP [R/W] 00000000 | PFRQ [R/W] --000000 | PFRR [R/W] 00000000 | |
| 00041CH | PFRS [R/W] 00000000 | | | | |
| 000420H 00043CH | ————— | | | | Reserved |

| Address | Register | | | | Block |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------------------------|
| | +0 | +1 | +2 | +3 | |
| 000440H | ICR00 [R/W] ---11111 | ICR01 [R/W] ---11111 | ICR02 [R/W] ---11111 | ICR03 [R/W] ---11111 | Interrupt Control unit |
| 000444H | ICR04 [R/W] ---11111 | ICR05 [R/W] ---11111 | ICR06 [R/W] ---11111 | ICR07 [R/W] ---11111 | |
| 000448H | ICR08 [R/W] ---11111 | ICR09 [R/W] ---11111 | ICR10 [R/W] ---11111 | ICR11 [R/W] ---11111 | |
| 00044CH | ICR12 [R/W] ---11111 | ICR13 [R/W] ---11111 | ICR14 [R/W] ---11111 | ICR15 [R/W] ---11111 | |
| 000450H | ICR16 [R/W] ---11111 | ICR17 [R/W] ---11111 | ICR18 [R/W] ---11111 | ICR19 [R/W] ---11111 | |
| 000454H | ICR20 [R/W] ---11111 | ICR21 [R/W] ---11111 | ICR22 [R/W] ---11111 | ICR23 [R/W] ---11111 | |
| 000458H | ICR24 [R/W] ---11111 | ICR25 [R/W] ---11111 | ICR26 [R/W] ---11111 | ICR27 [R/W] ---11111 | |
| 00045CH | ICR28 [R/W] ---11111 | ICR29 [R/W] ---11111 | ICR30 [R/W] ---11111 | ICR31 [R/W] ---11111 | |
| 000460H | ICR32 [R/W] ---11111 | ICR33 [R/W] ---11111 | ICR34 [R/W] ---11111 | ICR35 [R/W] ---11111 | |
| 000464H | ICR36 [R/W] ---11111 | ICR37 [R/W] ---11111 | ICR38 [R/W] ---11111 | ICR39 [R/W] ---11111 | |
| 000468H | ICR40 [R/W] ---11111 | ICR41 [R/W] ---11111 | ICR42 [R/W] ---11111 | ICR43 [R/W] ---11111 | |
| 00046CH | ICR44 [R/W] ---11111 | ICR45 [R/W] ---11111 | ICR46 [R/W] ---11111 | ICR47 [R/W] ---11111 | |
| 000470H 00047CH | _____ | | | | |
| 000480H | RSRR [R/W] 10000000 | STCR [R/W] 00110011 | TBCR [R/W] X0000X00 | CTBR [W] XXXXXXXX | Clock Control unit |
| 000484H | CLKR [R/W] 00000000 | WPR [W] XXXXXXXX | DIVR0 [R/W] 00000011 | DIVR1 [R/W] 00000000 | |
| 000488H 0005FCH | _____ | | | | Reserved |
| 000600H | _____ | | | | Reserved |
| 000604H | | | | | |
| 000608H | | | | | |
| 00060CH | | | | | |

| Address | Register | | | | Block | |
|-------------------------|-------------------------------|-------------------------|-------------------------------|-------------------------|----------|---------------|
| | +0 | +1 | +2 | +3 | | |
| 000610H | _____ | | | | Reserved | |
| 000614H | | | | | | |
| 000618H | | | | | | |
| 00061CH | | | | | | |
| 000620H | | | | | | |
| 000624H | | | | | | |
| 000628H 00063FH | _____ | | | | Reserved | |
| 000640H | ASR0 [W] 00000000 00000000 | | AMR0 [W] 11111000 11111111 | | T-unit | |
| 000644H | ASR1 [W] 00000000 00000000 | | AMR1 [W] 00000000 00000000 | | | |
| 000648H | ASR2 [W] 00000000 00000000 | | AMR2 [W] 00000000 00000000 | | | |
| 00064CH | ASR3 [W] 00000000 00000000 | | AMR3 [W] 00000000 00000000 | | | |
| 000650H | ASR4 [W] 00000000 00000000 | | AMR4 [W] 00000000 00000000 | | | |
| 000654H | ASR5 [W] 00000000 00000000 | | AMR5 [W] 00000000 00000000 | | | |
| 000658H | ASR6 [W] 00000000 00000000 | | AMR6 [W] 00000000 00000000 | | | |
| 00065CH | ASR7 [W] 00000000 00000000 | | AMR7 [W] 00000000 00000000 | | | |
| 000660H | AMD0 [R/W] -00XX111 | AMD1 [R/W] -XXXXXXXX | AMD2 [R/W] --XXXXXX | AMD3 [R/W] --XXXXXX | | |
| 000664H | AMD4 [R/W] --XXXXXX | AMD5 [R/W] --XXXXXX | AMD6 [R/W] -XXXXXXXX | AMD7 [R/W] -XXXXXXXX | | |
| 000668H | CSE 11000011 | _____ | _____ | _____ | | |
| 00066CH | _____ | _____ | _____ | _____ | | |
| 000670H | CHE 11111111 | _____ | _____ | _____ | | |
| 000674H 0007F8H | _____ | | | | | Reserved |
| 0007FCH | _____ | MODR [W] XXXXXXXX | _____ | _____ | | Mode Register |

| Address | Register | | | | Block |
|-------------------------|---|-------|-------|-------|--|
| | +0 | +1 | +2 | +3 | |
| 000800H 000B6CH | _____ | | | | Reserved |
| 001000H | DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | DMAC |
| 001004H | DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 001008H | DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 00100CH | DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 001010H | DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 001014H | DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 001018H | DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 00101CH | DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 001020H | DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 001024H | DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 001028H 003FFCH | _____ | | | | Reserved |
| 004000H 006FFFH | _____ | | | | Reserved |
| 007000H | FMCS [R/W] 1110X000 | _____ | _____ | _____ | Flash Memory Control Register |
| 007004H | FMWT [R/W] --000011 | _____ | _____ | _____ | |
| 007008H 00FFFC | _____ | | | | Reserved |
| 010000H 010FFCH | _____ | | | | Reserved |
| 011000H 011FFCH | _____ | | | | I-RAM 4 kB |

| Address | Register | | | | Block |
|-------------------------|-------------------|----|--------------------|----|---------------------------------------|
| | +0 | +1 | +2 | +3 | |
| 012000H 01FFFCH | _____ | | | | Reserved |
| 020000H 03BFFCH | _____ | | | | Reserved |
| 03C000H 03FFFCH | | | | | User RAM 16 kB (D-Bus) |
| 040000H 043FFCH | | | | | Fast RAM 16 kB (F-Bus) |
| 044000H 0FEFFC | _____ | | | | Reserved |
| 050000H 0507FCH | | | | | Boot ROM 2 kB (F-Bus) |
| 050800H 07FFF4H | _____ | | | | reserved |
| 080000H 09FFFCH | Sector 0 64 KB | | Sector 7 64 KB | | Flash Memory 512 K on F-Bus |
| 0A0000H 0BFFFC | Sector 1 64 KB | | Sector 8 64 KB | | |
| 0C0000H 0DFFFC | Sector 2 64 KB | | Sector 9 64 KB | | |
| 0E0000H 0EFFFFC | Sector 3 32 KB | | Sector 10 32 KB | | |
| 0F0000H 0F3FFCH | Sector 4 8 KB | | Sector 11 8 KB | | |
| 0F4000H 0F7FFCH | Sector 5 8 KB | | Sector 12 8 KB | | |
| 0F8000H 0FFFF4H | Sector 6 16 KB | | Sector 13 16 KB | | |

| Address | Register | | | | Block |
|--|-------------------------|----|----|----|-------------------------------|
| | +0 | +1 | +2 | +3 | |
| 0FFFF8H | FMV [R] 06 00 00 00H | | | | Fixed Reset/Mode Vector |
| 0FFFFCH | FRV [R] 00 05 00 00H | | | | |
| Write operations to address 0FFFF8H and 0FFFFCH are not possible. When reading these addresses, the values shown above will be read. | | | | | |

| Address | Register | | | | Block |
|-----------------------|--|----|-----------------------------------|-------------------------|---|
| | +0 | +1 | +2 | +3 | |
| 10000H | BVALR0 [R/W] 00000000 00000000 | | TREQR0 [R/W] 00000000 00000000 | | CAN 0 Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Men- tioned addresses are default val- ues, deter- mined by boot ROM con- tents. |
| 10004H | TCANR0 [W] 00000000 00000000 | | TCR0 [R/W] 00000000 00000000 | | |
| 10008H | RCR0 [R/W] 00000000 00000000 | | RRTRR0 [R/W] 00000000 00000000 | | |
| 1000CH | ROVRR0 [R/W] 00000000 00000000 | | RIER0 [R/W] 00000000 00000000 | | |
| 10010H | CSR0 [R/W] 00000000 00000001 | | | LEIR0 [R/W] 000-0000 | |
| 10014H | RTEC0 [R] 00000000 00000000 | | BTR0 [R/W] -1111111 11111111 | | |
| 10018H | IDER0 [R/W] XXXXXXXX XXXXXXXX | | TRTRR0 [R/W] 00000000 00000000 | | |
| 1001CH | RFWTR0 [R/W] XXXXXXXX XXXXXXXX | | TIER0 [R/W] 00000000 00000000 | | |
| 10020H | AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 10024H | AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 10028H | AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 1002CH 10048H | GENERAL PURPOSE RAM [R/W] | | | | |
| 1004CH | IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 10050H | IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 10054H | IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 10058H | IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 1005CH | IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 10060H | IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 10064H | IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |

| Address | Register | | | | Block |
|---------|---|----|---------------------------|----|-------|
| | +0 | +1 | +2 | +3 | |
| 100068H | IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | CAN 0 |
| 10006CH | IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100070H | IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100074H | IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100078H | IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 10007CH | IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100080H | IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100084H | IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100088H | IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 10008CH | DLCR00 [R/W] -----XXX | | DLCR10 [R/W] -----XXX | | |
| 100090H | DLCR20 [R/W] -----XXX | | DLCR30 [R/W] -----XXX | | |
| 100094H | DLCR40 [R/W] -----XXX | | DLCR50 [R/W] -----XXX | | |
| 100098H | DLCR60 [R/W] -----XXX | | DLCR70 [R/W] -----XXX | | |
| 10009CH | DLCR80 [R/W] -----XXX | | DLCR90 [R/W] -----XXX | | |
| 1000A0H | DLCR100 [R/W] -----XXX | | DLCR110 [R/W] -----XXX | | |
| 1000A4H | DLCR120 [R/W] -----XXX | | DLCR130 [R/W] -----XXX | | |
| 1000A8H | DLCR140 [R/W] -----XXX | | DLCR150 [R/W] -----XXX | | |
| 1000ACH | DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000B4H | DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |

| Address | Register | | | | Block |
|---------|--|----|----|----|-------|
| | +0 | +1 | +2 | +3 | |
| 1000BCH | DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | CAN 0 |
| 1000C4H | DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000CCH | DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000D4H | DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000DCH | DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000E4H | DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000ECH | DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000F4H | DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1000FCH | DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 100104H | DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 10010CH | DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 100114H | DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 10011CH | DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 100124H | DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 10012CH | CREG0 [R/W] 00000000 00000110 | | | | |

| Address | Register | | | | Block |
|-------------------------|---|----|-----------------------------------|-------------------------|---|
| | +0 | +1 | +2 | +3 | |
| 100200H | BVALR1 [R/W] 00000000 00000000 | | TREQR1 [R/W] 00000000 00000000 | | CAN 1 Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Men- tioned addresses are default val- ues, deter- mined by boot ROM con- tents. |
| 100204H | TCANR1 [W] 00000000 00000000 | | TCR1 [R/W] 00000000 00000000 | | |
| 100208H | RCR1 [R/W] 00000000 00000000 | | RRTRR1 [R/W] 00000000 00000000 | | |
| 10020CH | ROVRR1 [R/W] 00000000 00000000 | | RIER1 [R/W] 00000000 00000000 | | |
| 100210H | CSR1 [R/W] 00000000 00000001 | | | LEIR1 [R/W] 000-0000 | |
| 100214H | RTEC1 [R] 00000000 00000000 | | BTR1 [R/W] -1111111 11111111 | | |
| 100218H | IDER1 [R/W] XXXXXXXX XXXXXXXX | | TRTRR1 [R/W] 00000000 00000000 | | |
| 10021CH | RFWTR1 [R/W] XXXXXXXX XXXXXXXX | | TIER1 [R/W] 00000000 00000000 | | |
| 100220H | AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 100224H | AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 100228H | AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 10022CH 100248H | GENERAL PURPOSE RAM [R/W] | | | | |
| 10024CH | IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 100250H | IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 100254H | IDR21[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 100258H | IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX- | | | | |
| 10025CH | IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 100260H | IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |
| 100264H | IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX | | | | |

| Address | Register | | | | Block |
|---------|---|----|---------------------------|----|-------|
| | +0 | +1 | +2 | +3 | |
| 100268H | IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | CAN 1 |
| 10026CH | IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100270H | IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100274H | IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100278H | IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 10027CH | IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX-- | | | | |
| 100280H | IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100284H | IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 100288H | IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX-- XXXXXXXX | | | | |
| 10028CH | DLCR01 [R/W] -----XXX | | DLCR11 [R/W] -----XXX | | |
| 100290H | DLCR21 [R/W] -----XXX | | DLCR31 [R/W] -----XXX | | |
| 100294H | DLCR41 [R/W] -----XXX | | DLCR51 [R/W] -----XXX | | |
| 100298H | DLCR61 [R/W] -----XXX | | DLCR71 [R/W] -----XXX | | |
| 10029CH | DLCR81 [R/W] -----XXX | | DLCR91 [R/W] -----XXX | | |
| 1002A0H | DLCR101 [R/W] -----XXX | | DLCR111 [R/W] -----XXX | | |
| 1002A4H | DLCR121 [R/W] -----XXX | | DLCR131 [R/W] -----XXX | | |
| 1002A8H | DLCR141 [R/W] -----XXX | | DLCR151 [R/W] -----XXX | | |
| 1002ACH | DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002B4H | DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |

| Address | Register | | | | Block |
|---------|--|----|----|----|-------|
| | +0 | +1 | +2 | +3 | |
| 1002BCH | DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | CAN 1 |
| 1002C4H | DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002CCH | DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002D4H | DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002DCH | DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002E4H | DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002ECH | DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002F4H | DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 1002FCH | DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 100304H | DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 10030CH | DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 100314H | DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 10031CH | DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 100324H | DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 10032CH | CREG1 [R/W] 00000000 00000110 | | | | |

Appendix B Interrupt Vectors

This appendix lists the interrupt vector table.

The interrupt vector table lists the interrupt vectors and interrupt control registers assigned to each MB91360 interrupt.

| Interrupt | Interrupt number | | Interrupt level ¹ | | Interrupt vector ² | | RN |
|--|------------------|--------------|------------------------------|------------------|-------------------------------|------------------------|----|
| | Decimal | Hexa-decimal | Setting Register | Register address | Offset | Default Vector address | |
| Reset ⁶ | 0 | 00 | - | - | 0x3FC | 0x000FFFFC | |
| Mode vector ⁶ | 1 | 01 | - | - | 0x3F8 | 0x000FFFF8 | |
| System reserved | 2 | 02 | - | - | 0x3F4 | 0x000FFFF4 | |
| System reserved | 3 | 03 | - | - | 0x3F0 | 0x000FFFF0 | |
| System reserved | 4 | 04 | - | - | 0x3EC | 0x000FFFE4 | |
| System reserved | 5 | 05 | - | - | 0x3E8 | 0x000FFFE8 | |
| System reserved | 6 | 06 | - | - | 0x3E4 | 0x000FFFE4 | |
| Co-processor fault trap ⁴ | 7 | 07 | - | - | 0x3E0 | 0x000FFFE0 | |
| Co-processor error trap ⁴ | 8 | 08 | - | - | 0x3DC | 0x000FFFD4 | |
| INTE instruction ⁴ | 9 | 09 | - | - | 0x3D8 | 0x000FFFD8 | |
| Instruction break exception ⁴ | 10 | 0A | - | - | 0x3D4 | 0x000FFFD4 | |
| Operand break trap ⁴ | 11 | 0B | - | - | 0x3D0 | 0x000FFFD0 | |
| Step trace trap ⁴ | 12 | 0C | - | - | 0x3CC | 0x000FFFC4 | |
| NMI interrupt(tool) ⁴ | 13 | 0D | - | - | 0x3C8 | 0x000FFFC8 | |
| Undefined instruction exception | 14 | 0E | - | - | 0x3C4 | 0x000FFFC4 | |
| NMI request | 15 | 0F | FH fixed | | 0x3C0 | 0x000FFFC0 | |
| External Interrupt 0 | 16 | 10 | ICR00 | 0x440 | 0x3BC | 0x000FFFB4 | 4 |
| External Interrupt 1 | 17 | 11 | ICR01 | 0x441 | 0x3B8 | 0x000FFFB8 | 5 |
| External Interrupt 2 | 18 | 12 | ICR02 | 0x442 | 0x3B4 | 0x000FFFB4 | 8 |
| External Interrupt 3 | 19 | 13 | ICR03 | 0x443 | 0x3B0 | 0x000FFFB0 | 9 |
| External Interrupt 4 | 20 | 14 | ICR04 | 0x444 | 0x3AC | 0x000FFFA4 | |
| External Interrupt 5 | 21 | 15 | ICR05 | 0x445 | 0x3A8 | 0x000FFFA8 | |
| External Interrupt 6 | 22 | 16 | ICR06 | 0x446 | 0x3A4 | 0x000FFFA4 | |

| | | | | | | | |
|------------------------------|----|----|-------|-------|-------|------------|----|
| External Interrupt 7 | 23 | 17 | ICR07 | 0x447 | 0x3A0 | 0x000FFFA0 | |
| Reload Timer 0 | 24 | 18 | ICR08 | 0x448 | 0x39C | 0x000FFF9C | 6 |
| Reload Timer 1 | 25 | 19 | ICR09 | 0x449 | 0x398 | 0x000FFF98 | 7 |
| Reload Timer 2 | 26 | 1A | ICR10 | 0x44A | 0x394 | 0x000FFF94 | |
| CAN 0 RX | 27 | 1B | ICR11 | 0x44B | 0x390 | 0x000FFF90 | |
| CAN 0 TX/NS | 28 | 1C | ICR12 | 0x44C | 0x38C | 0x000FFF8C | |
| CAN 1 RX | 29 | 1D | ICR13 | 0x44D | 0x388 | 0x000FFF88 | |
| CAN 1 TX/NS | 30 | 1E | ICR14 | 0x44E | 0x384 | 0x000FFF84 | |
| CAN 2 RX ⁷ | 31 | 1F | ICR15 | 0x44F | 0x380 | 0x000FFF80 | |
| CAN 2 TX/NS ⁷ | 32 | 20 | ICR16 | 0x450 | 0x37C | 0x000FFF7C | |
| CAN 3 RX ⁵ | 33 | 21 | ICR17 | 0x451 | 0x378 | 0x000FFF78 | |
| CAN 3 TX/NS ⁵ | 34 | 22 | ICR18 | 0x452 | 0x374 | 0x000FFF74 | |
| PPG 0/1 | 35 | 23 | ICR19 | 0x453 | 0x370 | 0x000FFF70 | |
| PPG 2/3 | 36 | 24 | ICR20 | 0x454 | 0x36C | 0x000FFF6C | |
| PPG 4/5 ⁷ | 37 | 25 | ICR21 | 0x455 | 0x368 | 0x000FFF68 | |
| PPG 6/7 ⁷ | 38 | 26 | ICR22 | 0x456 | 0x364 | 0x000FFF64 | |
| Reload Timer 3 ⁷ | 39 | 27 | ICR23 | 0x457 | 0x360 | 0x000FFF60 | |
| Reload Timer 4 ⁷ | 40 | 28 | ICR24 | 0x458 | 0x35C | 0x000FFF5C | |
| Reload Timer 5 ⁷ | 41 | 29 | ICR25 | 0x459 | 0x358 | 0x000FFF58 | |
| ICU 0/1 | 42 | 2A | ICR26 | 0x45A | 0x354 | 0x000FFF54 | |
| OCU 0/1 | 43 | 2B | ICR27 | 0x45B | 0x350 | 0x000FFF50 | |
| ICU 2/3 | 44 | 2C | ICR28 | 0x45C | 0x34C | 0x000FFF4C | |
| OCU 2/3 ⁷ | 45 | 2D | ICR29 | 0x45D | 0x348 | 0x000FFF48 | |
| ADC | 46 | 2E | ICR30 | 0x45E | 0x344 | 0x000FFF44 | 14 |
| Timebase Overflow | 47 | 2F | ICR31 | 0x45F | 0x340 | 0x000FFF40 | |
| Free Running Counter 0 | 48 | 30 | ICR32 | 0x460 | 0x33C | 0x000FFF3C | |
| Free Running Counter 1 | 49 | 31 | ICR33 | 0x461 | 0x338 | 0x000FFF38 | |
| SIO 0 | 50 | 32 | ICR34 | 0x462 | 0x334 | 0x000FFF34 | |
| SIO 1 | 51 | 33 | ICR35 | 0x463 | 0x330 | 0x000FFF30 | |
| Sound Generator ⁷ | 52 | 34 | ICR36 | 0x464 | 0x32C | 0x000FFF2C | |
| UART 0 RX | 53 | 35 | ICR37 | 0x465 | 0x328 | 0x000FFF28 | 0 |
| UART 0 TX | 54 | 36 | ICR38 | 0x466 | 0x324 | 0x000FFF24 | 1 |
| UART 1 RX ⁷ | 55 | 37 | ICR39 | 0x467 | 0x320 | 0x000FFF20 | 2 |
| UART 1 TX ⁷ | 56 | 38 | ICR40 | 0x468 | 0x31C | 0x000FFF1C | 3 |

| | | | | | | | |
|--|-----------------|----------------|---------|-------|----------------------|--------------------------------|----|
| UART 2 RX ⁷ | 57 | 39 | ICR41 | 0x469 | 0x318 | 0x000FFF18 | 10 |
| UART 2 TX ⁷ | 58 | 3A | ICR42 | 0x46A | 0x314 | 0x000FFF14 | 11 |
| I2C | 59 | 3B | ICR43 | 0x46B | 0x310 | 0x000FFF10 | 13 |
| Alarm Comparator | 60 | 3C | ICR44 | 0x46C | 0x30C | 0x000FFF0C | |
| RTC / Calibration ⁸ (Watchtimer) | 61 | 3D | ICR45 | 0x46D | 0x308 | 0x000FFF08 | |
| DMA | 62 | 3E | ICR46 | 0x46E | 0x304 | 0x000FFF04 | |
| Delayed interrupt activation bit | 63 | 3F | ICR47 | 0x46F | 0x300 | 0x000FFF00 | |
| System reserved ^{*3} | 64 | 40 | - | - | 0x2FC | 0x000FFEFC | |
| System reserved ^{*3} | 65 | 41 | - | - | 0x2F8 | 0x000FFE8 | |
| Security vector | 66 | 42 | | | 0x2F4 | 0x000FEF4 | |
| System reserved | 67 | 43 | (ICR51) | 0x473 | 0x2F0 | 0x000FEF0 | |
| System reserved | 68 | 44 | (ICR52) | 0x474 | 0x2EC | 0x000FEFEC | |
| System reserved | 69 | 45 | (ICR53) | 0x475 | 0x2E8 | 0x000FEFEE8 | |
| System reserved | 70 | 46 | (ICR54) | 0x476 | 0x2E4 | 0x000FEFEE4 | |
| System reserved | 71 | 47 | (ICR55) | 0x477 | 0x2E0 | 0x000FEFEE0 | |
| System reserved | 72 | 48 | (ICR56) | 0x478 | 0x2DC | 0x000FEFDC | |
| System reserved | 73 | 49 | (ICR57) | 0x479 | 0x2D8 | 0x000FEFD8 | |
| System reserved | 74 | 4A | (ICR58) | 0x47A | 0x2D4 | 0x000FEFD4 | |
| System reserved | 75 | 4B | (ICR59) | 0x47B | 0x2D0 | 0x000FEFD0 | |
| System reserved | 76 | 4C | (ICR60) | 0x47C | 0x2CC | 0x000FEFCC | |
| System reserved | 77 | 4D | (ICR61) | 0x47D | 0x2C8 | 0x000FEFC8 | |
| System reserved | 78 | 4E | (ICR62) | 0x47E | 0x2C4 | 0x000FEFC4 | |
| System reserved | 79 | 4F | (ICR63) | 0x47F | 0x2C0 | 0x000FEFC0 | |
| Used by the INT instruction. | 80 to 255 | 50 to FF | - | - | 0x2BC to 0x000 | 0x000FEFBC to 0x000FFC00 | |

^{*1} The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

^{*2} The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset. After execution of the internal boot ROM TBR is set to 0x00FFC00.

^{*3} Used by REALOS

^{*4} System reserved

^{*5} Only available on MB91V360/MB91FV360

^{*6} Mode and reset vector cannot be changed, for their contents see IO map

^{*7} not available on MB91F367GA/F368GA

*⁸ calibration unit is not available on F365G

Remarks:

The 1-Kbyte area from the address specified in TBR is the EIT vector area.

Each vector consists of four bytes. The following formula shows the relationship between the vector number and vector address.

$$\begin{aligned} \text{vctadr} &= \text{TBR} + \text{vctofs} \\ &= \text{TBR} + (3\text{FCH} - 4 \times \text{vct}) \end{aligned}$$

vctadr:Vector address

vctofs:Vector offset

vct:Vector number