

**Attenuator, Digital, 5-Bit
0.1-20.0 GHz**

MAATGM0004

Rev—
Preliminary Information

Features

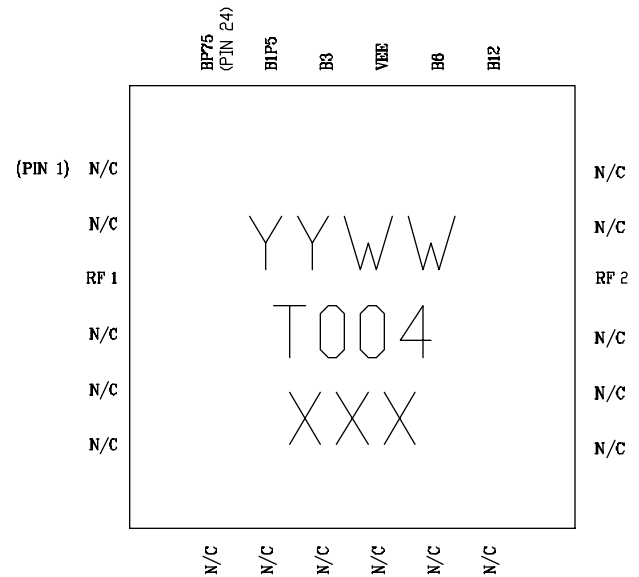
- ◆ 5-Bit Attenuator, 22 dB Range, LSB = 0.75 dB
- ◆ 0.1 to 20.0 GHz Operation
- ◆ 4 mm, 24-Lead PQFN
- ◆ TTL Control Inputs
- ◆ MSAG™ Process

Description

The MAATGM0004 is a 5-bit bi-directional Digital Attenuator with Parallel Input Control. This product is fully matched to 50 ohms on both the input and output.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using M/A-COM's GaAs Multi-function Self-Aligned Gate (MSAG) Process.

The 4 mm PQFN package has a lead-free lead finish that is RoHS compliant and compatible with a 260°C reflow temperature. The package also features low lead inductance and an excellent thermal path. The MTTF is 1,000,000 hours at 170°C.



Primary Applications

- ◆ VSAT
- ◆ Point-to-Point Communications
- ◆ Weather Radar
- ◆ Military Radar
- ◆ Electronic Warfare

Also Available in:

Description	Die	Plastic Package Sample Board
Part Number	MAATGM0004-DIE	MAAT-000004-SMB003

Electrical Characteristics: $T_B = 25^\circ\text{C}$, $Z_0 = 50\Omega$, $V_{EE} = -5\text{V}$

Parameter	Symbol	Typical	Units
Bandwidth	f	0.1-20	GHz
Attenuation Range	ΔG	22	dB
Digital Supply Current	IEE	<10	mA
Reference State Insertion Loss (<10 GHz)	IL	<4	dB
Reference State Insertion Loss (10 - 20 GHz)	IL	<6	dB
VSWR (All States - <10 GHz)	VSWR	1.5:1	
VSWR (All States - 10 - 20 GHz)	VSWR	3:1	
Attenuation Error (<10 GHz)	Err	-1.5 to +0.1	dB
Attenuation Error (10 - 20 GHz)	Err	-0.5 to +2.0	dB
Phase Variation (All States - <10 GHz)	$\Delta\Phi$	< ± 5	°
Phase Variation (All States - 10 - 20 GHz)	$\Delta\Phi$	< ± 20	°

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Maximum Ratings¹

Parameter	Symbol	Absolute Maximum	Units
Input Power	P _{IN}	36	dBm
Source Supply Voltage	V _{EE}	-6	V
Junction Temperature	T _J	170	°C
Storage Temperature	T _{STG}	-55 to +150	°C

1. Operation beyond these limits may result in permanent damage to the part.

Recommended Operating Conditions²

Characteristic	Symbol	Min	Typ	Max	Unit
Control Voltage	A1 thru A6				
Logic High		3	5	5	V
Logic Low		0	0	0.4	V
Junction Temperature	T _J			150	°C
Digital Supply Voltage	V _{EE}	-5.2	-5	-4.8	V

2. Operation outside of these ranges may reduce product reliability.

Truth Table³

Pin	Description	Level	State
19	12.0 dB Attenuation Bit	Logic High	Attenuation ≈ 12.0 dB
20	6.0 dB Attenuation Bit	Logic High	Attenuation ≈ 6.0 dB
21	VEE: DC Suply Voltage	-5V	ON
22	3.0 dB Attenuation Bit	Logic High	Attenuation ≈ 3.0 dB
23	1.5 dB Attenuation Bit	Logic High	Attenuation ≈ 1.5 dB
24	0.75 dB Attenuation Bit : LSB	Logic High	Attenuation ≈ 0.75 dB

3. All Attenuation Bits at Logic Low = Reference State.

Operating Instructions

This device is static and light sensitive. Operation of the digital circuitry can be impaired under high intensity light, e.g., microscope light.

No voltage sequencing is required to operate this part.



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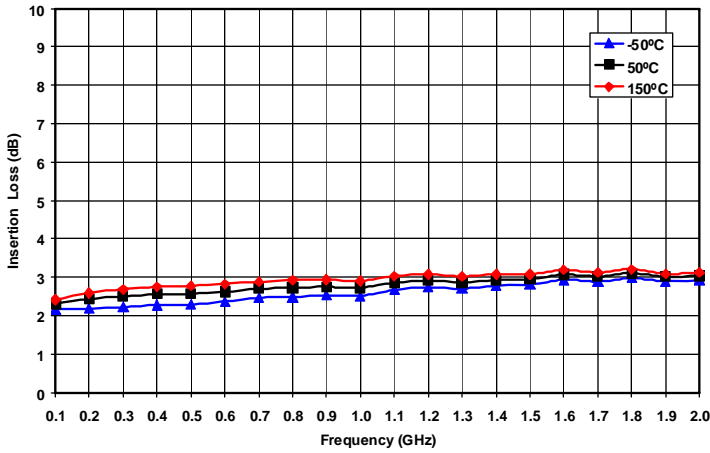


Figure 1. Insertion Loss vs. Frequency & Case Temperature - Reference State

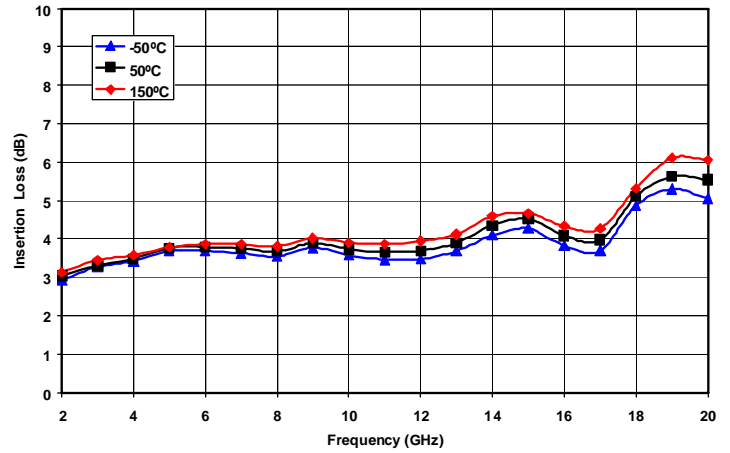


Figure 2. Insertion Loss vs. Frequency & Case Temperature - Reference State

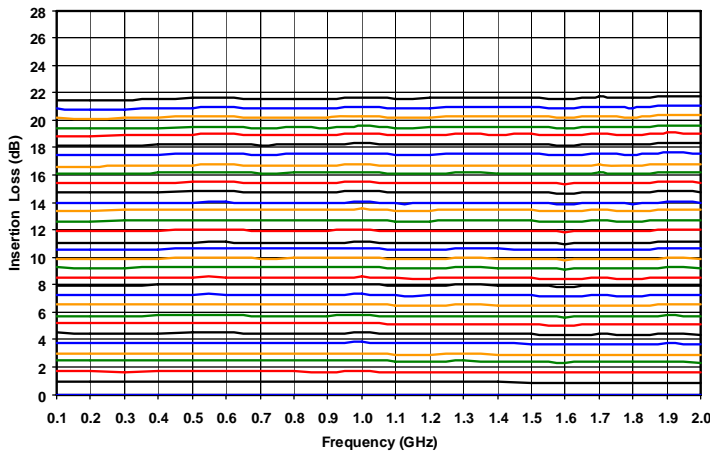


Figure 3. Relative Insertion Loss vs. Frequency & Attenuation State - All States

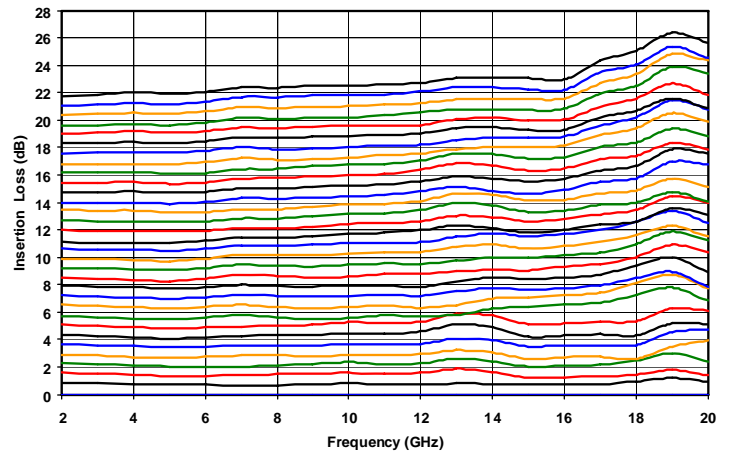


Figure 4. Relative Insertion Loss vs. Frequency & Attenuation State - All States

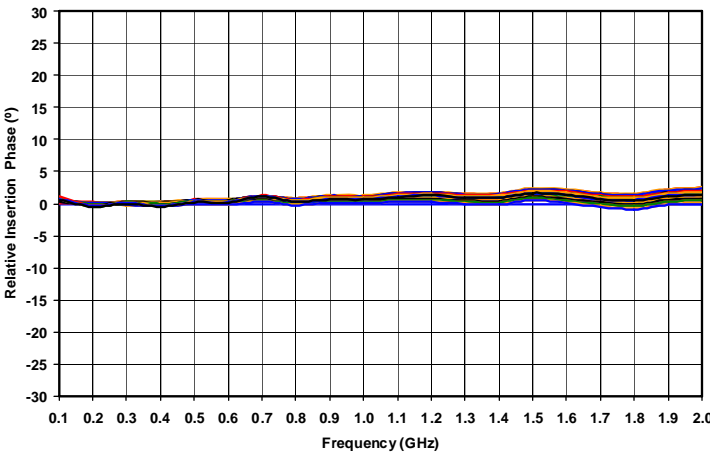


Figure 5. Relative Insertion Phase vs. Frequency & Attenuation State - All States

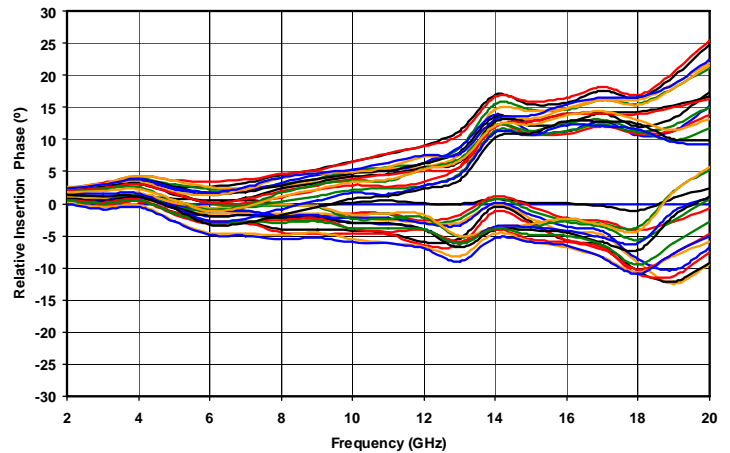


Figure 6. Relative Insertion Phase vs. Frequency & Attenuation State - All States

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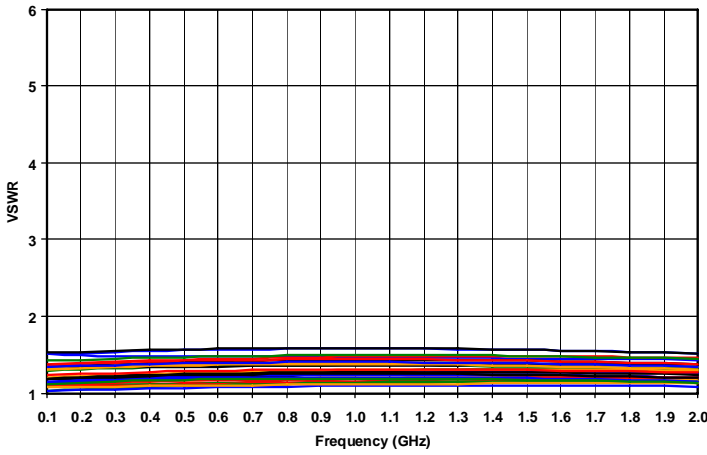


Figure 7. VSWR (RF Port 1) vs. Frequency & Attenuation State - All States

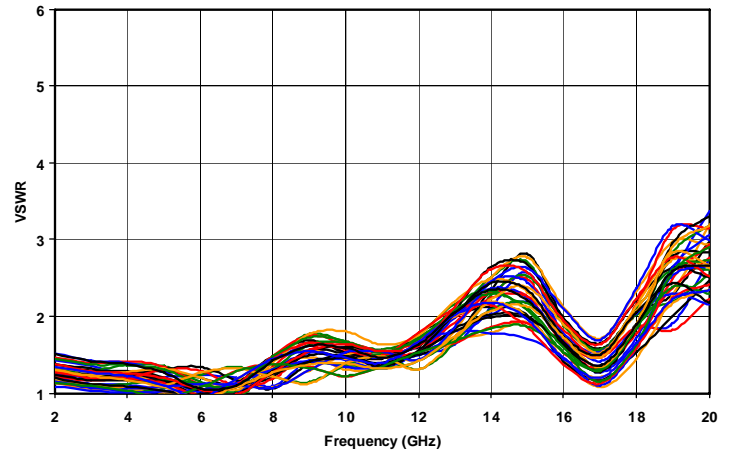


Figure 8. VSWR (RF Port 1) vs. Frequency & Attenuation State - All States

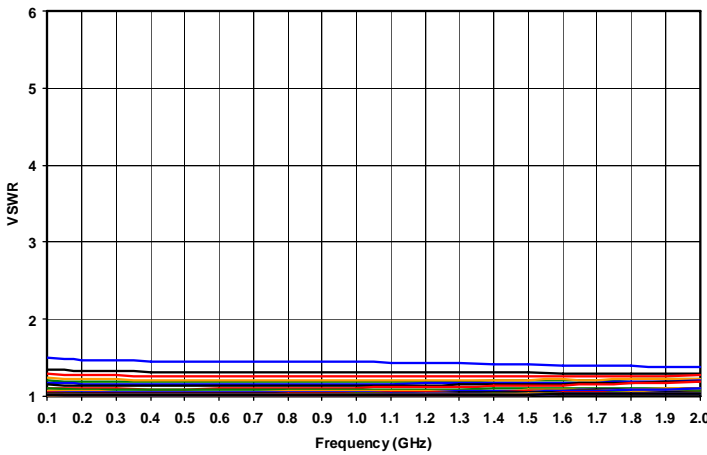


Figure 9. VSWR (RF Port 2) vs. Frequency & Attenuation State - All States

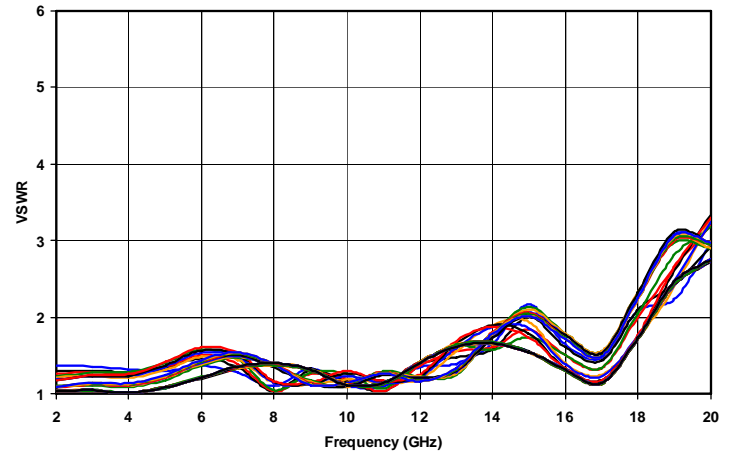


Figure 10. VSWR (RF Port 2) vs. Frequency & Attenuation State - All States

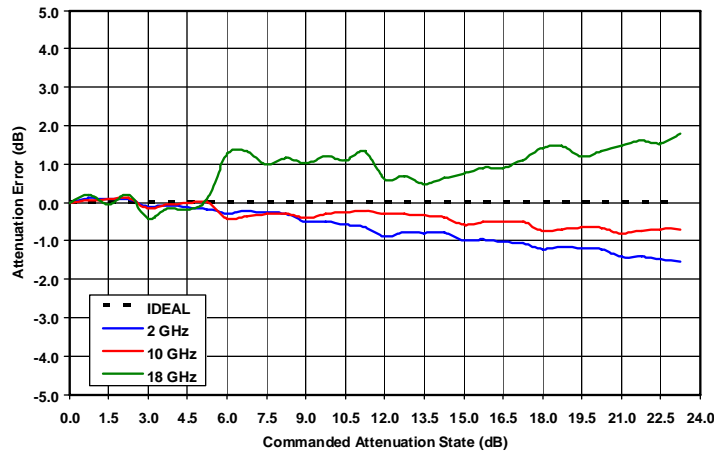


Figure 11. Typical Attenuation Error vs. Commanded Attenuation State & Frequency

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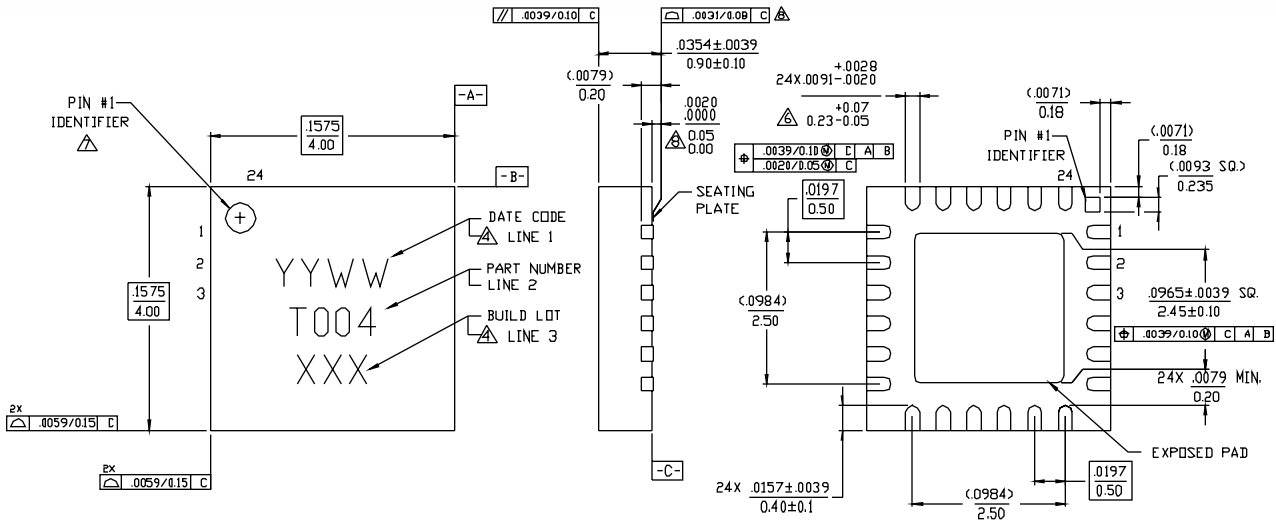


Figure 12. 4mm PQFN 24 Lead Package Drawing

Reference JEDEC M0-220 (see <http://www.jedec.org>), VAR. VJJC-3 (Issue E) for additional dimensional and tolerance information.

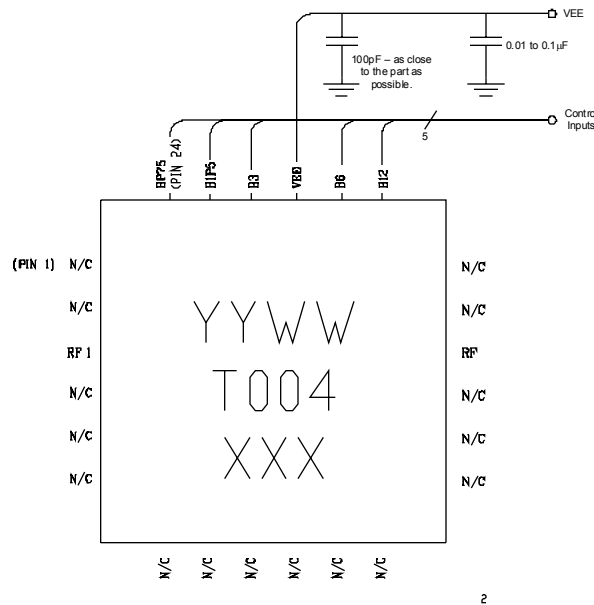


Figure 13. Recommended Bias Configuration

Note: The exposed pad centered on the package bottom must be connected to RF and dc ground for proper electrical and thermal operation.

Refer to M/A-COM Application Note **Surface Mounting Instructions for PQFN Packages #S2083*** for assembly guidelines.

*Application Notes can be found by going to M/A-COM's web page (<http://www.macom.com/Application%20Notes/index.htm>) and selecting the required Application Note.

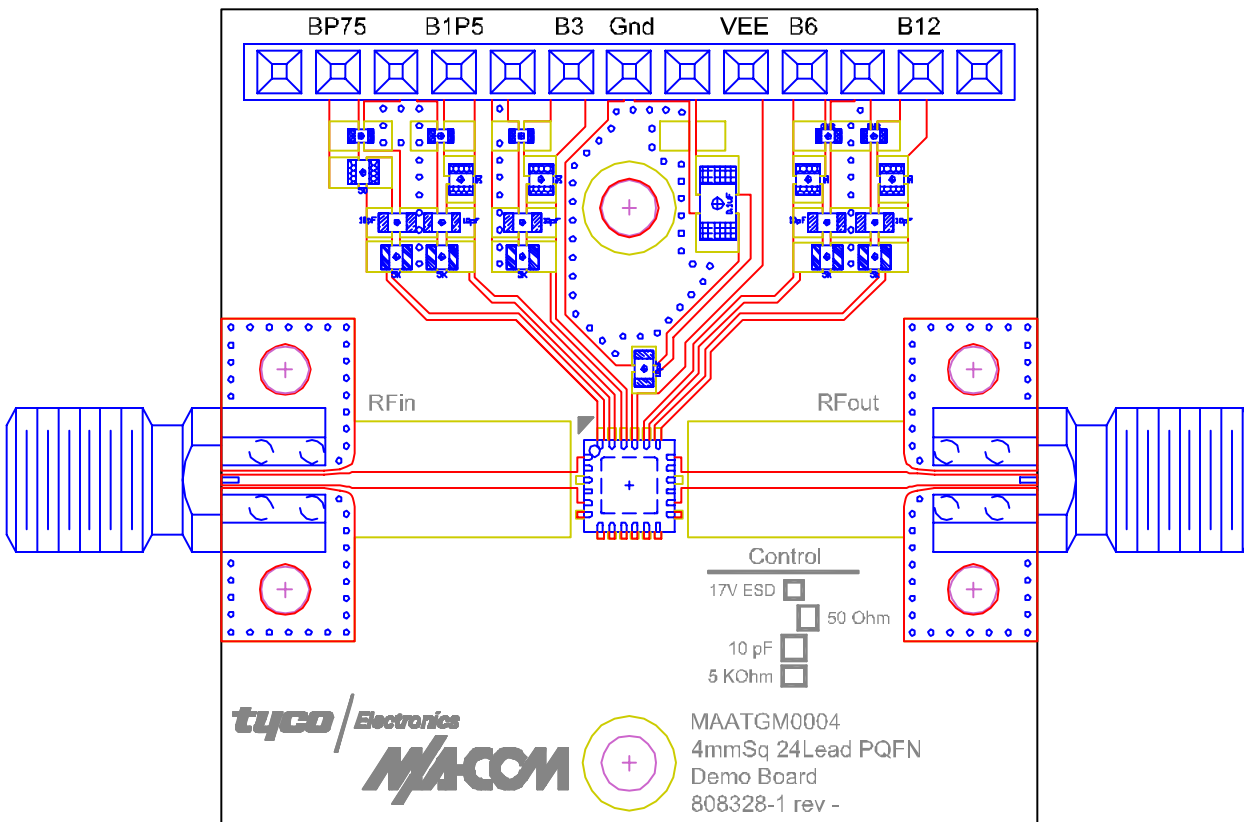


Figure 14. Demonstration Board PN MAAT-000004-SMB003 (available upon request).