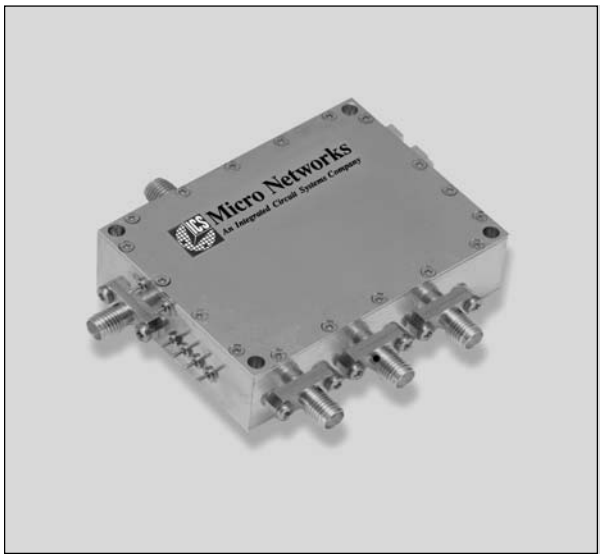
# M830 Series

## 12.249Gb/s OC-192 Clock & Data Recovery Transmitter Module




## FEATURES

- **Superior PLL-based jitter performance**
- **8psec p-p jitter**
- **0.9Vp-p complementary data outputs**
- **1 UI externally adjustable clock phase**
- **200mVp-p input sensitivity**
- **Optional adjustable bias @ data input to decision circuit**
- **Externally adjustable decision threshold**

## APPLICATIONS

- **SONET OC-192 and SDH STM Physical Layer and Clock and Data Recovery Applications Incorporating Forward Error Correction**

## DESCRIPTION

The M830 Series CDR module is specifically designed to regenerate the spectral clock component from an incoming NRZ data stream, incorporating forward error correction, and output a low-jitter clock and retimed complementary data.

The module utilizes a phase-locked loop architecture incorporating a high-stability, low noise SAW VCO to provide extremely low jitter clock and data outputs. The incoming data is frequency doubled to recover the clock component. The clock signal is then filtered by a microwave band pass filter to remove wide band noise and spurious signal. This signal is further filtered using the narrow band SAW VCO based PLL to minimize the noise close to the carrier. The low jitter clock is then used to retime the data and serves as the module's clock output. The module provides user-controlled clock phase shifter and output data crossover adjustments to optimize system performance.

PLL lock-in range and loop transfer characteristics are optimized for minimal jitter in accordance with ITU and Bellcore standards for SONET/SDH systems.

## ABSOLUTE MAX RATINGS

| | |
|---|---|
| Operating Temp. Range (Case) | 0°C to +70°C |
| Storage Temp. Range (Ambient) | -40°C to +125°C |
| Power Supply Voltage | |
| Vcc: | +5.25Vdc |
| Vee: | -5.25Vdc |
| Ref Voltage | +0.3 to -1.6V |
| Phase Shift Control | 0 to +15V |

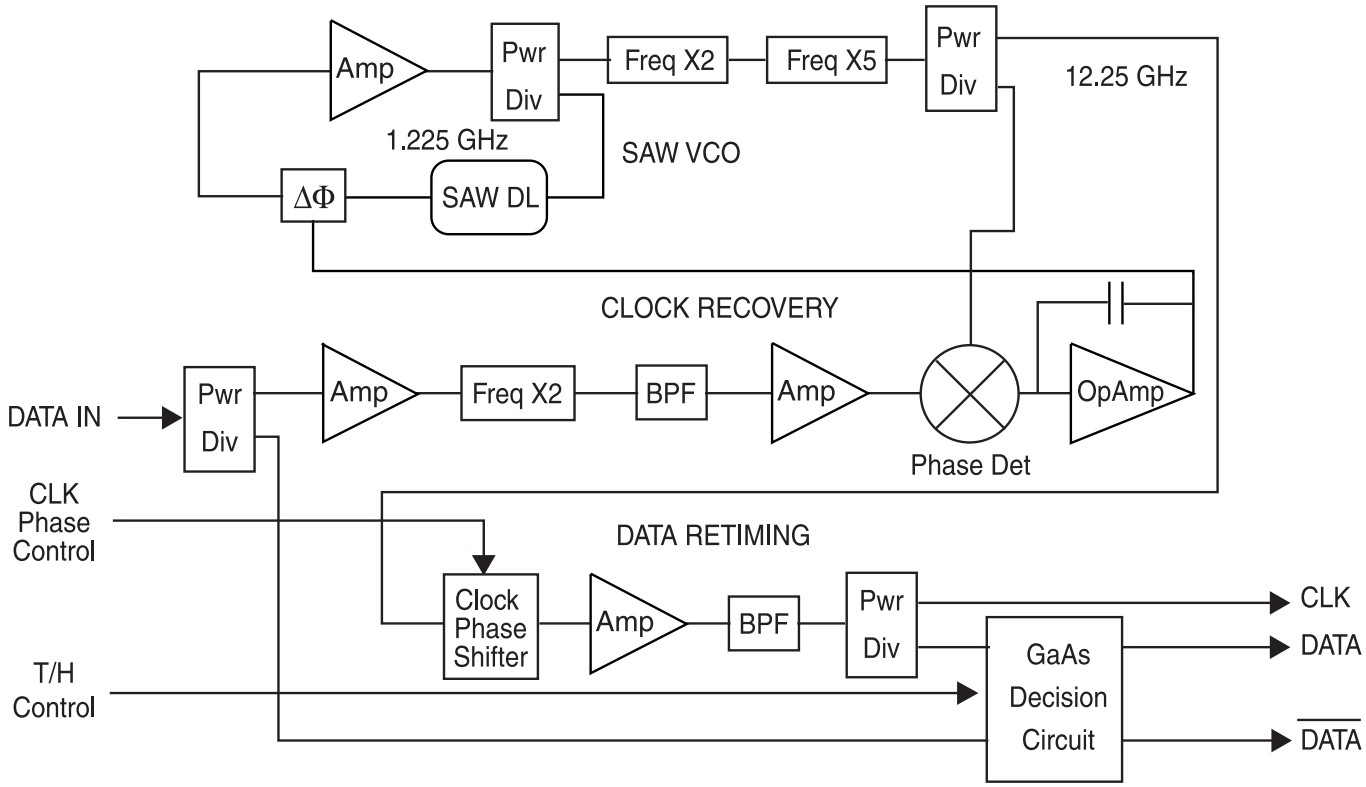
**ISO 9001 Registered**

## SPECIFICATIONS

*Specifications @ Vcc = +5.0 Volts, Vee = -5.0 Volts, Data in = $2^{31}$-1 PRBS NRZ, Mark ratio = 1:2, and $T_A$ = +25°C unless otherwise specified*

| PARAMETER | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Data Rate | | 12.2493 | | Gb/s | NRZ |
| Data Input Level | 200 | | 600 | mVp-p | Single-ended, 50Ω, AC coupled |
| Data Input Return Loss | | 10 | 12 | dB | 50MHz to 7GHz |
| Data Output Voltage | 750 | 900 | 1100 | mVp-p | Data & $\overline{\text{Data}}$ |
| Data Output Jitter | | 7.5 | 10 | psec p-p | $2^7$–1 PRBS NRZ |
| Data Output Duty Cycle Distortion | | 2.5 | 5 | % | |
| Data Output Rise Time (20% to 80%) | | 25 | 35 | psec | 50Ω, AC coupled |
| Data Output Fall Time (80% to 20%) | | 25 | 35 | psec | 50Ω, AC coupled |
| Data Output Return Loss | 10 | 12 | | dB | 50MHz to 9GHz |
| PLL Loop BW | | .3 | | MHz | |
| Decision Threshold Control | 10 | | 90 | % | Relative to max Data Input Voltage Ref -0.2 to -0.75V |
| Decision Threshold Control Voltage Range | -0.75 | | -0.2 | Volts | Internal load of 45Ω to -0.45V |
| Clock Output Level | 800 | 1200 | 1400 | mVp-p | 50Ω, AC coupled |
| Clock Phase Control | 1 | | | UI | |
| Clock Phase Control Voltage | 0 | | +15 | Volts | 10kΩ, minimum load impedance |
| Clock SSB Phase Noise | | | | | |
| @100Hz Offset | | -70 | | dBc/Hz | $2^{31}$–1 PRBS NRZ |
| @1kHz Offset | | -85 | | dBc/Hz | |
| @10kHz Offset | | -90 | | dBc/Hz | |
| Clock Jitter | | 7.5 | 9 | psec p-p | $2^7$–1 PRBS NRZ |
| Spurious Output | | -50 | | dBc | |
| Harmonic Output | | -30 | | dBc | |
| Supply Voltage | | | | | |
| Vcc | +4.75 | +5.0 | +5.25 | Volts | |
| Vee | -5.25 | -5.0 | -4.75 | Volts | |
| Supply Current | | | | | |
| Icc | | 450 | 600 | mA | |
| Iee | | 300 | 550 | mA | |

## BLOCK DIAGRAM




The M830 clock and data recovery module has a SAW VCO based phase-locked loop architecture. The 1.225GHz fundamental VCO is implemented as a transmission oscillator. The oscillator loop includes the SAW resonator that has a linear phase with frequency characteristic, a linear voltage controlled phase shifter, loop amplifier, and power divider to couple signal from the loop. The oscillator is frequency doubled to 2.450GHz and band pass filtered. The 2.450GHz is then multiplied by five to the final frequency of 12.25GHz. The output of the VCO is power divided to provide an input to the phase detector and a clock signal.

The input data is power divided to provide inputs to the decision circuit and the clock recovery circuitry. The input to the clock recovery circuit is amplified and applied to an analog frequency doubler to extract a clock spectral component from the NRZ data input stream. The 12.25GHz doubler output is band pass filtered and amplified.

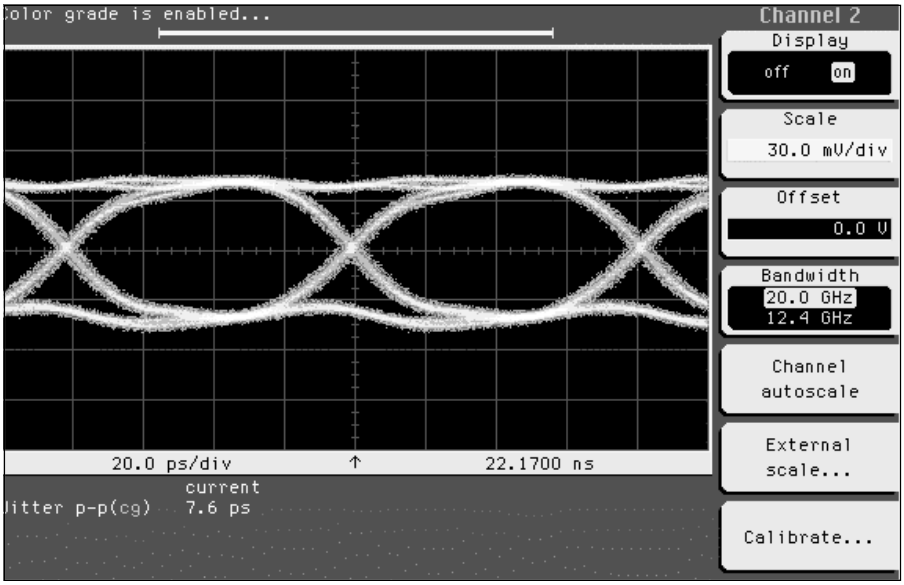
One VCO output and the clock extracted from the input data serve as inputs to a microwave phase detector. The phase detector output is applied to an integrator circuit. The integrator output controls the phase shifter in the SAW VCO, completing the phase-lock loop. The phase-locked loop causes the low noise VCO output to be phase-locked to the clock signal extracted from the NRZ input data, providing a low jitter clock signal.

The clock signal is applied to a phase shifter that allows the timing between the input data and clock to be adjusted for optimum performance. The phase shifter output is amplified and band pass filtered to provide a low jitter and low spurious clock. The clock is power divided to provide the clock output of the module and the clock input to the decision circuit.

The decision circuit is a high speed D flip-flop. In addition to the clock and data inputs, a user adjustable decision threshold voltage is available. This voltage is used to optimize the retimed data. The CDR threshold and phase shifter do not require adjustment over the temperature and input data level ranges.

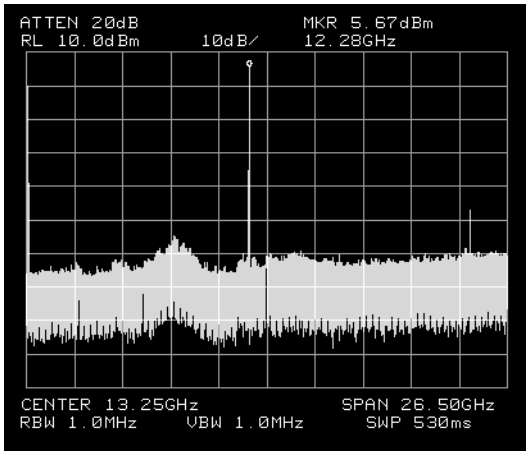
The clock output of the CDR is a low spurious sinusoidal signal and the complementary data outputs are AC coupled ECL signals. DC coupled ECL compatible data outputs are available.

## DATA OUTPUT EYE DIAGRAM

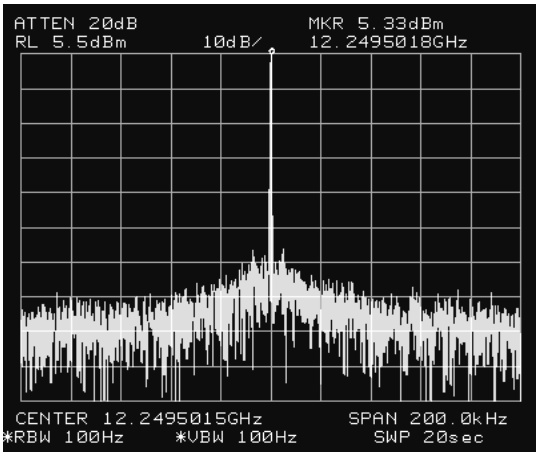



Data Output Eye Diagram

## CLOCK SPECTRUM




Narrow Band Clock Spectrum




Wide Band Clock Output Spectrum

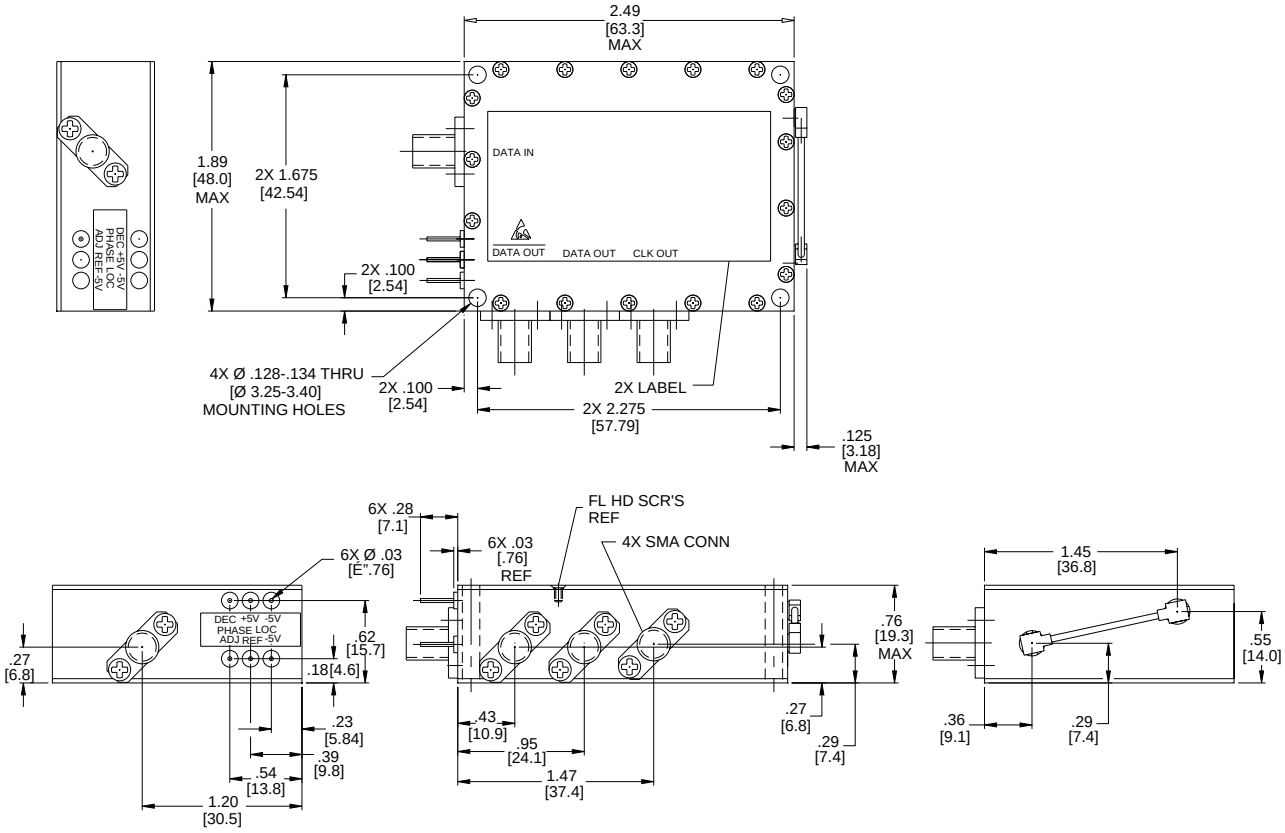
## ORDERING INFORMATION & MECHANICAL DIMENSIONS

**Part Number:** M830 X XXXXX.XX X X

- Series
- No of Inputs
  - D = Single Input
- Frequency
- Temperature Range
  - K = 0 to +70°C
- Package Type
  - C = Case/Module Package

### PIN DESCRIPTIONS

| Symbol | Name | Description |
|---|---|---|
| DATA IN | Data Input | AC coupled 50Ω data input |
| DATA OUT | Data Output (non-inverted) | AC coupled 50Ω data output |
| $\overline{\text{DATA OUT}}$ | Data Output (inverted) | AC coupled 50Ω data output |
| CLK OUT | Clock Output (sinusoidal) | AC coupled 50Ω clock output |
| PHASE ADJ | Phase Shift Adjust | User input to phase shift the recovered clock over a 100ps range. The control voltage range is 0 to 15V. |
| REF | Decision Threshold Adjustment | User input to adjust the decision circuit threshold. The control range is -0.2V to -0.75V. |
| LOC DEC | Lock Detect | TTL output indicating PLL loss of lock. TTL "1" indicates lock. TTL "0" indicates loss of lock. |
| +5V | +5V Power Supply | Positive power supply input. |
| -5V | -5V Power Supply | Negative power supply input. |
| GND | Power Supply Ground Connection | Ground lug to allow connection of power supply returns to case ground. |



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