

# M61314SP

## I<sup>2</sup>C BUS CONTROLLED VIDEO PRE-AMP FOR HIGH RESOLUTION COLOR DISPLAY

### DESCRIPTION

M61314SP is Semiconductor Integrated Circuit for CRT Display Monitor. It includes OSD Blanking, OSD Mixing, Retrace Blanking, Video detector, Sync Sepa, Wide band Amplifier. Brightness Control, Main/Sub Contrast, OSD level, 4ch D/A OUT, Video response adjust can be controlled by I<sup>2</sup>C Bus.

### FEATURES

■ Frequency Band Width

RGB: 180MHz (3Vp-p at -3dB)  
 OSD: 80MHz

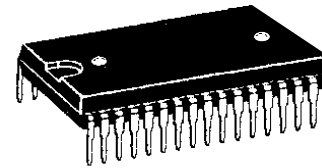
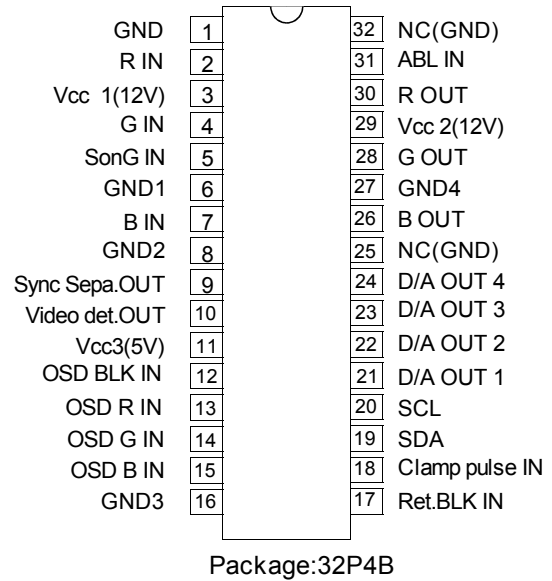
■ Input

RGB: 0.7Vp-p (typical)  
 OSD: 3.5V~5V (positive)  
 OSD BLK: 3.5V~5V (positive)  
 Retrace BLK: 2.5V~5V (positive)  
 Clamp Pulse: 2.5V~5V (positive)

■ Output

RGB: 5Vp-p  
 (at Brightness less than 2V DC)  
 OSD: 4Vp-p  
 (at Brightness less than 2V DC)  
 Sync OUT: 5Vp-p

### PIN CONFIGURATION (TOP VIEW)



32 pin plastic SDIP

### RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	-----	11.50V ~ 12.50V (V3, V29)
		4.75V ~ 5.25V (V11)
Rated Supply Voltage	-----	12.00V (V3, V29)
		5.00V (V11)

### APPLICATION EXAMPLE

CRT Display Monitor

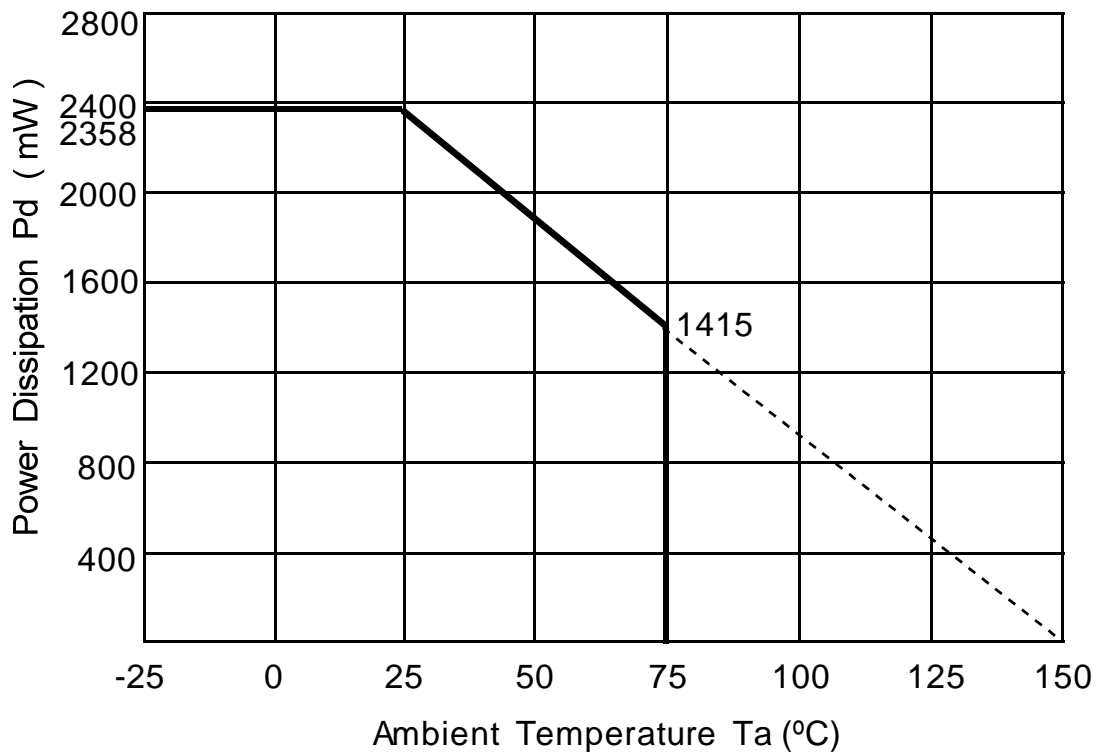
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## ABSOLUTE MAXIMUM RATINGS(Ambient temperature 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage(Pin3,29)	Vcc12	13.0	V
Supply voltage(Pin11)	Vcc5	6.0	V
Power dissipation	Pd	2358	mW
Ambient temperature	Topr	-20 ~ +75	°C
Storage temperature	Tstg	-40 ~ +150	°C
Recommend supply 12	Vopr12	12.0	V
Recommend supply 5	Vopr5	5.0	V
Voltage range 12	Vopr'12	11.5 ~ 12.5	V
Voltage range 5	Vopr'5	4.75 ~ 5.25	V

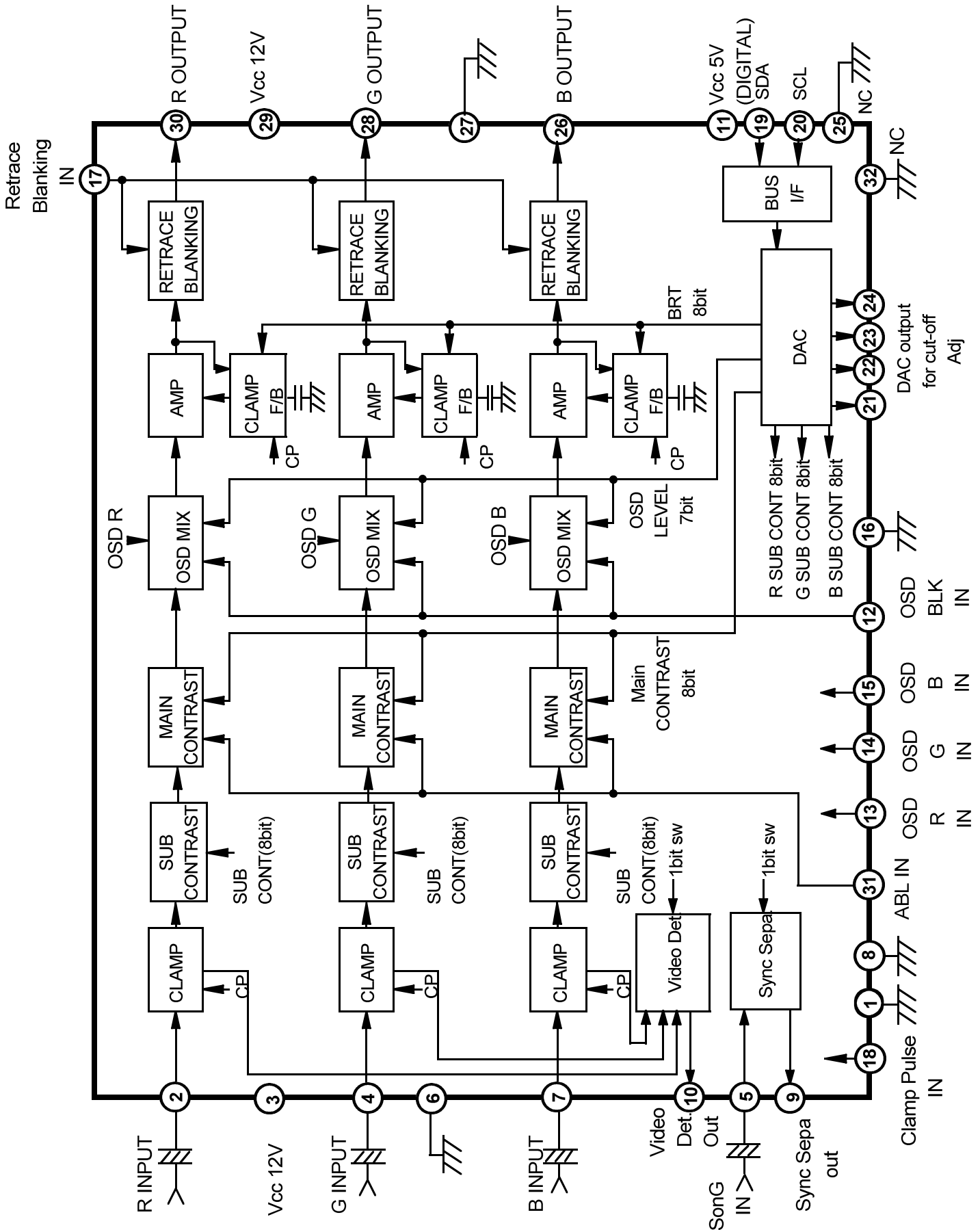
## THERMAL DERATING



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## BLOCK DIAGRAM



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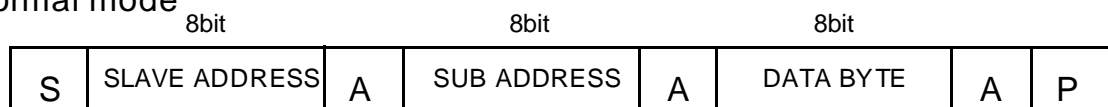
### BUS CONTROL TABLE

(1) Slave address:

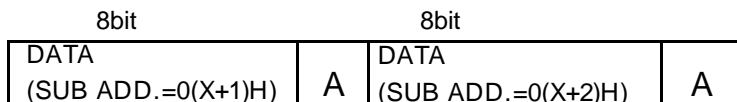
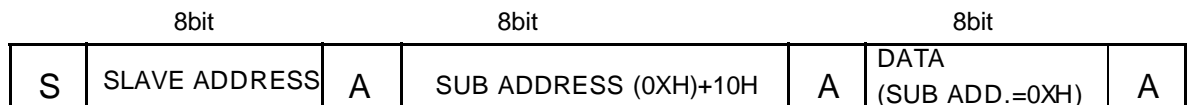
D7	D6	D5	D4	D3	D2	D1	R/W	
1	0	0	0	1	0	0	0	=88H

(2) Slave receiver format:

normal mode



auto increment mode



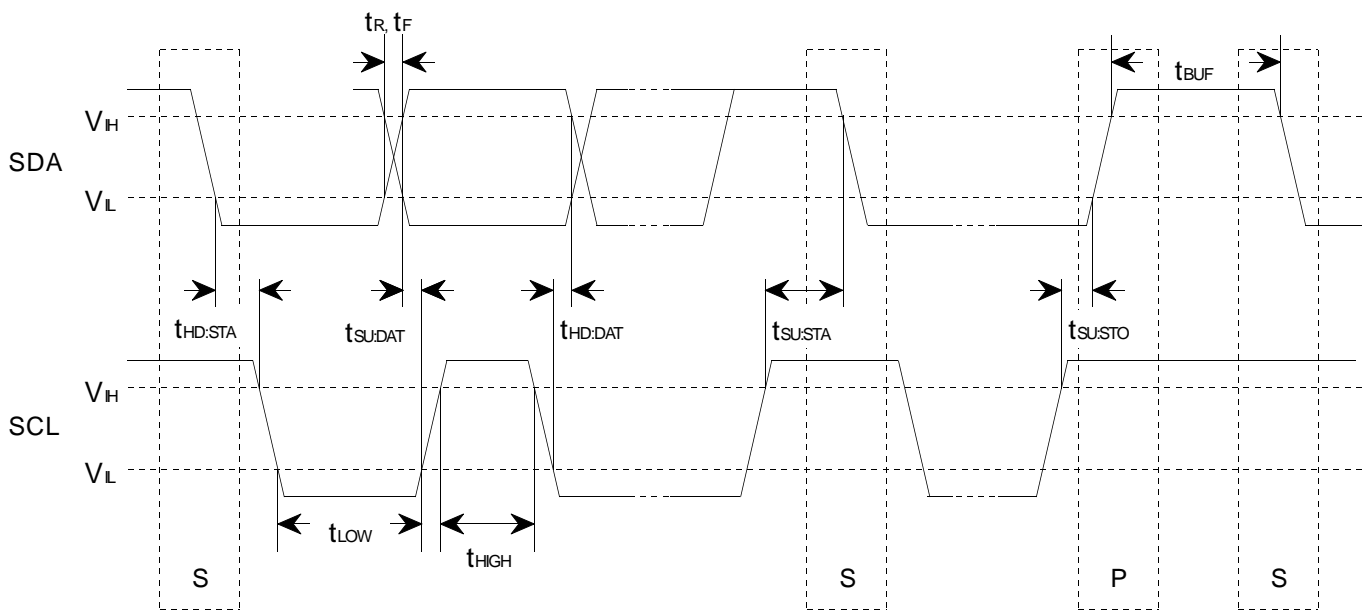
|  
|  
|  
|

S : Start condition  
A : Acknowledge  
P : Stop condition

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**SDA, SCL CHARACTERISTIC**

parameter	symbol	MIN	MAX	unit
min. input LOW voltage	V <sub>L</sub>	-0.5	1.5	V
max. input HIGH voltage	V <sub>H</sub>	3.0	5.5	V
SCL clock frequency.	f <sub>SCL</sub>	0	400	KHz
Time the bus must be free before a new transmission can start.	t <sub>BUF</sub>	1.3	-	μs
Hold time start condition.After this period the first clock pulse is generated.	t <sub>HD:STA</sub>	0.6	-	μs
The LOW period of the clock	t <sub>LOW</sub>	1.3	-	μs
The HIGH period of the clock	t <sub>HIGH</sub>	0.6	-	μs
Set-up time for start condition.(Only relevant for a repeated Start condition.	t <sub>SU:STA</sub>	0.6	-	μs
Hold time DATA.	t <sub>HD:DAT</sub>	0	0.9	μs
Set-up time DATA	t <sub>SU:DAT</sub>	100	-	ns
Rise time both SDA and SCL lines.	t <sub>R</sub>	20+ 0.1Cb	300	ns
Fall time both SDA and SCL lines.	t <sub>F</sub>	20+ 0.1Cb	300	ns
Set-up time for stop condition	t <sub>SU:STO</sub>	0.6	-	μs



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(3) Pre - Amp Block sub address byte and data byte format

sub add.	function	bit	Data Byte (top:byte format under:start condition)							
			D7	D6	D5	D4	D3	D2	D1	D0
00H	Main contrast	8	A07	A06	A05	A04	A03	A02	A01	A00
			0	0	0	0	0	0	0	1
01H	Brightness control	8	A17	A16	A15	A14	A13	A12	A11	A10
			0	0	0	0	0	0	0	1
02H	Sub contrast R	8	A27	A26	A25	A24	A23	A22	A21	A20
			0	0	0	0	0	0	0	1
03H	Sub contrast G	8	A37	A36	A35	A34	A33	A32	A31	A30
			0	0	0	0	0	0	0	1
04H	Sub contrast B	8	A47	A46	A45	A44	A43	A42	A41	A40
			0	0	0	0	0	0	0	1
05H	OSD level	7	-	A56	A55	A54	A53	A52	A51	A50
			-	0	0	0	0	0	0	1
06H	D/A OUT1	8	A67	A66	A65	A64	A63	A62	A61	A60
			0	0	0	0	0	0	0	1
07H	D/A OUT2	8	A77	A76	A75	A74	A73	A72	A71	A70
			0	0	0	0	0	0	0	1
08H	D/A OUT3	8	A87	A86	A85	A84	A83	A82	A81	A80
			0	0	0	0	0	0	0	1
09H	D/A OUT4	8	A97	A96	A95	A94	A93	A92	A91	A90
			0	0	0	0	0	0	0	1
0AH	Sharpness control	4	-	-	-	-	AA3	AA2	AA1	AA0
			-	-	-	-	0	0	0	1
	Sync Sepa SW	1	-	-	-	AA4	-	-	-	-
			-	-	-	0	-	-	-	-
Video Det SW	1	-	-	AA5	-	-	-	-	-	
		-	-	0	-	-	-	-	-	
Test mode	2	AA7	AA6	-	-	-	-	-	-	
		0	0	-	-	-	-	-	-	

\*)pre-data

\*)subadd. 0AH

Sync Sepa SW AA4 0:Sync Sepa ON 1:Sync Sepa OFF

Video Det SW AA5 0:Video Det ON 1:Video Det OFF

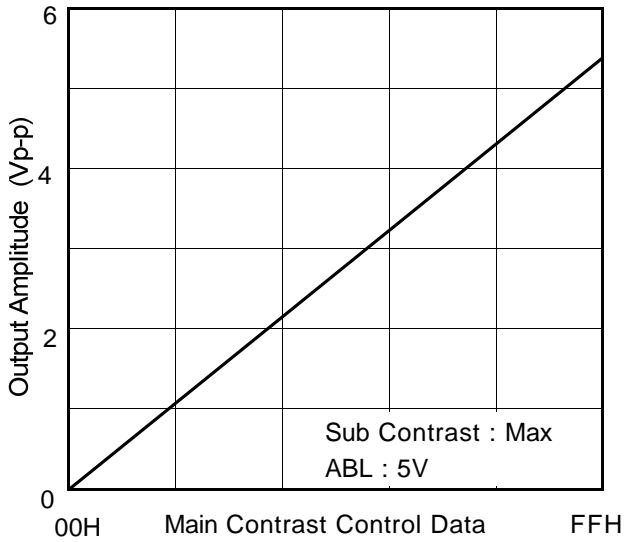
Always set up as AA6 and AA7 in 0

For IIC Data, please transfer in the period of Vertical.

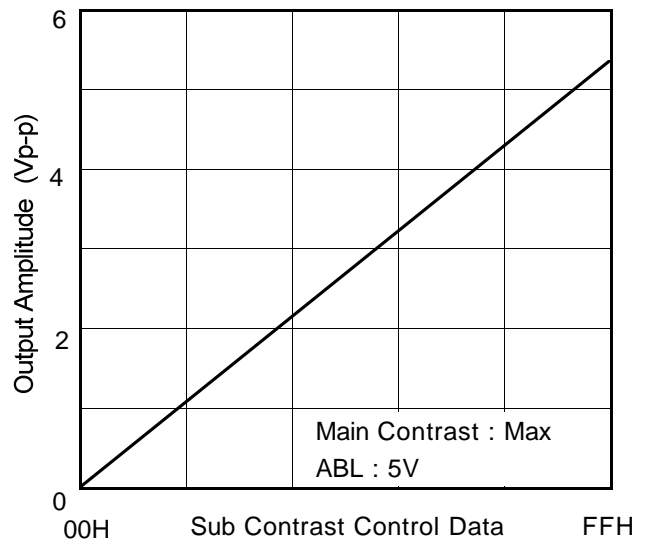
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**ELECTRICAL CHARACTERISTICS**

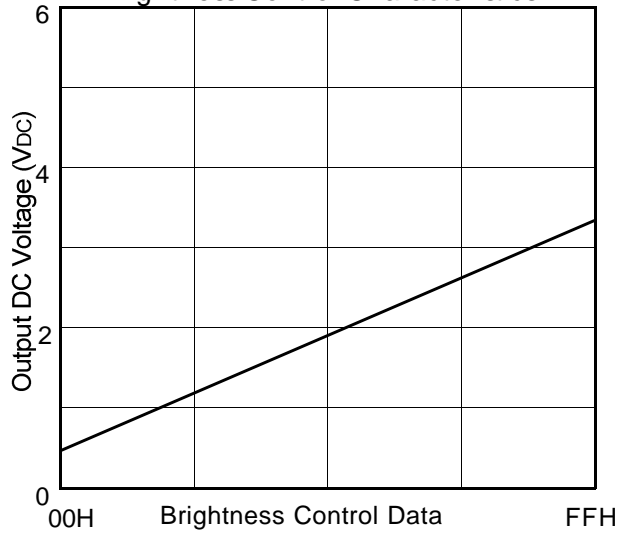
Main Contrast Control Characteristics



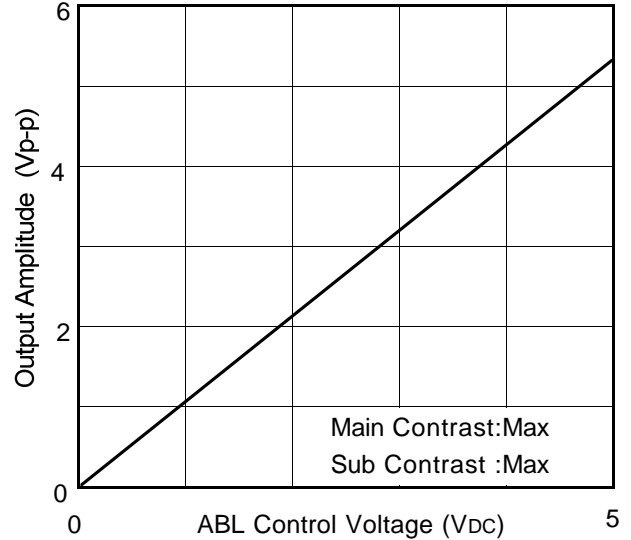
Sub Contrast Control Characteristics



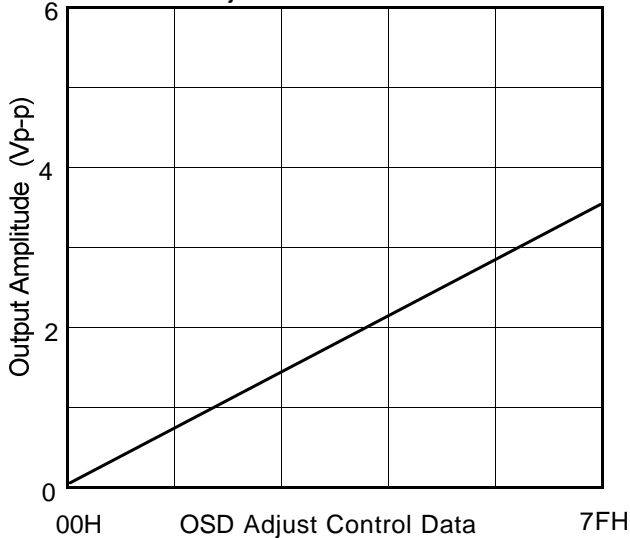
Brightness Control Characteristics



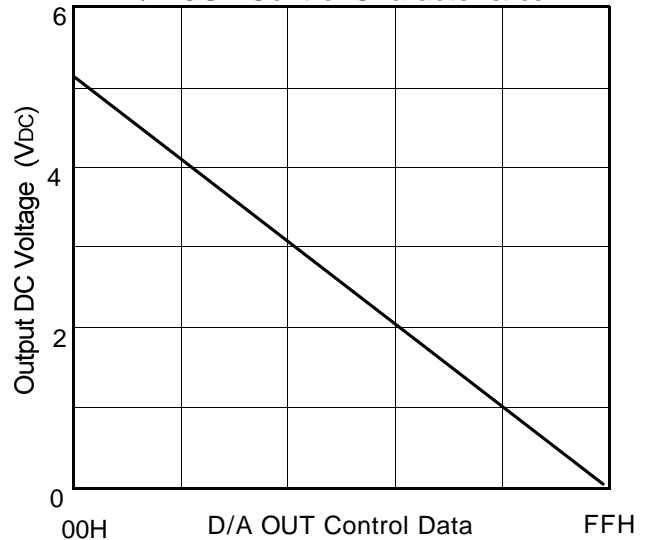
ABL Characteristics



OSD Adjust Control Characteristics



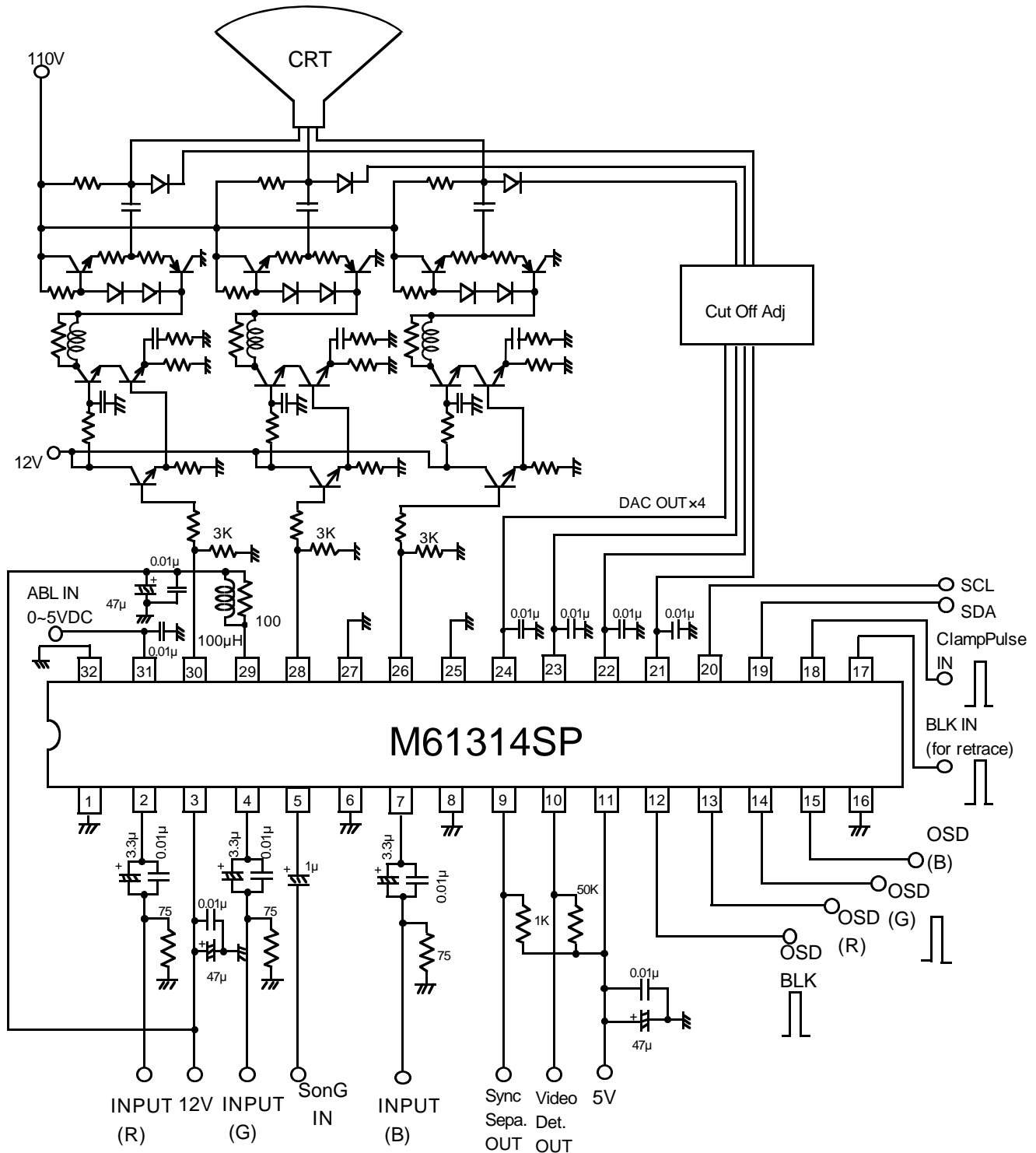
D/A OUT Control Characteristics



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## APPLICATION EXAMPLE



"Purchase of Mitsubishi electric corporation's I<sup>2</sup>C components conveys a licence under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms the I<sup>2</sup>C Standard Specification as defined by Philips"



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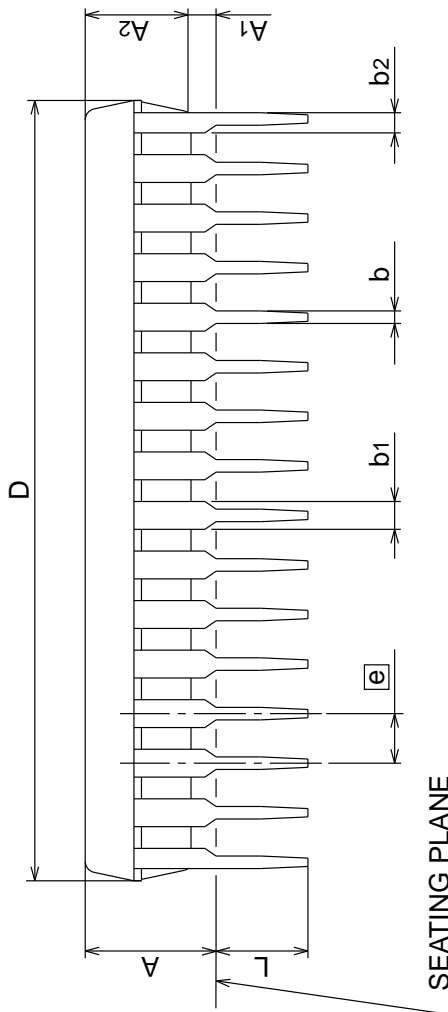
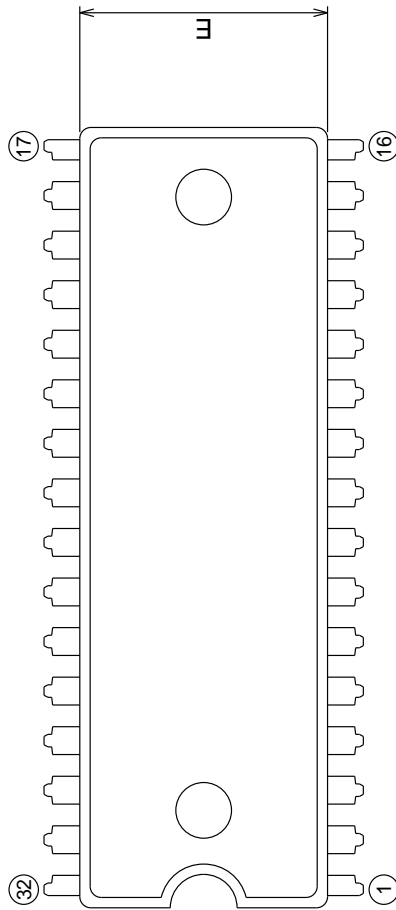
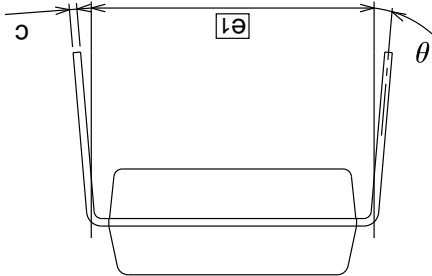
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**DETAILED DIAGRAM OF PACKAGE OUTLINE**

**Plastic 32pin 400mil SDIP**

**32P4B**

EIAJ Package Code SDIP32-P-400-1.78	JEDEC Code -	Weight(g) 2.2	Lead Material Alloy 42/Cu Alloy
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Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	5.08
A1	0.51	-	-
A2	-	3.8	-
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	-	1.778	-
e1	-	10.16	-
L	3.0	-	-
theta	0°	-	15°

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