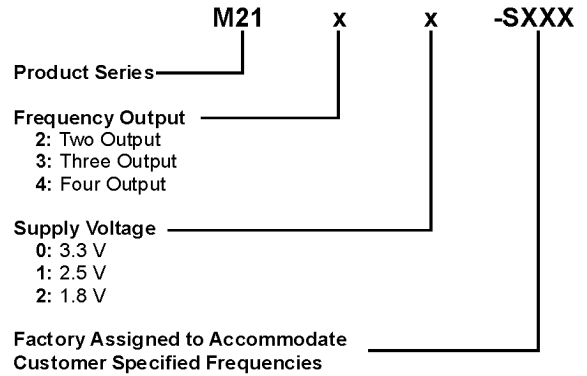


# M21x Series Multiple Frequency Clock Oscillator

## 5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/HCMOS Output



### Product Definition

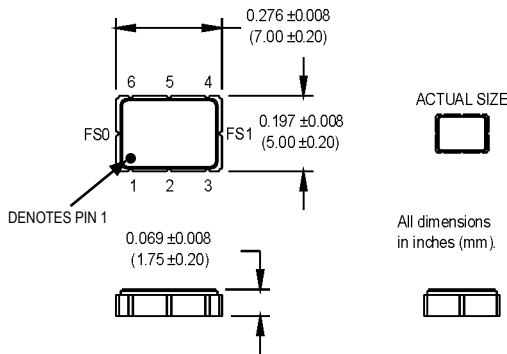


### Features:

- Multiple Output Frequencies (2, 3, or 4) - Selectable
- **QiK Chip™** Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 50 MHz - 1.4 GHz (LVDS/LVPECL/CML) and 10 - 150 MHz (CMOS)

### Phase Lock Loop Applications:

- Where more than one selectable frequency is required for different global regions, FEC (Forward Error Correction) or selectable functionality are required.
- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications



All dimensions in inches (mm).

### PIN 1 ENABLE

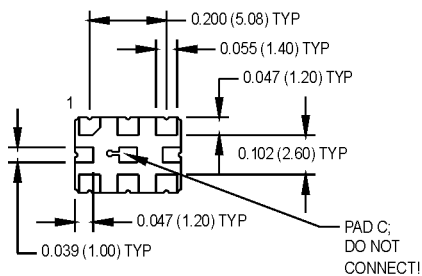
- Pad1: Enable/Disable or Tristate
- Pad2: N/C
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML, HCMOS)
- Pad5: Output  $\bar{Q}$  (LVPECL, LVDS, CML) N/C for HCMOS
- Pad6: Vcc
- PadA: FS0
- PadB: FS1
- PadC: Do not connect!

### PIN 2 ENABLE

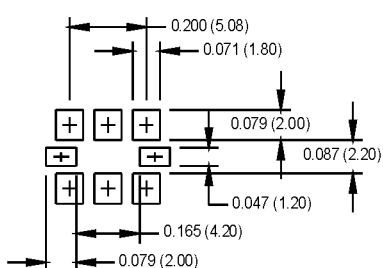
- Pad1: N/C
- Pad2: Enable/Disable or Tristate
- Pad3: Ground
- Pad4: Output Q (LVPECL, LVDS, CML, HCMOS)
- Pad5: Output  $\bar{Q}$  (LVPECL, LVDS, CML) N/C for HCMOS
- Pad6: Vcc
- PadA: FS0
- PadB: FS1
- PadC: Do not connect!

Frequency Select Truth Table		
	FS1	FS0
Frequency 1	High	High
Frequency 2	High	Low
Frequency 3	Low	High
Frequency 4	Low	Low

NOTE: Logic Low = 20% Vcc max.  
Logic High = 80% Vcc min.



### SUGGESTED SOLDER PAD LAYOUT

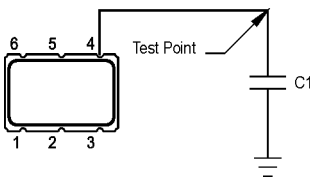


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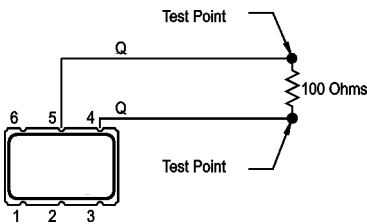
Please see [www.mtronpti.com](http://www.mtronpti.com) for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.

# M21x Series Multiple Frequency Clock Oscillator

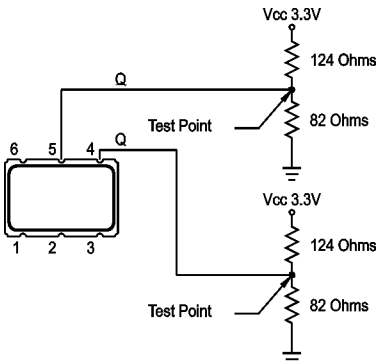
## 5x7 mm, 3.3/2.5/1.8 Volt, LVPECL/LVDS/CML/HCMOS Output



HCMOS Load Circuit



LVDS Load Circuit



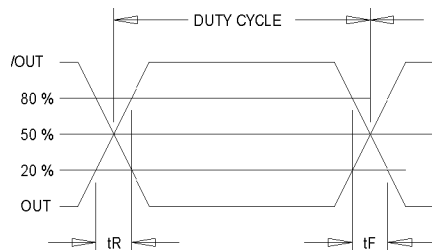
3.3V LVPECL Load Circuit

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	50 10		1400 150	MHz	PECL/LVDS/CML - See Note 1 CMOS
Operating Temperature	T <sub>A</sub>		-20 to +70 -40 to +85		°C °C	
Storage Temperature	T <sub>S</sub>	-55		+125	°C	
Frequency Stability	ΔF/F		±25 or ±50		ppm	See Note 2
Aging						
1st Year		-3		+3	ppm	
Thereafter (per year)		-1		+1	ppm	
Supply Voltage	V <sub>CC</sub>	1.71 2.375 3.135	1.8 2.5 3.3	1.89 2.625 3.465	V V V	
Input Current	I <sub>CC</sub>			125 105	mA mA	LVPECL/CMOS/CML LVDS
Load		50 Ohms to (V <sub>CC</sub> - 2) V <sub>CC</sub> 100 Ohm differential load				See Note 3 LVPECL Waveform LVDS/CML Waveform CMOS Waveform
Symmetry (Duty Cycle)		45		55	%	@ 50% of waveform
Output Skew				10	ps	LVPECL
				20	ps	LVDS, CML
Differential Voltage		350	425 TBD	500	mV <sub>ppd</sub>	LVDS CML
Common Mode Output Voltage	V <sub>CM</sub>		1.2		V	LVDS
Logic "1" Level	V <sub>OH</sub>	V <sub>CC</sub> - 1.02			V	LVPECL HCMOS
		90% V <sub>DD</sub>				LVPECL HCMOS
Logic "0" Level	V <sub>OL</sub>			V <sub>CC</sub> - 1.63	V	LVPECL HCMOS
				10% V <sub>DD</sub>		HCMOS
Rise/Fall Time	T <sub>r</sub> /T <sub>f</sub>		0.23	0.35	ns	@ 20/80% LVPECL
				6.0	ns	Ref. 10%-90% V <sub>DD</sub> HCMOS
Enable Function		80% V <sub>CC</sub> min. or N/C: output active 20% V <sub>CC</sub> max: output disables to high-Z 20% V <sub>CC</sub> max: output active 80% V <sub>CC</sub> min: output disables to high-Z				Output Option B Output Option S
Frequency Selection		See Truth Table				
Settling Time				10	ms	To within ± 1 ppm of frequency
Tristate Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z				
Start up Time			10		ms	
Phase Jitter						
@ 622.08 MHz	φ <sub>J</sub>		0.50		ps RMS	LVPECL/LVDS/CML Integrated 12 kHz - 20 MHz
@ 125 MHz				1.0	ps RMS	HCMOS (12 kHz - 20 MHz)
<b>Environmental</b>						
<b>Mechanical Shock</b>	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)					
<b>Vibration</b>	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
<b>Hermeticity</b>	Per MIL-STD-202, Method 112, (1x10 <sup>9</sup> atm. cc/s of Helium)					
<b>Thermal Cycle</b>	Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)					
<b>Solderability</b>	Per EIAJ-STD-002					

Note 1: Contact factory for exact frequency availability over 945 MHz.

Note 2: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.

Note 3: See Load Circuit Diagram in this datasheet. Consult factory with nonstandard output load requirements.



Output Waveform: LVDS/CML/LVPECL

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# MtronPTI Lead Free Solder Profile

