

## DRAM

## 64 K x 16 DRAM FAST PAGE MODE

### FEATURES

- X16 organization
- FAST PAGE access mode
- 2  $\overline{\text{CAS}}$  Byte/Word Read/Write operation
- Single 5V ( $\pm 10\%$ ) power supply
- TTL-compatible inputs and outputs
- 256-cycle refresh in 4ms
- Refresh modes :  $\overline{\text{RAS}}$  only,  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  (CBR) and HIDDEN
- JEDEC standard pinout
- Key AC Parameter

	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>
-25	25	8	43	15
-30	30	9	55	20
-35	35	10	65	23
-40	40	11	75	25

### ORDERING INFORMATION - PACKAGE

40-pin 400mil SOJ  
44 / 40-pin 400mil TSOP (TypeII)

PRODUCT NO.	PACKING TYPE
M10B11664A-25J	SOJ
M10B11664A-30J	
M10B11664A-35J	
M10B11664A-40J	
M10B11664A-25T	TSOPII
M10B11664A-30T	
M10B11664A-35T	
M10B11664A-40T	

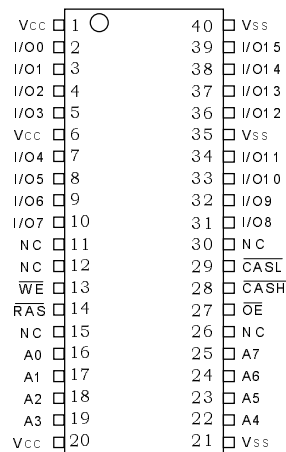
### GENERAL DESCRIPTION

The M10B11664A is a randomly accessed solid state memory, organized as 65,536 x 16 bits device. It offers Fast Page mode, 5V ( $\pm 10\%$ ) single power supply. Access time (-25,-30,-35,-40) and package type (SOJ, TSOP II) are optional features of this family. All these family have  $\overline{\text{CAS}}$  - before  $\overline{\text{RAS}}$ ,  $\overline{\text{RAS}}$  -only refresh and Hidden refresh capabilities.

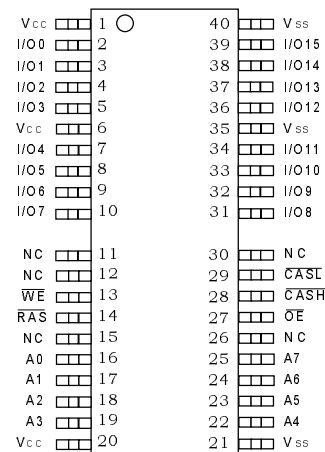
Two access modes are supported by this device : Byte access and Word access. Use only one of the two  $\overline{\text{CAS}}$  and leave the other staying high will result in a BYTE access. WORD access happens when two  $\overline{\text{CAS}}$  ( $\overline{\text{CASL}}$ ,  $\overline{\text{CASH}}$ ) are used.  $\overline{\text{CASL}}$  transiting low during READ or WRITE cycle will output or input data into the lower byte (IO0~IO7), and  $\overline{\text{CASH}}$  transiting low will output or input data into the upper byte (IO8~15).

### PIN ASSIGNMENT

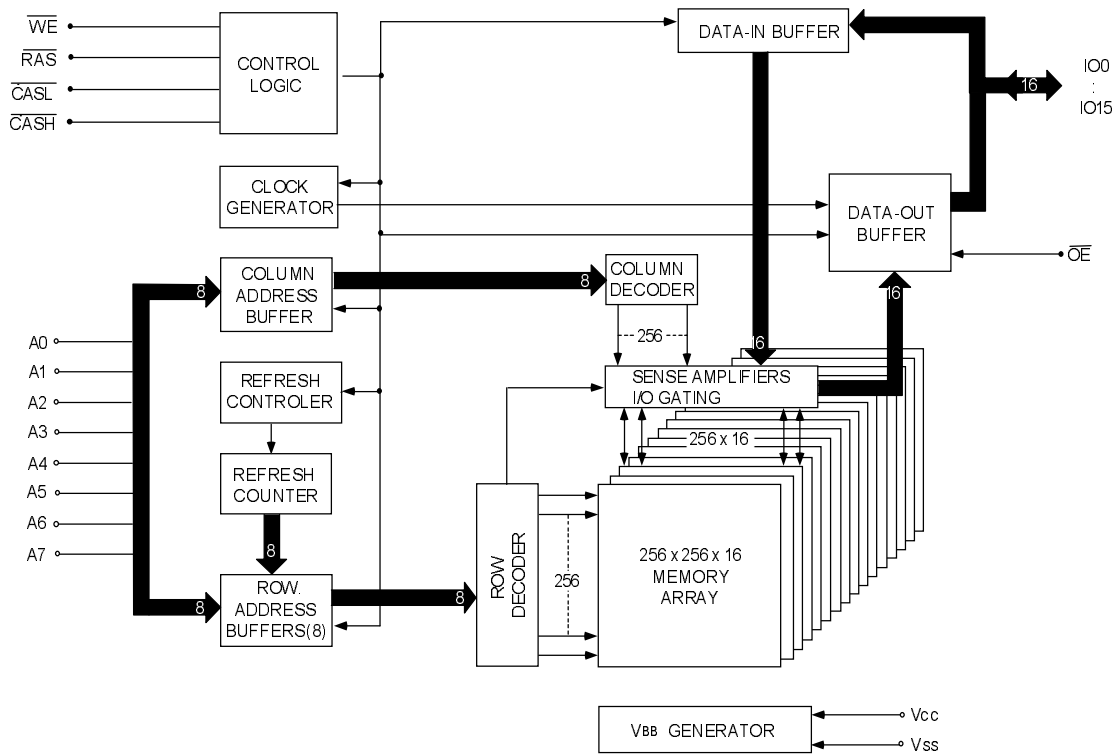
SOJ Top View



TSOP (TypeII) Top View



## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	DESCRIPTION
16~19, 22~25	A0~A7	Input	Address Input Row Address : A0~A7 Column Address : A0~A7
14	$\overline{\text{RAS}}$	Input	Row Address Strobe
28	$\overline{\text{CASH}}$	Input	Column Address Strobe / Upper Byte Control
29	$\overline{\text{CASL}}$	Input	Column Address Strobe / Lower Byte Control
13	$\overline{\text{WE}}$	Input	Write Enable
27	$\overline{\text{OE}}$	Input	Output Enable
2~5, 7~10, 31~34, 36~39	I/O0 ~ I/O15	Input / Output	Data Input / Output
1, 6, 20	Vcc	Supply	Power, 5V
21, 35, 40	Vss	Ground	Ground
11, 12, 15, 30	NC	-	No Connect

## ABSOLUTE MAXIMUM RATINGS

Voltage on Any pin Relative to V<sub>SS</sub> .....-1V to +7V  
 Operating Temperature, T<sub>A</sub> (ambient) ....0 °C to +70 °C  
 Storage Temperature (plastic) .....-55 °C to +150 °C  
 Power Dissipation ..... 1.0W  
 Short Circuit Output Current .....50mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation of the device above those conditions indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED

**OPERATING CONDITIONS** (0 °C ≤ T<sub>A</sub> ≤ 70 °C ; V<sub>CC</sub> = 5V ± 10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V <sub>CC</sub>	4.5	5.5	V	1
Supply Voltage		V <sub>SS</sub>	0	0	V	
Input High (Logic)Voltage		V <sub>IH</sub>	2.4	V <sub>CC</sub> + 1	V	1
Input Low (Logic)Voltage		V <sub>IL</sub>	-1.0	0.8	V	1
Input Leakage Current	0V ≤ V <sub>IH</sub> ≤ 7V	I <sub>LI</sub>	-10	10	μA	
Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ 7V Output(s) disable	I <sub>LO</sub>	-10	10	μA	
Output High Voltage	I <sub>OH</sub> = -5 mA	V <sub>OH</sub>	2.4	-	V	
Output Low Voltage	I <sub>OL</sub> = 4.2 mA	V <sub>OL</sub>	-	0.4	V	

Note : 1.All Voltages referenced to V<sub>SS</sub>

DESCRIPTION	CONDITIONS	SYMBOL	MAX				UNITS	NOTES
			-25	-30	-35	-40		
Operating Current	$\overline{RAS}$ , $\overline{CAS}$ cycling, t <sub>RC</sub> = min	I <sub>CC1</sub>	170	150	130	120	mA	1,2
Standby Current	TTL interface, $\overline{RAS}$ , $\overline{CAS}$ = V <sub>IH</sub> , D <sub>OUT</sub> = High-Z	I <sub>CC2</sub>	4	4	4	4	mA	
	CMOS interface, $\overline{RAS}$ , $\overline{CAS}$ > V <sub>CC</sub> -0.2V		2	2	2	2	mA	
$\overline{RAS}$ only refresh Current	t <sub>RC</sub> = min	I <sub>CC3</sub>	170	150	130	120	mA	2
FAST Page Mode Current	t <sub>PC</sub> = min	I <sub>CC4</sub>	170	150	130	120	mA	1,3
Standby Current	$\overline{RAS}$ = V <sub>IH</sub> , $\overline{CAS}$ = V <sub>IL</sub>	I <sub>CC5</sub>	5	5	5	5	mA	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	t <sub>RC</sub> = min	I <sub>CC6</sub>	170	150	130	120	mA	

Note : 1. ICC max is specified at the output open condition.

2. Address can be changed twice or less while  $\overline{RAS}$  = V<sub>IL</sub>.
3. Address can be changed once or less while  $\overline{CAS}$  = V<sub>IH</sub>.

## CAPACITANCE

(Ta = 25 °C , Vcc = 5V ± 10%)

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input Capacitance (address)	C <sub>i1</sub>	-	5	pF
Input Capacitance (RAS, CASH, CASL, WE, OE)	C <sub>i2</sub>	-	7	pF
Output capacitance (I/O0~I/O15)	C <sub>i/o</sub>	-	10	pF

## AC ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C , Vcc = 5V ± 10%, Vss = 0V) (note 14)

## Test Conditions

Input timing reference levels : 0V, 3V

Output reference level : Vol= 0.8V, Voh=2.0V

Output Load : 2TTL gate + CL (50pF)

Assumed tr = 2ns

PARAMETER	SYMBOL	-25		-30		-35		-40		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	trc	43		55		65		75		ns	
Read Write Cycle Time	trwc	65		85		95		105		ns	
Fast-Page-Mode Read or Write Cycle Time	tpc	15		20		23		25		ns	22
Fast-Page-Mode Read-Write Cycle Time	tpcm	37		42		49		52		ns	22
Access Time From RAS	trac		25		30		35		40	ns	4
Access Time From CAS	tcac		8		9		10		11	ns	5, 20
Access Time From OE	toac		8		9		10		11	ns	13, 20
Access Time From Column Address	t <sub>aa</sub>		12		16		18		20	ns	
Access Time From CAS Precharge	t <sub>acp</sub>		14		18		20		22	ns	20
RAS Pulse Width	tr <sub>as</sub>	25	10,000	30	10,000	35	10,000	40	10,000	ns	
RAS Pulse Width (Fast Page Mode)	tr <sub>asc</sub>	25	10,000	30	100,000	35	100,000	40	100,000	ns	
RAS Hold Time	tr <sub>sh</sub>	8		9		10		11		ns	24
RAS Precharge Time	tr <sub>p</sub>	15		20		23		25		ns	
CAS Pulse Width	tr <sub>cas</sub>	4	10,000	9	10,000	10	10,000	11	10,000	ns	
CAS Hold Time	tr <sub>cas</sub>	21		30		35		40		ns	19
CAS Precharge Time	tr <sub>cp</sub>	4		5		6		7		ns	23
RAS to CAS Delay Time	tr <sub>cd</sub>	10	17	10	21	10	25	10	29	ns	7, 18
CAS to RAS Precharge Time	tr <sub>crp</sub>	5		5		5		5		ns	19
Row Address Setup Time	tr <sub>asr</sub>	0		0		0		0		ns	
Row Address Hold Time	tr <sub>ah</sub>	5		5		5		5		ns	
RAS to Column Address Delay Time	tr <sub>ad</sub>	8	13	8	14	8	17	8	20	ns	8
Column Address Setup Time	tr <sub>asc</sub>	0		0		0		0		ns	18
Column Address Hold Time	tr <sub>cah</sub>	5		5		5		5		ns	18
Column Address Hold Time (Reference to RAS)	tr <sub>ar</sub>	22		26		30		34		ns	
Column Address to RAS Lead Time	tr <sub>al</sub>	12		16		18		20		ns	

(Continued)

PARAMETER	SYMBOL	-25		-30		-35		-40		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read Command Setup Time	t <sub>RCS</sub>	0		0		0		0		ns	15,18
Read Command Hold Time Reference to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0		0		0		0		ns	9,15,19
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0		0		0		0		ns	9
$\overline{\text{RAS}}$ to Output in Low-Z	t <sub>CLZ</sub>	3		3		3		3		ns	20
Output Buffer Turn-off Delay From $\overline{\text{RAS}}$	t <sub>OFF1</sub>	3	15	3	15	3	15	3	15	ns	10,17,20
Output Buffer Turn-off to $\overline{\text{OE}}$	t <sub>OFF2</sub>		6		8		8		8	ns	17,25
Write Command Setup Time	t <sub>WCS</sub>	0		0		0		0		ns	11,15,18
Write Command Hold Time	t <sub>WCH</sub>	5		5		5		5		ns	15,24
Write Command Hold Time(Reference to $\overline{\text{RAS}}$ )	t <sub>WCR</sub>	22		26		30		34		ns	15
Write Command Pulse Width	t <sub>WP</sub>	5		5		5		5		ns	15
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	7		8		9		10		ns	15
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	5		6		7		8		ns	15,19
Data-in Setup Time	t <sub>DS</sub>	0		0		0		0		ns	12,20
Data-in Hold Time	t <sub>DH</sub>	5		5		5		5		ns	12,20
Data-in Hold Time (Reference to $\overline{\text{RAS}}$ )	t <sub>DHR</sub>	22		26		30		34		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	34		46		51		56		ns	11
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	21		32		34		36		ns	11
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	17		25		26		27		ns	11,18
Transition Time (rise or fall)	t <sub>tr</sub>	1.5	50	1.5	50	2.5	50	2.5	50	ns	2,3
Refresh Period (256 cycles)	t <sub>REF</sub>		4		4		4		4	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	t <sub>RPC</sub>	10		10		10		10		ns	
$\overline{\text{CAS}}$ Setup Time(CBR REFRESH)	t <sub>CSR</sub>	5		10		10		10		ns	1,18
$\overline{\text{CAS}}$ Hold Time(CBR REFRESH)	t <sub>CHR</sub>	7		10		10		10		ns	1,19
$\overline{\text{OE}}$ Hold Time From $\overline{\text{WE}}$ During Read-Modify-Write Cycle	t <sub>OEH</sub>	4		4		4		5		ns	16
$\overline{\text{OE}}$ Setup Prior to $\overline{\text{RAS}}$ During Hidden Refresh Cycle	t <sub>ORD</sub>	0		0		0		0		ns	
Last $\overline{\text{CAS}}$ Going Low to First $\overline{\text{CAS}}$ Returning High	t <sub>CLCH</sub>	4		9		10		11		ns	21
Read Setup Time Reference to $\overline{\text{RAS}}$ in CBR	t <sub>RSR</sub>	5		5		5		5		ns	
Read Hold Time Reference to $\overline{\text{RAS}}$ in CBR	t <sub>RHR</sub>	5		5		5		5		ns	

## Notes :

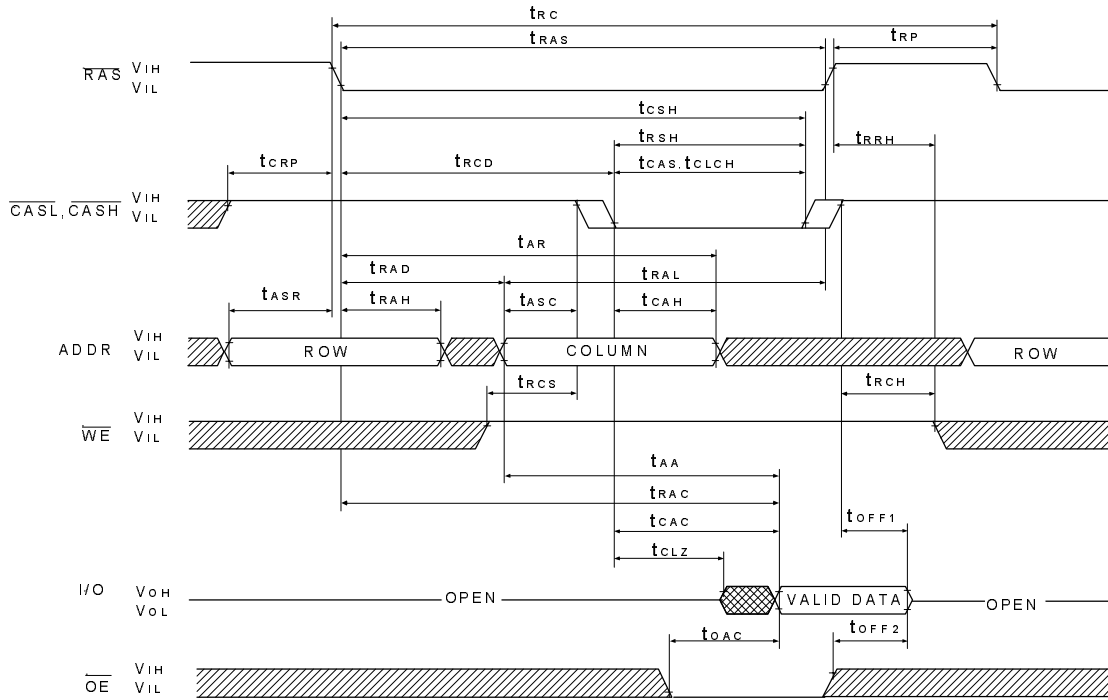
1. Enables on-chip refresh and address counters.
2.  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
3. In addition to meet the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  in a monotonic manner.
4. Assume that  $t_{RCD} < t_{RCD(max)}$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
5. Assume that  $t_{RCD} \geq t_{RCD(max)}$
6. If  $\overline{RAS}$  is low at the falling edge of  $\overline{RAS}$ , data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer,  $\overline{CAS}$  must be pulsed high.
7. Operation within the  $t_{RCD}$  limit ensures that  $t_{RCD(max)}$  can be met,  $t_{RCD(max)}$  is specified as a reference point only ; if  $t_{RCD}$  is greater than the specified  $t_{RCD(max)}$  limit, access time is controlled by  $t_{CAC}$ .
8. Operation within the  $t_{RAD}$  limit ensures that  $t_{RAD(max)}$  can be met.  $t_{RAD(max)}$  is specified as a reference point only ; if  $t_{RAD}$  is greater than the specified  $t_{RAD(max)}$  limit, access time is controlled by  $t_{AA}$ .
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
10.  $t_{OFF1(max)}$  defines the time at which the output achieves the open circuit condition ; it is not a reference to  $V_{OH}$  or  $V_{OL}$ .
11.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If  $t_{WCS} \geq t_{WCS(min)}$ , the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{RWD} \geq t_{RWD(min)}$ ,  $t_{AWD} \geq t_{AWD(min)}$  and  $t_{CWD} \geq t_{CWD(min)}$ , the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\overline{CAS}$  and  $\overline{RAS}$  or  $\overline{OE}$  go back to  $V_{IH}$ ) is indeterminate.  $\overline{OE}$  held high and  $\overline{WE}$  taken low after  $\overline{CAS}$  goes low result in a LATE WRITE ( $\overline{OE}$ -controlled) cycle.
12. Those parameters are referenced to  $\overline{CAS}$  leading edge in EARLY WRITE cycles and  $\overline{WE}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
13. During a READ cycle, if  $\overline{OE}$  is low then taken HIGH before  $\overline{CAS}$  goes high, I/O goes open, if  $\overline{OE}$  is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of 200  $\mu s$  is required after power-up followed by eight  $\overline{RAS}$  refresh cycles ( $\overline{RAS}$  only or CBR) before proper device operation is assured. The eight  $\overline{RAS}$  cycle wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
15. WRITE command is defined as  $\overline{WE}$  going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OFF2}$  and  $t_{OEH}$  met ( $\overline{OE}$  high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once  $t_{OFF1}$  or  $t_{OFF2}$  occur.
18. Referenced to the earlier  $\overline{CAS}$  falling edge.
19. Referenced to the latter  $\overline{CAS}$  rising edge.
20. Output parameter (I/O) is referenced to corresponding  $\overline{CAS}$  input, IO0~7 by  $\overline{CASL}$  and IO8~15 by  $\overline{CASH}$ .
21. Last falling  $\overline{CAS}$  edge to first rising  $\overline{CAS}$  edge.
22. Last rising  $\overline{CAS}$  edge to next cycle's last rising  $\overline{CAS}$  edge.
23. Last rising  $\overline{CAS}$  edge to first falling  $\overline{CAS}$  edge.
24. Referenced to the latter  $\overline{CAS}$  falling edge.
25. All IOs controlled by  $\overline{OE}$ , regardless  $\overline{CASL}$  and  $\overline{CASH}$ .

## Truth Table

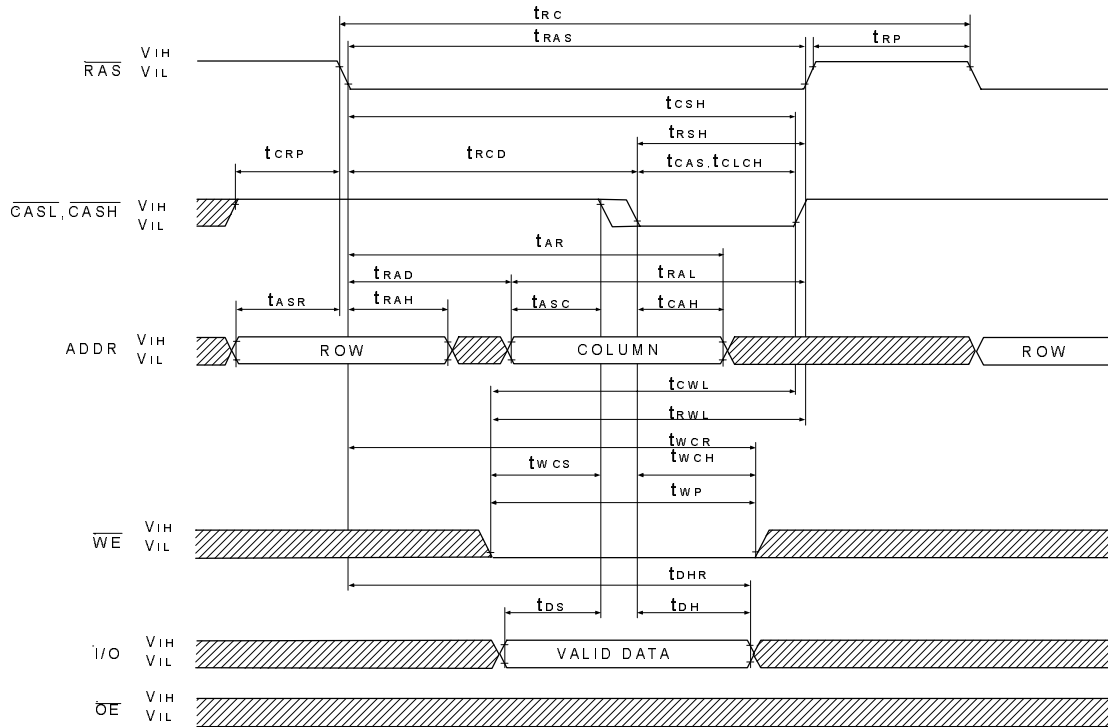
FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES		DQs	NOTES
							tr	tc		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
Read : Word		L	L	L	H	L	ROW	COL	Data-Out	
Read : Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, Data-Out	
Read : Upper Byte		L	H	L	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, Data-Out	
Write : Word (Early Write)		L	L	L	L	X	ROW	COL	Data-In	
Write : Lower Byte (Early)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
Write : Upper Byte (Early)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
Read-Write		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
Fast-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L		COL	Data-Out	2
Fast-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X		COL	Data-In	1
Fast-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H		COL	Data-Out, Data-In	1, 2
Hidden Refresh		L→H→L	L	L	H	L	ROW	COL	Data-Out	2
RAS -Only Refresh		L	H	H	X	X	ROW		High-Z	
CBR Refresh		H→L	L	L	H	X	X	X	High-Z	3

- \*Note : 1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).  
 2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).  
 3. Only one  $\overline{\text{CAS}}$  must be active ( $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$ ).

**READ CYCLE**



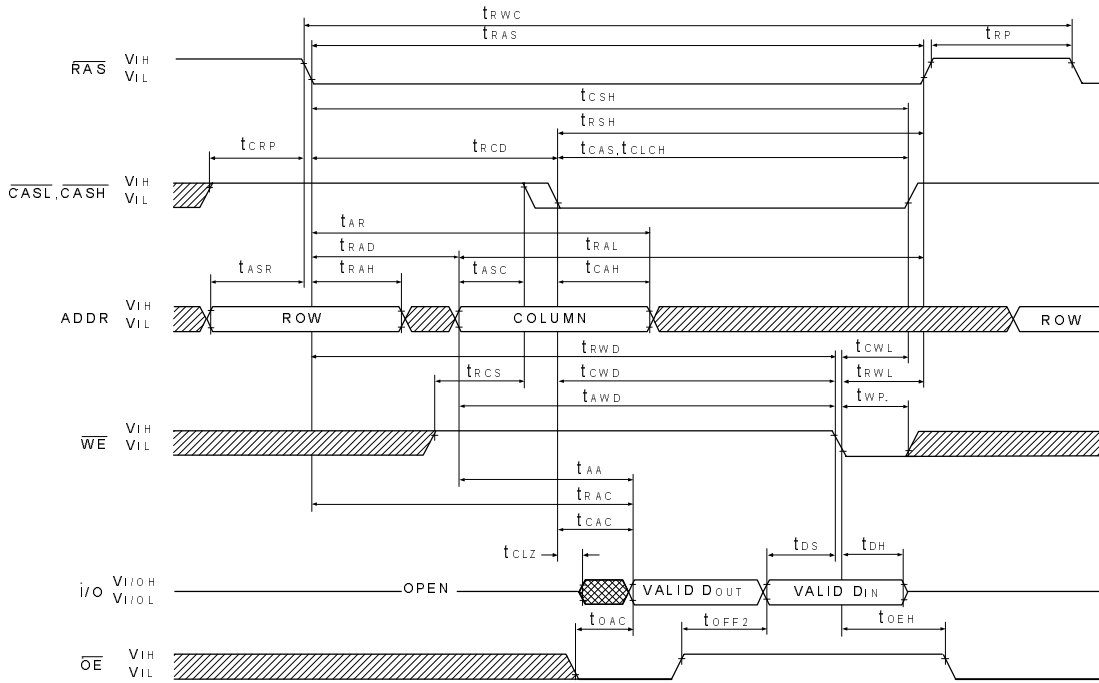
**EARLY WRITE CYCLE**



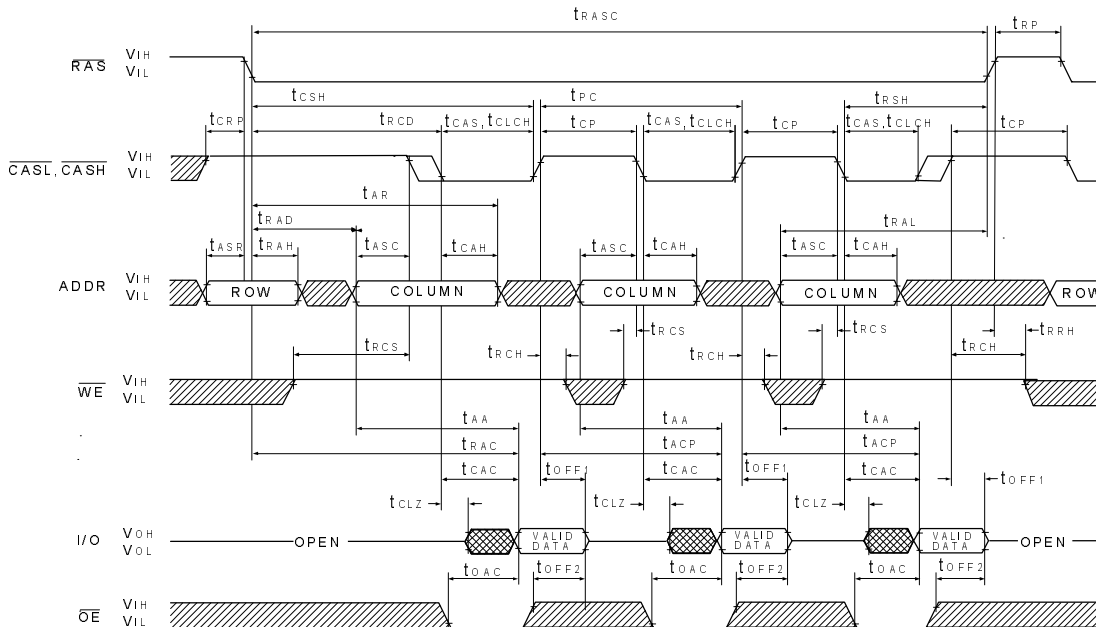
 DONT CARE  
 UNDEFINED



**READ WRITE CYCLE  
(LATE WRITE and READ-MODIFY-WRITE CYCLES)**

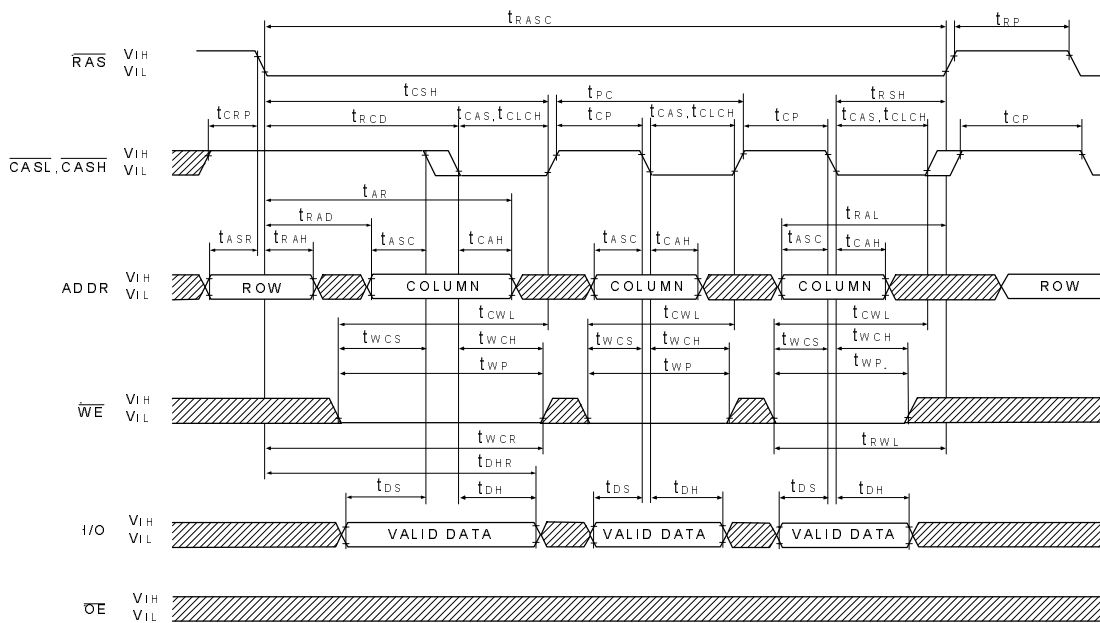


**FAST-PAGE-MODE READ CYCLE**

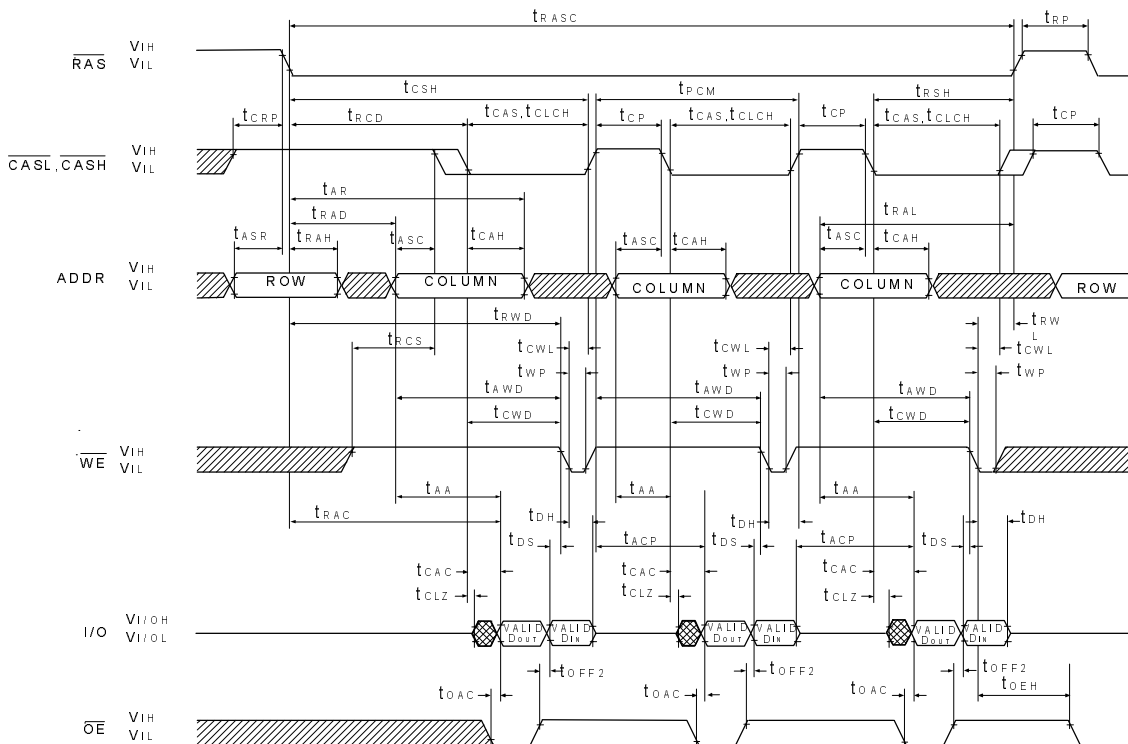


 DON'T CARE  
 UNDEFINED

**FAST-PAGE-MODE EARLY-WRITE CYCLE**

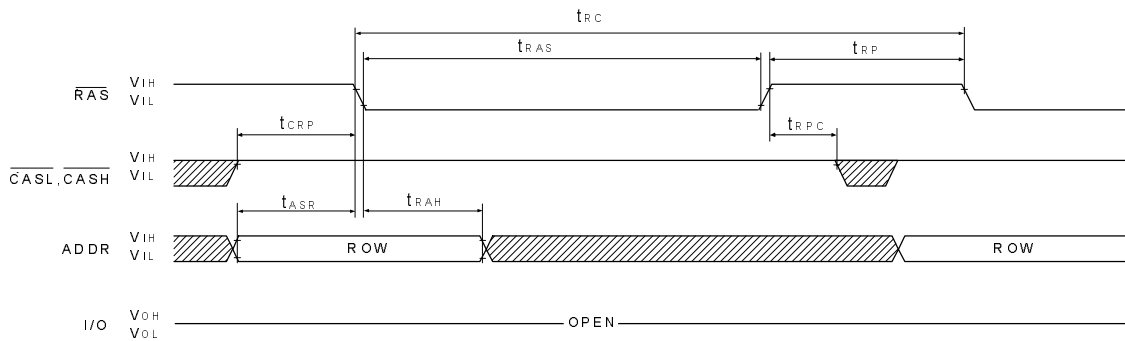


**FAST-PAGE-MODE READ-WRITE CYCLE  
(LATE WRITE and READ-MODIFY-WRITE CYCLES)**

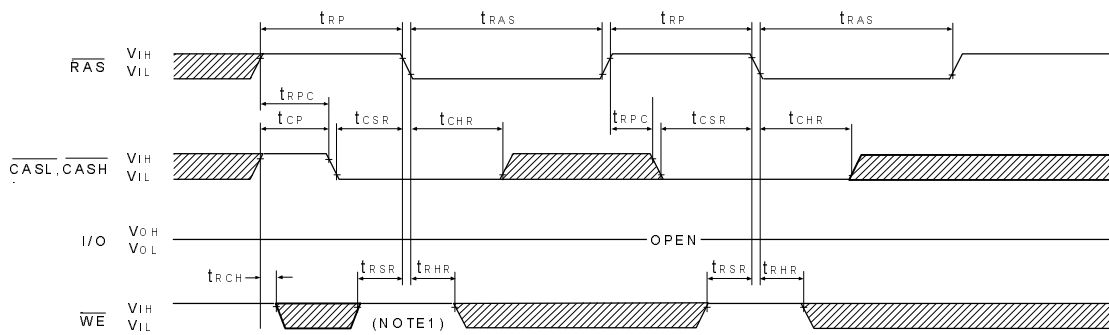


DON'T CARE  
 UNDEFINED

**RAS ONLY REFRESH CYCLE**  
**(ADDR = A0~A7 ;  $\overline{OE}$  ,  $\overline{WE}$  = DON'T CARE)**



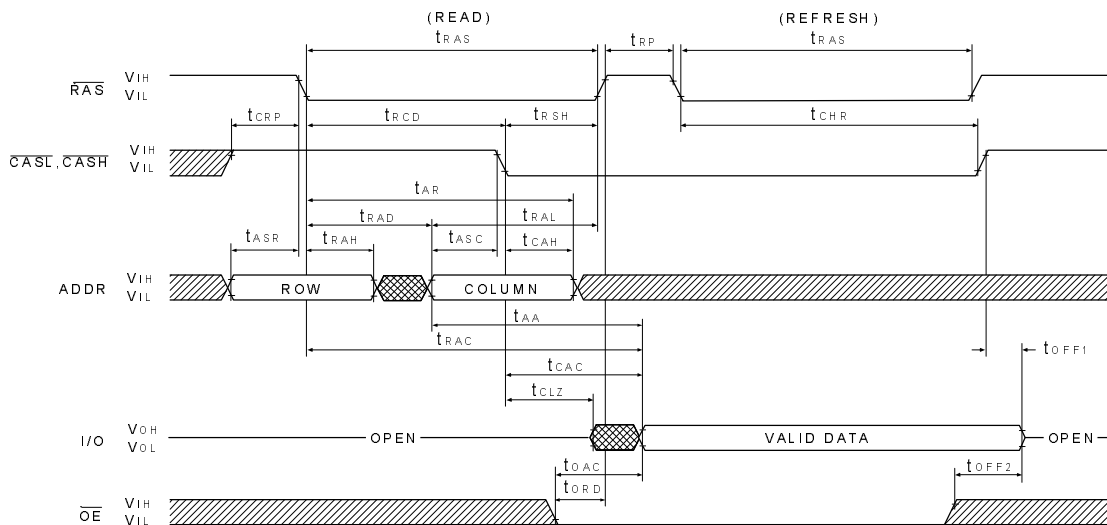
**CBR REFRESH CYCLE**  
**(A0~A7 ;  $\overline{OE}$  = DON'T CARE)**



▨ DON'T CARE  
 ▩ UNDEFINED

Note : 1.  $t_{RSR}$  and  $t_{RHR}$  are for system design reference only. The  $\overline{WE}$  signal is actually a "don't care" at  $\overline{RAS}$  time during a CBR REFRESH. However,  $\overline{WE}$  should be held HIGH at  $\overline{RAS}$  time during a CBR REFRESH to ensure compatibility with other DRAMs which require  $\overline{WE}$  HIGH at  $\overline{RAS}$  time during a CBR REFRESH.

**HIDDEN REFRESH CYCLE  
( $\overline{WE}$  = HIGH ;  $\overline{OE}$  = LOW)**

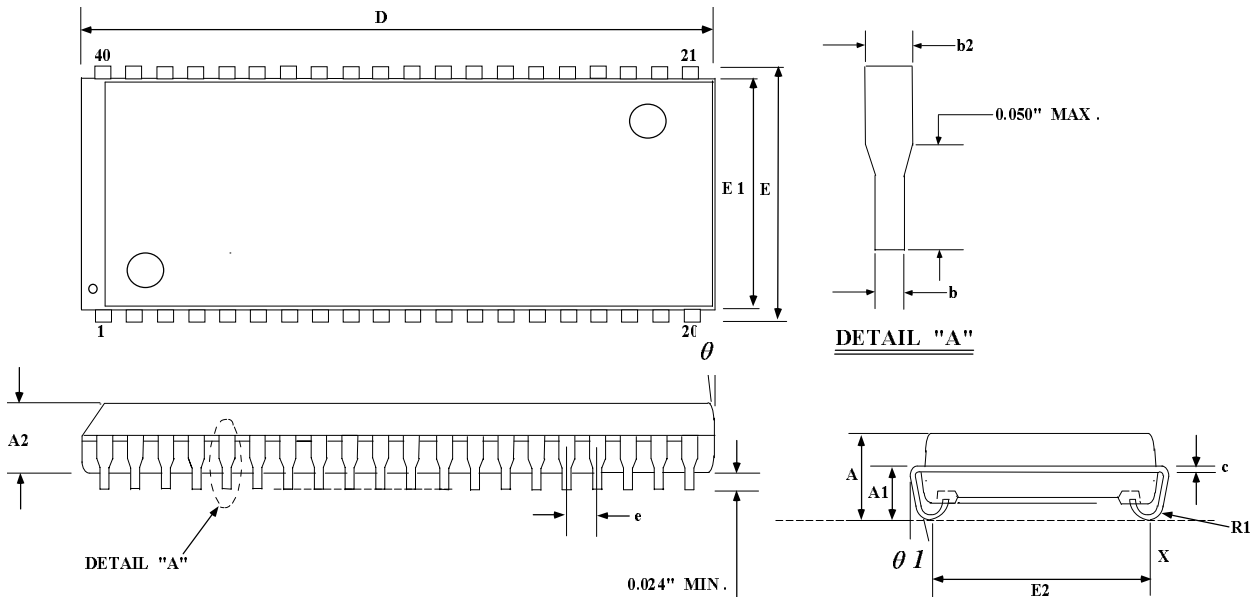


 DON'T CARE  
 UNDEFINED

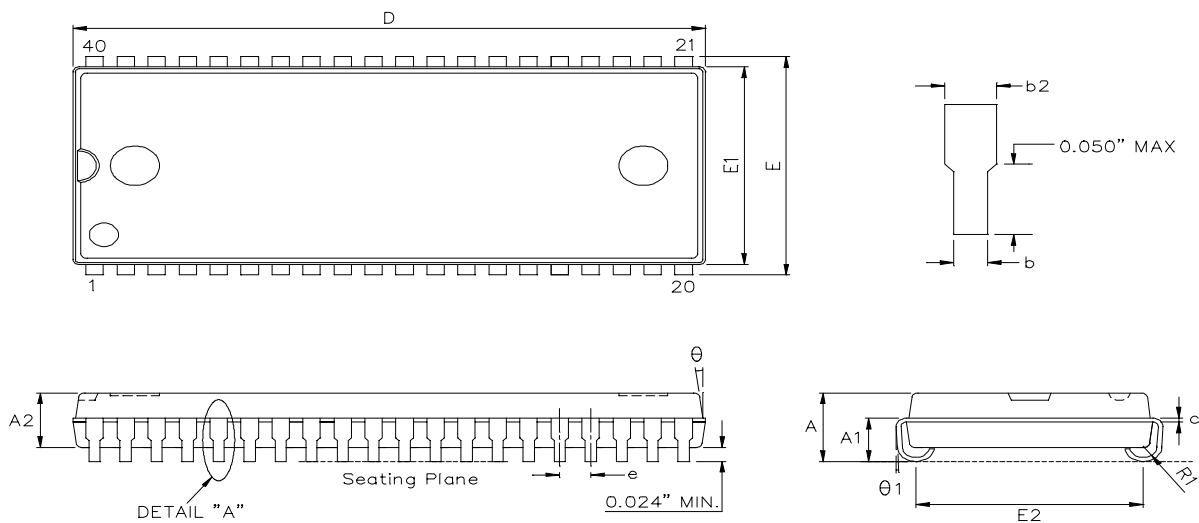
## PACKING DIMENSIONS

40-LEAD SOJ(400mil)

### SECTION I



### SECTION II



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	3.250	3.510	3.760	0.128	0.138	0.148	E	10.920	11.176	11.430	0.430	0.440	0.450
A1	2.080	___	___	0.082	___	___	E1	10.030	10.160	10.290	0.395	0.400	0.405
A2	2.790 REF			0.110 REF			E2	9.40 BSC			0.370 BSC		
b	0.380	0.460	0.560	0.015	0.018	0.022	R1	0.760	0.890	1.020	0.030	0.035	0.040
b2	0.635 REF			0.025 REF			b2	0.635 REF			0.025 REF		
c	0.180	0.250	0.360	0.007	0.010	0.014	$\theta 1$	0°	___	10°	0°	___	10°
e	1.270 BSC			0.050 BSC			e	1.270 BSC			0.050 BSC		
D	25.91	26.040	26.290	1.02	1.025	1.035	y1	___	___	0.381	___	___	0.015

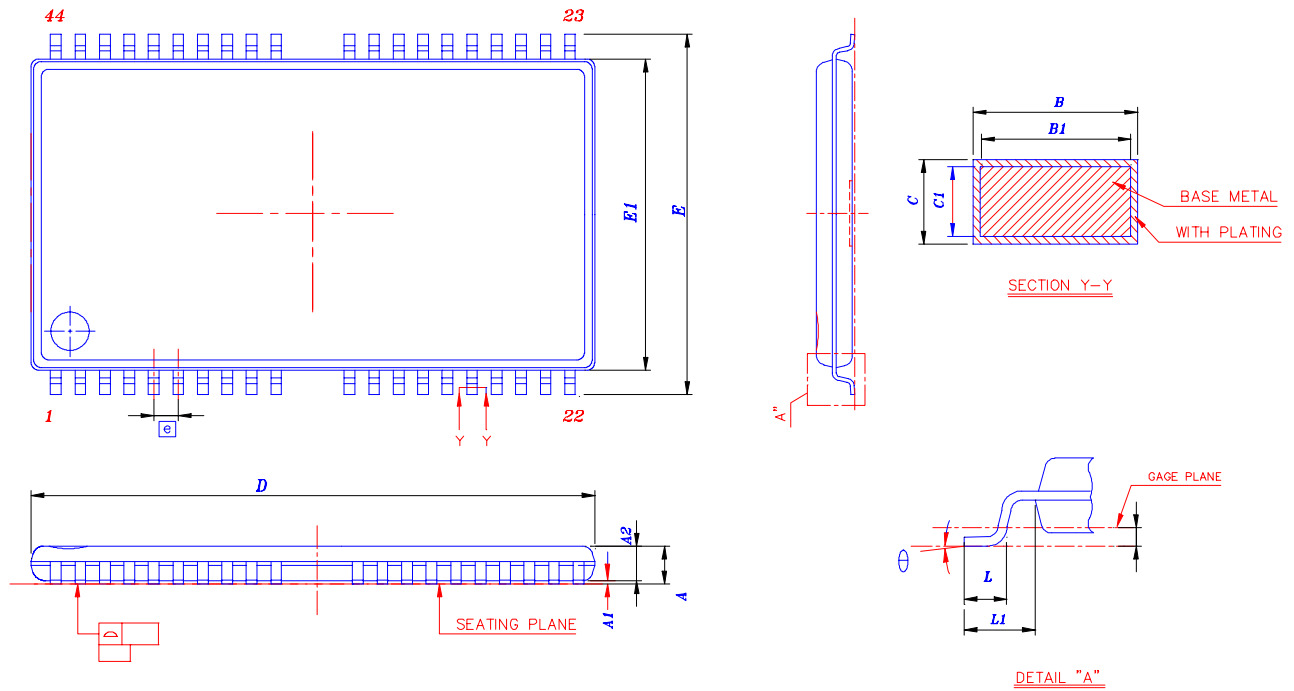
PACKING

DIMENSIONS

40 / 44-LEAD

TSOP(II)

DRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
b	0.30	—	0.45	0.012	—	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	—	0.21	0.005	—	0.008
c1	0.10	—	0.16	0.004	—	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	0° ~ 7° REF			0° ~ 7° REF		

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