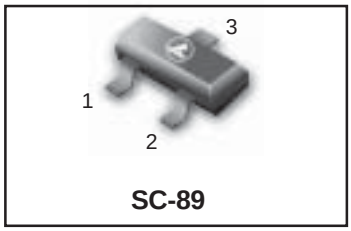
Bias Resistor Transistors

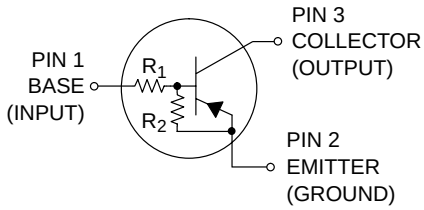
PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

LDTA143EET1



This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SC-89 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- Pb-Free Package is Available.



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, FR–4 Board (Note 1.) @ T_A = 25°C Derate above 25°C	P_D	 200 1.6	 mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1.)	$R_{\theta JA}$	600	°C/W
Total Device Dissipation, FR–4 Board (Note 2.) @ T_A = 25°C Derate above 25°C	P_D	 300 2.4	 mW mW/°C
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C

1. FR–4 @ Minimum Pad
2. FR–4 @ 1.0 × 1.0 Inch Pad

DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LDTA143EET1	6J	3000/Tape&Reel
LDTA143EET1G	6J (Pb-Free)	3000/Tape&Reel

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{BE} = 6.0 V)	I_{EBO}	–	–	1.5	mAdc
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS (Note 3)					
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	h_{FE}	15	27	–	
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 1 mA)	$V_{CE(sat)}$	–	–	0.25	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	–	–	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R_1	3.3	4.7	6.1	kΩ
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

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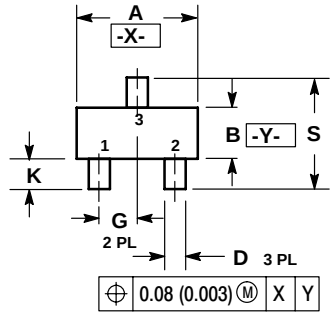
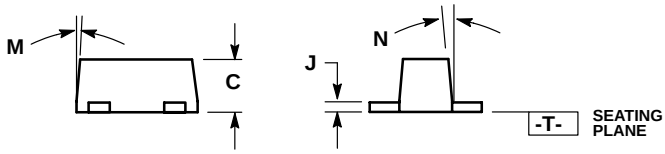
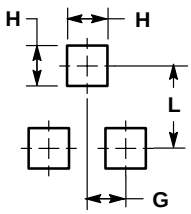
SC−89





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G		0.50 BSC			0.020 BSC	
H		0.53 REF			0.021 REF	
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L		1.10 REF			0.043 REF	
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



RECOMMENDED PATTERN OF SOLDER PADS