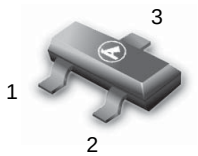
Digital transistors (built-in resistors)

LDTA123JET1



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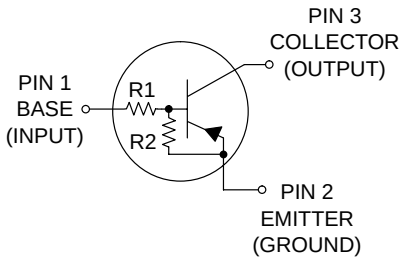
FEATURES:

1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
3) Only the on/off conditions need to be set for operation, making device design easy.

STRUCTURE:

PNP digital transistor
(Built-in resistor type)



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, FR–4 Board (Note 1.) @ T_A = 25°C Derate above 25°C	P_D	 200 1.6	 mW mW/°C
Thermal Resistance, Junction to Ambient (Note 1.)	$R_{\theta JA}$	600	°C/W
Total Device Dissipation, FR–4 Board (Note 2.) @ T_A = 25°C Derate above 25°C	P_D	 300 2.4	 mW mW/°C
Thermal Resistance, Junction to Ambient (Note 2.)	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C

1. FR–4 @ Minimum Pad
2. FR–4 @ 1.0 × 1.0 Inch Pad

DEVICE MARKING

LDTA123JET1=6M

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector–Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter–Base Cutoff Curren (V_{EB} = 6.0 V, I_C = 0)	I_{EBO}	–	–	0.5	mAdc
Collector–Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 3.) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS (Note 3.)					
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	h_{FE}	80	140	–	
Collector–Emitter Saturation Voltage (I_C = 10 mA, I_E = 0.3 mA)	$V_{CE(sat)}$	–	–	0.25	Vdc
Input Resistor	R1	1.54	2.2	2.86	kΩ
Resistor Ratio	R_1/R_2	0.038	0.047	0.056	

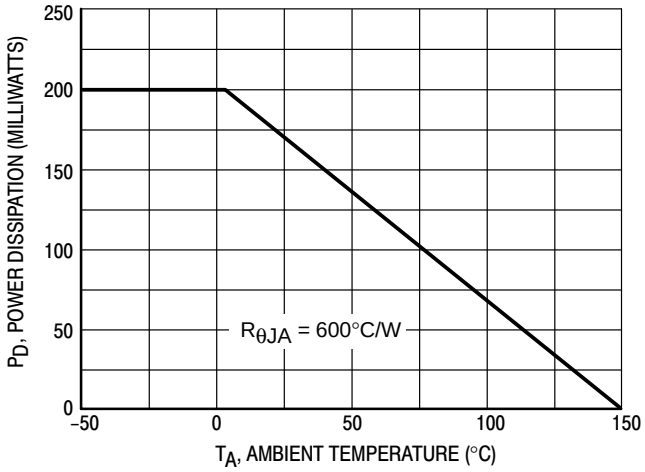


Figure 1. Derating Curve

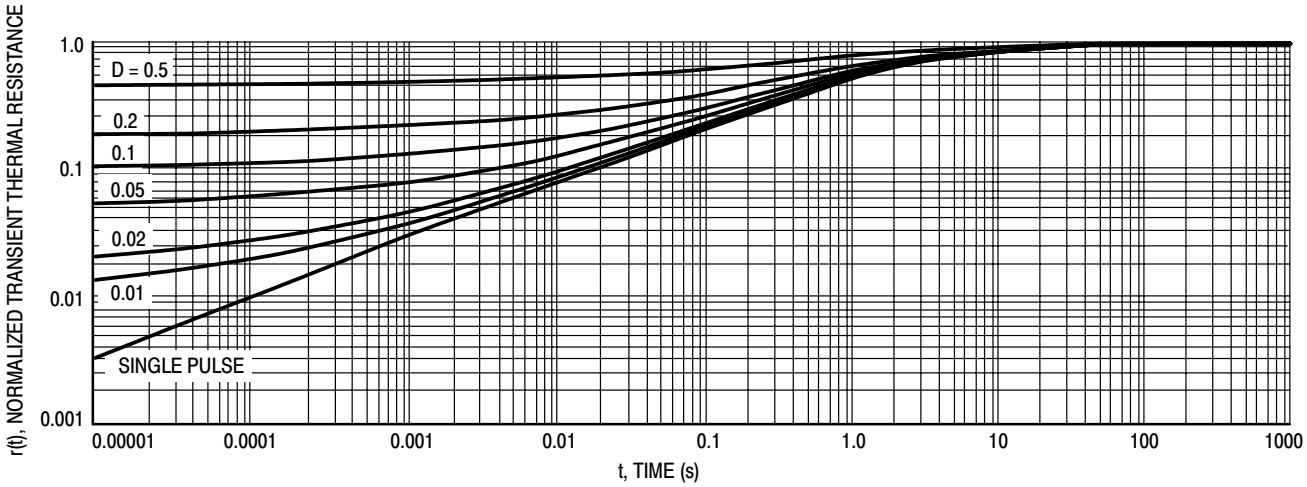


Figure 2. Normalized Thermal Response

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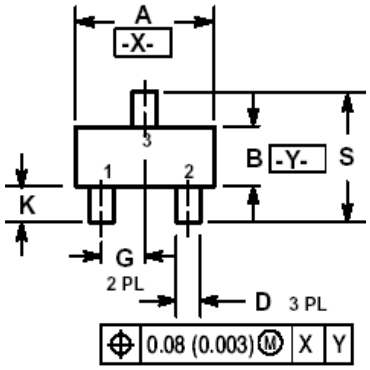
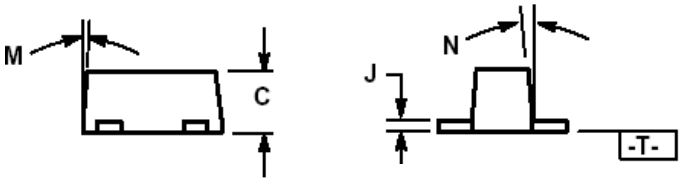


NOTES:
1.DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.CONTROLLING DIMENSION: MILLIMETERS
3.MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4.463C-01 OBSOLETE, NEW STANDARD 463C-02.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067