32Mb A-die DDR SRAM Specification

153FCBGA with Pb & Pb-Free

(RoHS compliant)

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Document Title

32M DDR SYNCHRONOUS SRAM

Revision History

Rev No.	History	Draft Data	Remark
Rev. 0.0	Initial document.	Dec. 2002	Advance
Rev. 0.1	Remove /G operation thru the Spec. - Remove /G from PUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION, TRUTH TABLE and TIMING WAVEFORMs Add 300MHz Speed bin. - Add Part ID at ORDERING INFORMATION & I_{DD30} at DC CHARACTERISTICS Change I_{LI} and I_{Lo} at DC CHARCATERISTICS - I_{LI} : MIN -1 -> -3, MAX 1 -> 3, I_{Lo} : MIN -1 -> -5, MAX 1 -> 5 Change the comment of Programmable Impedance Output Driver. Change RECOMMENDED DC OPERATING CONDITIONS. - V_{REF} : Min 0.68 -> 0.65, Max 1.0 -> 0.85 Change PIN CAPACITANCE : C_{IN} : 3 -> 3.1 Change AC TEST CONDITIONS : T_R/R_F: 0.4/0.4 -> 0.5/0.5 Change AC TIMING CHARACTERISTICS - t_{CHCL} : t_{KHKL} -0.1 -> t_{KHKL} -0.2 , t_{CLCH} : t_{KLKH} -0.1 -> t_{KLKH} -0.2 - t_{CXCV} : 2.10 -> 2.30	Jan. 2003	Advance
Rev 0.2	Change VDDQ RANGE - In FEATURES : 1.5V V_{DDQ} -> 1.5~.1.8V V_{DDQ} - In RECOMENDED DC OPERATING CONDITIONS : Max V_{DDQ} : 1.6 -> 1.9 Change TRUTH TABLE : Remove Clock Stop Change DC CHARACTERISTICS - x36 I_{DD} : I_{DD50} : 950 -> 1050, I_{DD45} : 850 -> 950, I_{DD40}: 800 -> 860, I_{DD30}: 750 -> 760 - x18 I_{DD}: I_{DD50} : 850 -> 1000, I_{DD45} : 800 -> 900, I_{DD40}: 750 -> 810, I_{DD30}: 700 -> 710 - I_{SB1} : 150 -> 200 Change PIN CAPACITANCE : C_{IN} : 3.1 -> 3.2, C_{OUT} : 4 -> 4.2 Change AC TIMING CHARACTERISTICS - MIN t_{KHKL}, t_{KHKL} : -40 : 1.1 -> 1.2, -30 : 1.1 -> 1.4 - MIN t_{AVKH}, t_{BVKH}, t_{KHAX}, t_{KHBX} : -45 : 0.25 -> 0.27 - t_{KXCV} MIN/MAX : 0.8/2.3 -> 1.0/2.5 Change PACKAGE THERMAL CHARACTERISTICS	Feb. 2003	Advance

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Revision History

Rev No.	History	Draft Data	Remark
Rev 0.3	Change DC CHARACTERISTICS - x36 I_{DD} : I_{DD50} : 1050 -> 1150 , I_{DD45} : 950 -> 1050, I_{DD40}: 860 -> 960, I_{DD30}: 760 -> 860 - x18 I_{DD}: I_{DD50} : 1000 -> 1100, I_{DD45} : 900 -> 1000, I_{DD40}: 810 -> 910, I_{DD30}: 710 -> 810 - I_{SB1} : 200 -> 300	May. 2003	Advance
Rev 0.4	Change 300Mhz speed bin to 333Mhz	Jun. 2003	Advance
Rev 0.5	Change PIN CONFIGURATIONS - change DQ pin number Change AC CHARACTERISTICS - t_{CHCL}, t_{CLCH} : -/+0.2 -> -/+ 0.1	Aug. 2003	Advance
Rev 0.6	Change AC CHARACTERISTICS - Remove : t_{QTRK}, t_{CXCV} - Add : t_{CXCH},t_{CXCL},t_{CHQV},t_{CLQV},t_{CHQX},t_{CLQX},t_{CLQZ},t_{CHLZ}	Sep. 2003	Advance
Rev 0.7	Add Power-Up/Power-Down Supply Voltage Sequencing	Sep. 2003	Advance
Rev 0.8	Change PACKAGE PIN CONFIGURATIONS - Remove the number at DQ pins	Oct. 2003	Advance
Rev 0.9	Change Bin - 50, 45, 40, 33 -> 40, 37, 33	Feb. 2003	Advance
Rev 1.0	Change the word in READ OPERATION - at least one NOP -> at least two NOP	Mar. 2003	Final
Rev 1.1	Add AC INPUT CHARACTERISTICS and AC INPUT DEFINITION.	Apr. 2004	Final
Rev 1.2	Remove the comment for DDR3 from Spec.	Jun. 2004	Final
Rev 1.3	Modify AC TIMING CHARACTERISTICS - clock high/low pulse width : -40 : 1.2 -> 1.15 - remove min. value of t_{CHQV} and t_{CLQV}	Jan. 2005	Final
Rev 1.4	Add Pb free.	Oct. 2005	Final

FEATURES

- 1Mx36 or 2Mx18 Organizations.
- 1.8~2.5V V_{DD}/1.5V ~1.8V_{DDQ}.
- HSTL Input and Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write.
- Free Running Active High and Active Low Echo Clock Output Pin.
- Registered Addresses, Burst Control and Data Inputs.
- Registered Outputs.
- Double and Single Data Rate Burst Read and Write.
- Burst Count Controllable With Max Burst Length of 4
- Interleved and Linear Burst mode support
- Bypass Operation Support
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1)
- 153(9x17) Flip Chip Ball Grid Array Package(14mmx22mm)
- No Output enable support.

GENERAL DESCRIPTION

The K7D323674A and K7D321874A are 37,748,736 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 1,048,576 words by 36 bits for K7D323674A and 2,097,152 words by 18 bits for K7D321874A, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level clock, K and $\overline{K}$ are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. Data inputs are registered one cycle after write addresses are asserted(Late Write), at the rising edge of K clock for single data rate (SDR) write operations and at rising and falling edge of K clock for a double data rate (DDR) write operations.

Data outputs are updated from output registers off the rising edges of K clock for SDR read operations and off the rising and falling edges of K clock for DDR read operations. Free running echo clocks are supported which are representative of data output access time for all SDR and DDR operations.

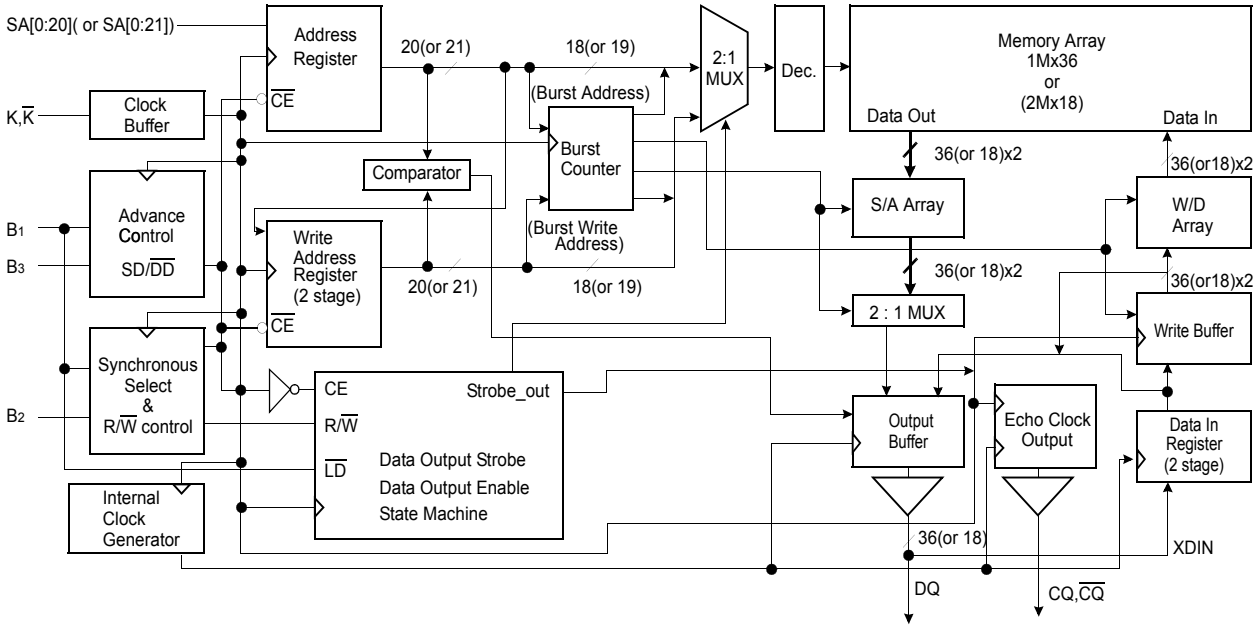
The chip is operated with 1.8~2.5V power supply and is compatible with HSTL input and output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

ORDERING INFORMATION

Part Number	Organization	Maximum Frequency
K7D323674A-H(G)C40	1Mx36	400MHz
K7D323674A-H(G)C37		375MHz
K7D323674A-H(G)C33		333MHz
K7D321874A-H(G)C40	2Mx18	400MHz
K7D321874A-H(G)C37		375MHz
K7D321874A-H(G)C33		333MHz

* G : Lead free package

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks	TCK	JTAG Test Clock
SA	Synchronous Address Input	TMS	JTAG Test Mode Select
SA_0, SA_1	Synchronous Burst Address Input (SA_0 = LSB)	TDI	JTAG Test Data Input
DQ	Synchronous Data I/O	TDO	JTAG Test Data Output
CQ, $\overline{CQ}$	Differential Output Echo Clocks	V_{REF}	HSTL Input Reference Voltage
B_1	Load External Address	V_{DD}	Power Supply
B_2	Burst R/$\overline{W}$ Enable	V_{DDQ}	Output Power Supply
B_3	Single/Double Data Selection	V_{SS}	GND
$\overline{LBO}$	Linear Burst Order	NC	No Connection
ZQ	Output Driver Impedance Control Input		

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7D323674A(1Mx36)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	DQ	DQ	SA	V_{SS}	B_1	V_{SS}	SA	DQ	DQ
C	V_{SS}	V_{DDQ}	SA	SA	SA	SA	SA	V_{DDQ}	V_{SS}
D	DQ	DQ	SA	V_{ss}(5)	V_{DD}	V_{ss}(6)	SA	DQ	DQ
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	DQ	CQ	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	CQ	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	K	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	DQ	DQ	V_{DD}	$\overline{K}$	V_{DD}	DQ	DQ	DQ
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	DQ	DQ	DQ	V_{SS}	B_2	V_{SS}	DQ	DQ	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B_3	MODE(7)	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	$\overline{CQ}$	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	$\overline{CQ}$	DQ
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	DQ	DQ	NC*	V_{SS}	V_{DD}(2)	V_{SS}	SA	DQ	DQ
R	V_{SS}	V_{DDQ}	V_{DD}(4)	SA	SA_1	SA	V_{DD}(3)	V_{DDQ}	V_{SS}
T	DQ	DQ	SA	V_{SS}	SA_0	V_{SS}	SA	DQ	DQ
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	V_{SS}

K7D321874A(2Mx18)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	NC	DQ	SA	V_{SS}	B_1	V_{SS}	SA	NC	DQ
C	V_{SS}	V_{DDQ}	SA	SA	SA	SA	SA	V_{DDQ}	V_{SS}
D	DQ	NC	SA	V_{ss}(5)	V_{DD}	V_{ss}(6)	SA	DQ	NC
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	NC	CQ	NC	V_{DD}	V_{DD}	V_{DD}	DQ	NC	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	K	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	NC	DQ	V_{DD}	$\overline{K}$	V_{DD}	NC	DQ	NC
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	NC	DQ	NC	V_{SS}	B_2	V_{SS}	DQ	NC	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B_3	MODE(7)	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	NC	DQ	V_{DD}	V_{DD}	V_{DD}	NC	$\overline{CQ}$	NC
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	NC	DQ	SA	V_{SS}	V_{DD}(2)	V_{SS}	SA	NC	DQ
R	V_{SS}	V_{DDQ}	V_{DD}(4)	SA	SA_1	SA	V_{DD}(3)	V_{DDQ}	V_{SS}
T	DQ	NC	SA	V_{SS}	SA_0	V_{SS}	SA	DQ	NC
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	V_{SS}

(1) Variable address see "Variable address assignment table"
(2) Variable address see "Variable address assignment table"
(3) Variable address see "Variable address assignment table"
(4) Variable address see "Variable address assignment table"
(5) Variable address see "Variable address assignment table"
(6) Variable address see "Variable address assignment table"
(7) Internally NC

VARIABLE ADDRESS ASSIGNMENT TABLE

Density	Ball 5C (1)	Ball 5P (2)	Ball 7R (3)	Ball 3R (4)	Ball 4D (5)	Ball 6D (6)
32 Mb	SA	V_{DD}	V_{DD}	V_{DD}	V_{ss}	V_{ss}
64 Mb	SA	SA	V_{DD}	V_{DD}	V_{ss}	V_{ss}
144 Mb	NC	SA	SA	SA	V_{ss}	V_{ss}
288 Mb	SA	SA	SA	SA	V_{ss}	V_{ss}
576 Mb	NC	SA	SA	SA	SA	SA
1152 Mb	SA	SA	SA	SA	SA	SA

NOTE : - SRAM density definition beyond 144Mb will include the parity bits.

Read Operation(Single and Double)

During SDR read operations, addresses and controls are registered at the first rising edge of K clock and then the internal array is read between first and second rising edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During DDR read operations, addresses and controls are registered at the first rising edge of K clock, and then the internal array is read twice between first and second rising edges of K clock. Data outputs are updated from output registers sequentially by burst order off the second rising and falling edge of K clock.
Interleave and linear burst operation is controlled by $\overline{LBO}$ pin and the burst count is controllable with the maximum burst length of 4.
To avoid data contention,at least two NOP operations are required between the last read and the first write operation.

Write Operation(Late Write)

During SDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. During DDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered twice at the following rising and falling edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write opeation are data inputs fully written into SRAM array.

Echo clock operation

Free running type of Echo clocks are generated from K clock regardless of read, write and NOP operations. They will stop operation only when K clock is in the stop mode.
Echo clocks are designed to represent data output access time and this allows the echo clocks to be used as reference to capture data outputs outputs.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array.

Programmable Impedance Output Driver

The data output and echo clock driver impedance are adjusted by an external resistor, RQ, connected between ZQ pin and V_{SS}, and are equal to RQ/5. For example, 250Ω resistor will give an output impedance of 50Ω. Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Output driver impedance is updated every 64 clock cycles of Non-Read operation (Write or NOP) but since the echo clock drivers are in operation even during Non-Read operation, the impedance is update only the drivers are not in operation. Therefore impedance updates for "0s" or pull down drivers occur whenever the echo clock driver is driving "1s" or vice versa. Furthermore, to guarantee optimum output driver impedance after power up, the SRAM need 2048 deselect (or write) cycles.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, then V_{IN}. V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, V_{SS}. V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

TRUTH TABLE

K	B1	B2	B3	DQ	Operation
↑	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	H	H	DOUT	Load Address, Single Read
↑	L	H	L	DOUT	Load Address, Double Read
↑	L	L	H	DIN	Load Address, Single Write
↑	L	L	L	DIN	Load Address, Double Write
↑	H	H	X	B	Increment Address, Continue

NOTE : - B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".
- K & $\overline{K}$ are complementary.

OUTPUT TRISTATE TRUTH TABLE

K	Operation	DQ (n)	DQ (n+1)
↑	Write (B2=L)	X	High-Z
↑	Deslect (NOP) (B1=H, B2=L)	X	High-Z

BURST SEQUENCE TABLE

4 Burst Operation for Interleaved Burst ($\overline{LBO}$ = V_{DDQ})

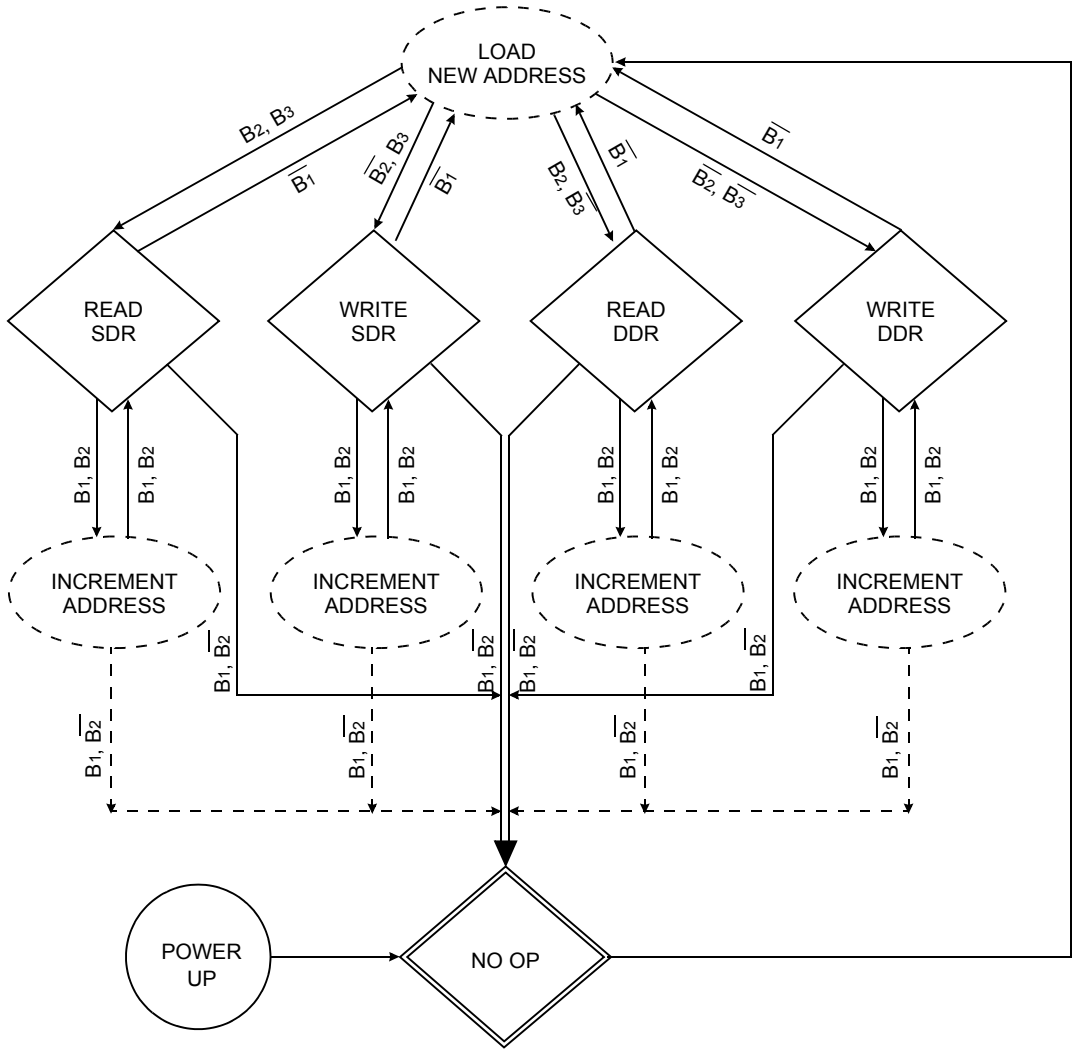
Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

NOTE : - For Interleave Burst $\overline{LBO}$ = V_{DDQ} is recommended. If $\overline{LBO}$ = V_{DD}, it must not exceed 2.63V.

4 Burst Operation for Linear Burst ($\overline{LBO}$ = V_{SS})

Linear Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE :

1. State transitions ; $\overline{B}_1$ =(Load Address), B_1=(Increment Address, Continue)
   B_2 =(Read), $\overline{B}_2$ =(Write)
   B_3 =(Single Data Rate), $\overline{B}_3$ =(Double Data Rate)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to V_{SS}	V_{DD}	-0.5 to 3.13	V
Output Supply Voltage Relative to V_{SS}	V_{DDQ}	-0.5 to 2.3	V
Voltage on any pin Relative to V_{SS}	V_{IN}	-0.5 to V_{DDQ}+0.5 (2.3V MAX)	V
Output Short-Circuit Current(per I/O)	I_{OUT}	25	mA
Storage Temperature	T_{STR}	-55 to 125	°C
Maxmum Junction Temperature	T_J	110	°C
Maxmum Power Dissipation	P_D	3.0	W

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	1.7	2.5	2.6	V	
Output Power Supply Voltage	V_{DDQ}	1.4	1.5	1.9	V	
Input High Level Voltage	V_{IH}	V_{REF}+0.1	-	V_{DDQ}+0.3	V	1, 2
Input Low Level Voltage	V_{IL}	-0.3	-	V_{REF}-0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	1.0	V	

NOTE :1. These are DC test criteria. DC design criteria is V_{REF}±50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max)DC=V_{DDQ}+0.3, V_{IH} (Max)AC=2.6V (2.1V for DQs) (pulse width ≤ 20% of cycle time).
3. V_{IL} (Min)DC=-0.3V, V_{IL} (Min)AC=-1.0V (-0.5V for DQs) (pulse width ≤ 20% of cycle time).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current(x36) (Cycle time = t_{KHKH} min)	I_{DD40} I_{DD37} I_{DD33}	-	960 940 900	mA	1,2
Average Power Supply Operating Current(x18) (Cycle time = t_{KHKH} min)	I_{DD40} I_{DD37} I_{DD33}	-	910 890 850	mA	1,2
Stop Clock Standby Current (V_{IN}=V_{DD}-0.2V or 0.2V fixed, K=Low, $\overline{K}$=High)	I_{SB1}	-	300	mA	1
Input Leakage Current (V_{IN}=V_{SS} or V_{DDQ})	I_{LI}	-3	3	μA	
Output Leakage Current (V_{OUT}=V_{SS} or V_{DDQ})	I_{LO}	-5	5	μA	
Output High Voltage(Programmable Impedance Mode)	V_{OH1}	V_{DDQ}/2	V_{DDQ}	V	3
Output Low Voltage(Programmable Impedance Mode)	V_{OL1}	V_{SS}	V_{DDQ}/2	V	4
Output High Voltage(I_{OH}=-0.1mA)	V_{OH2}	V_{DDQ}-0.2	V_{DDQ}	V	
Output Low Voltage(I_{OL}=0.1mA)	V_{OL2}	V_{SS}	0.2	V	

NOTE :1. Minimum cycle. I_{OUT}=0mA.
2. 50% read cycles.
3. $|I_{OH}|$=(V_{DDQ}/2)/(RQ/5)±15% @V_{OH}=V_{DDQ}/2 for 175Ω ≤ RQ ≤ 300Ω.
4. $|I_{OL}|$=(V_{DDQ}/2)/(RQ/5)±15% @V_{OL}=V_{DDQ}/2 for 175Ω ≤ RQ ≤ 300Ω.

PIN CAPACITANCE

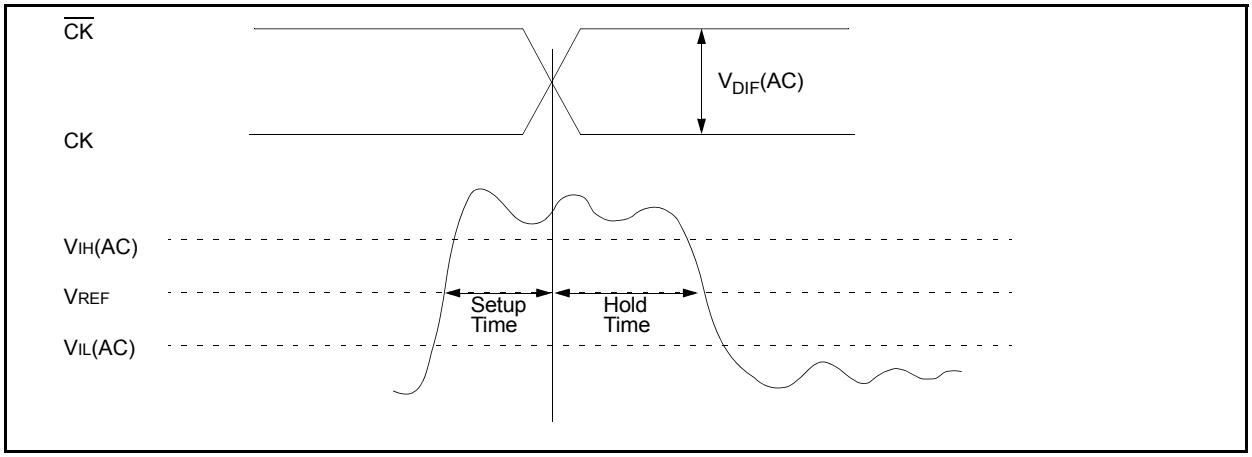
Parameter	Symbol	Test Condition	TYP	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	3.2	pF
Data Output Capacitance	C_{OUT}	V_{OUT}=0V	-	4.2	pF

NOTE : Periodically sampled and not 100% tested.(T_A=25°C, f=500MHz)

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
AC Input Logic High	V_{IH} (AC)	V_{REF} + 0.4		V	-
AC Input Logic Low	V_{IL} (AC)		V_{REF} - 0.4	V	-
Clock Input Differential Voltage	V_{DIF} (AC)	0.8		V	-
V_{REF} Peak-to-Peak AC Voltage	V_{REF} (AC)		5% V_{REF} (DC)	V	-

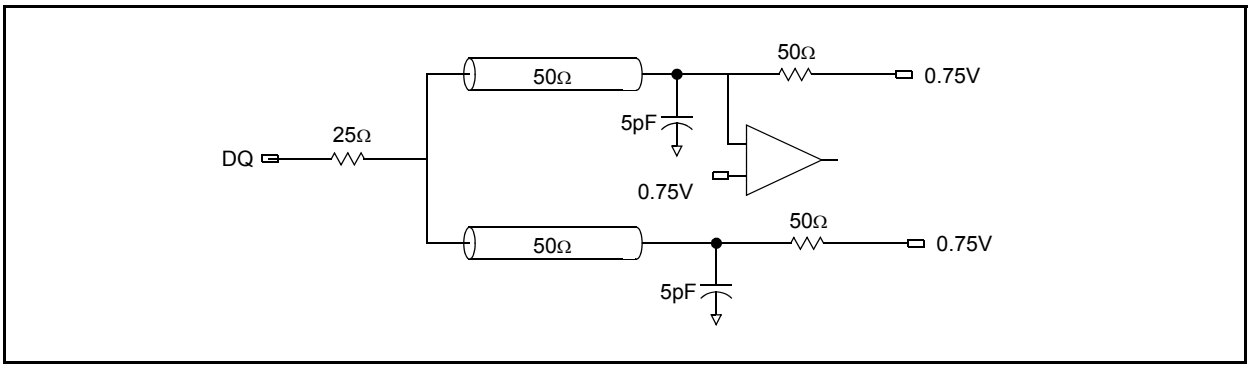
AC INPUT DEFINITION



AC TEST CONDITIONS(T_A=0 to 70°C, V_{DD}=2.37 -2.63V, V_{DDQ}=1.5V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.25/0.25	V	-
Input Reference Level	V_{REF}	0.75	V	-
Input Rise/Fall Time	T_R/T_F	0.5/0.5	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load	See Below			-

AC TEST OUTPUT LOAD

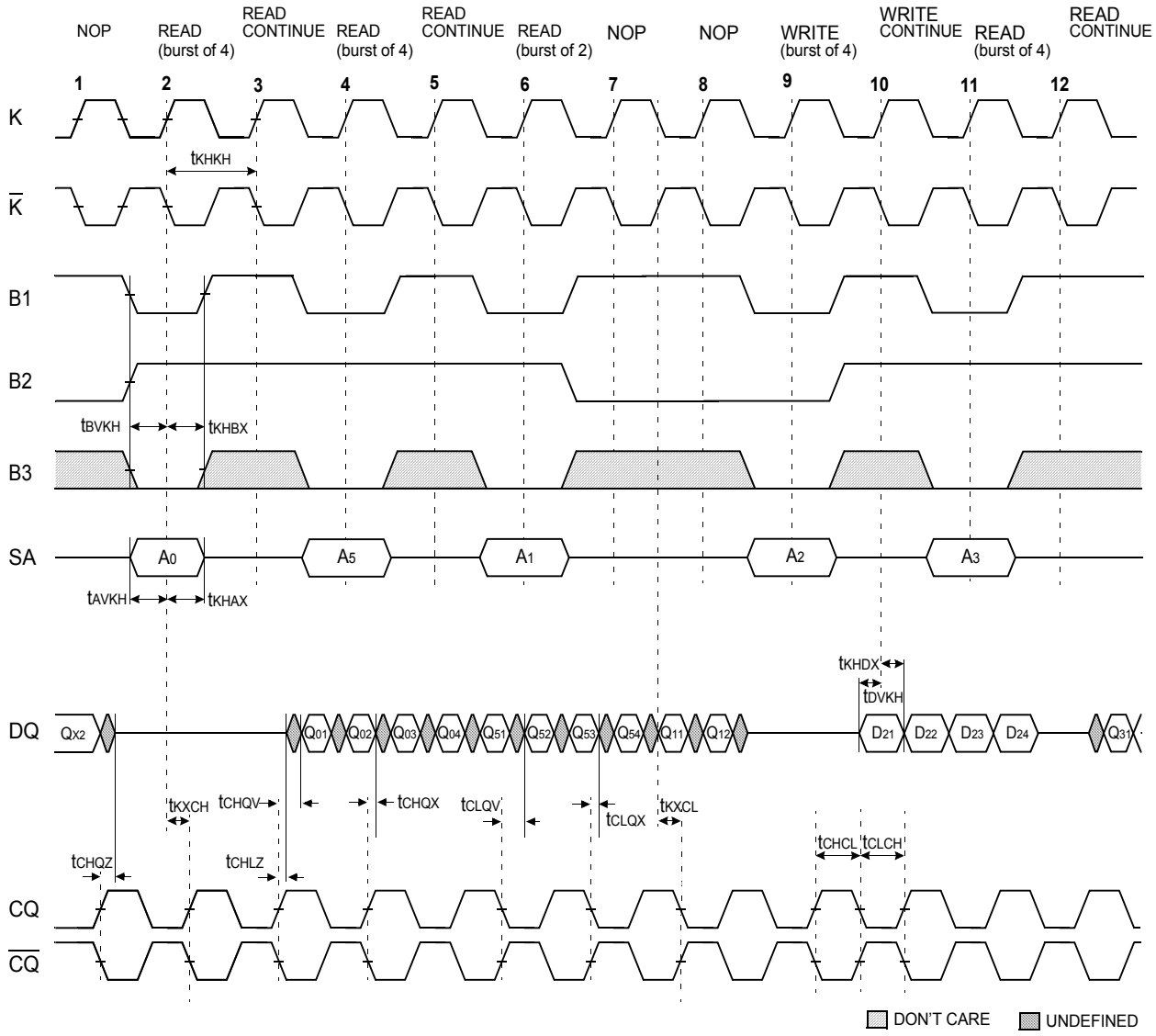


AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-40		-37		-33		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock Cycle Time	t_{KHKH}	2.50	5.00	2.67	6.00	3.00	6.00	ns	1
Clock High Pulse Width	t_{KHKL}	1.15		1.25		1.40		ns	
Clock Low Pulse Width	t_{KLKH}	1.15		1.25		1.40		ns	
Setup Times									
Address Setup Time	t_{AVKH}	0.30		0.33		0.35		ns	
Control(B1,B2,B3) Setup Time	t_{BVKH}	0.30		0.33		0.35		ns	
Data Setup Time	t_{DVKX}	0.20		0.25		0.30		ns	2
Hold Times									
Address Hold Time	t_{KHAX}	0.30		0.33		0.35		ns	
Control(B1,B2,B3) Hold Time	t_{KHBX}	0.30		0.33		0.35		ns	
Data Hold Time	t_{KXDX}	0.20		0.25		0.30		ns	2
Output Times									
Echo Clock High Pulse Width	t_{CHCL}	t_{KHKL}-0.1	t_{KHKL}+0.1	t_{KHKL}-0.1	t_{KHKL}+0.1	t_{KHKL}-0.1	t_{KHKL}+0.1	ns	2
Echo Clock Low Pulse Width	t_{CLCH}	t_{KLKH}-0.1	t_{KLKH}+0.1	t_{KLKH}-0.1	t_{KLKH}+0.1	t_{KLKH}-0.1	t_{KLKH}+0.1	ns	2
Clock Crossing to Echo Clock	t_{CXCH}	1.0	2.5	1.0	2.5	1.0	2.5	ns	3
Clock Crossing to Echo Clock	t_{CXCL}	1.0	2.5	1.0	2.5	1.0	2.5	ns	3
Echo Clock High to Output Vaild	t_{CHQV}		0.20		0.20		0.20	ns	
Echo Clock Low to Output Valid	t_{CLQV}		0.20		0.20		0.20	ns	
Echo Clock High to Output Hold	t_{CHQX}	-0.20		-0.20		-0.20		ns	
Echo Clock Low to Output Hold	t_{CLQX}	-0.20		-0.20		-0.20		ns	
Echo Clock High to Output High-Z	t_{CHQZ}		0.20		0.20		0.20	ns	
Echo Clock High to Output Low-Z	t_{CHLZ}	-0.20		-0.20		-0.20		ns	

Notes: 1. The maximum cycle time must be limited to guarantee AC timing specification.
2. This parameter is guaranteed by design, and may not be tested at values shown in the table.
3. This parameter refers to CQ and $\overline{CQ}$ rising and falling edges.
4. This parameter is only for 32Mb density
5. K and $\overline{K}$ Clocks must be used differencitally to meet AC timing specifications.

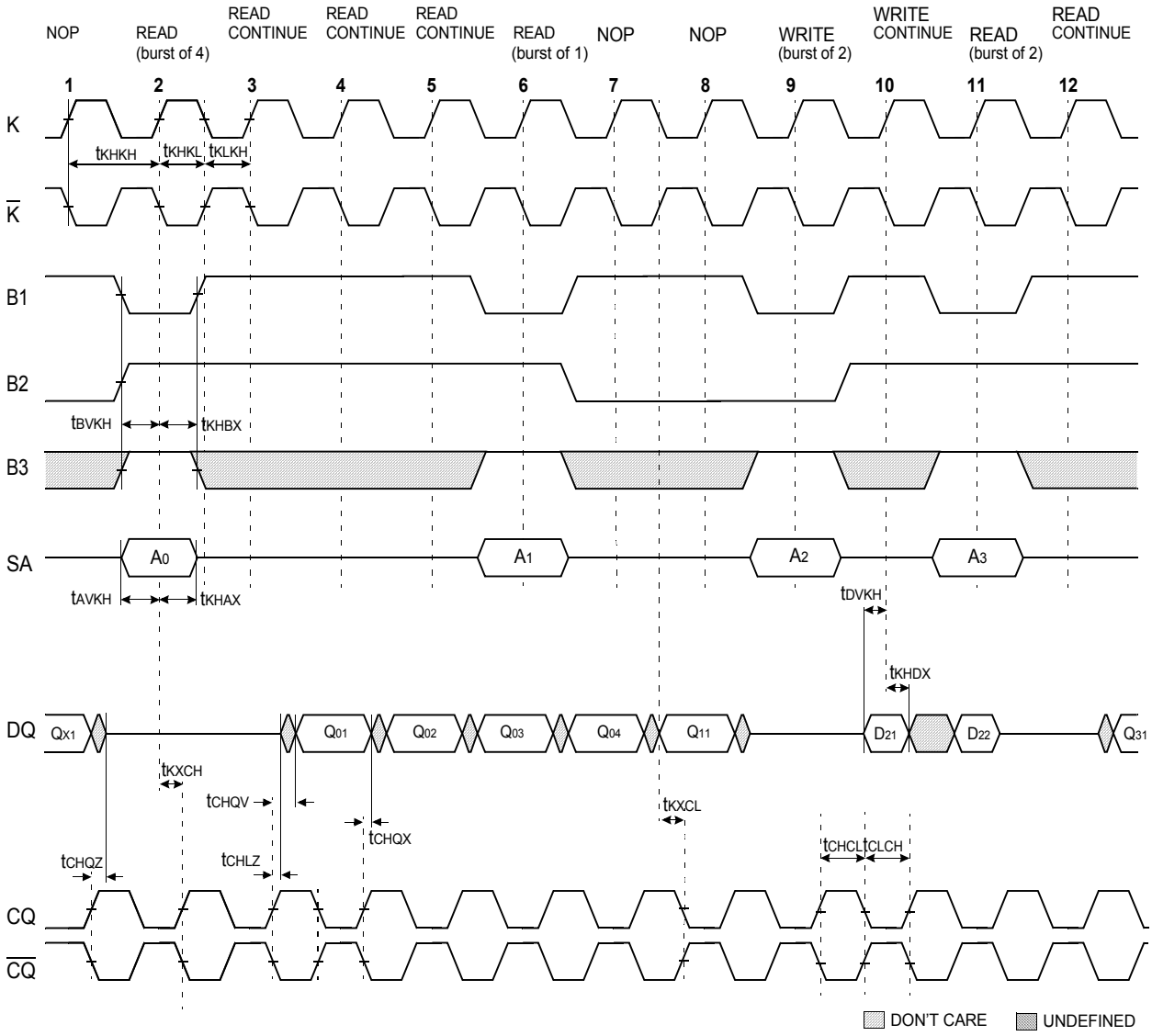
TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES (Burst Length=4, 2)



NOTE

1. Q_{01} refers to output from address A. Q_{02} refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.

TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES
(Burst Length=4, 2, 1)

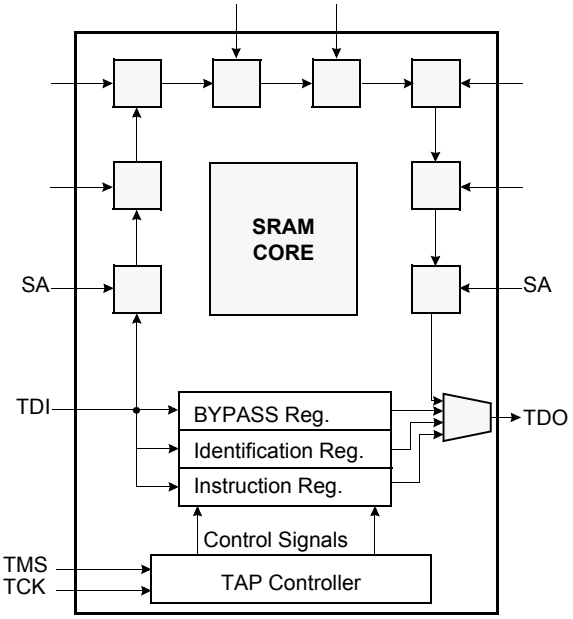


NOTE :
1. Q_{01} refers to output from address A_0. Q_{02} refers to output from the next internal burst address following A_0, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. This devices supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation. Any further Continue assertions constitute invalid operations.
4. This device will have an address wraparound if further Continues are applied.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and therefore can be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



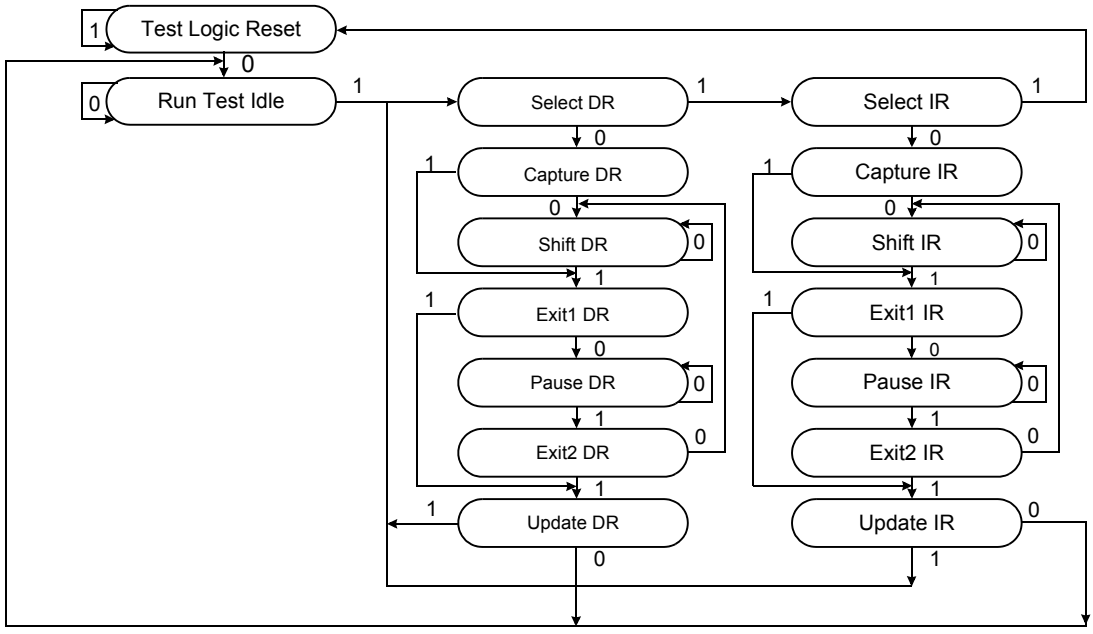
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	PRIVATE3	Bypass Register	3,5
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	PRIVATE2	Bypass Register	3,5
1	1	0	PRIVATE1	Bypass Register	3,5
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. Input terminators are switched off.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked.
   The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.
5. PRIVATE1 and PRIVATE2 are reserved for the exclusive use of SAMSUNG. This instruction should not be used.

TAP Controller State Diagram



BOUNDARY SCAN EXIT ORDER(x36)

1	5P	V_{DD}(2)		38	5C	SA
2	5R	SA_1		39	4A	SA
3	5T	SA_0		40	4C	SA
4	6R	SA		41	4D	V_{SS}(2
5	7T	SA		42	3A	SA
6	7R	V_{DD}(2)		43	3B	SA
7	7P	SA		44	3C	SA
8	8T	DQ1		45	3D	SA
9	9T	DQ2		46	2B	DQ19
10	8P	DQ10		47	1B	DQ20
11	7M	DQ0		48	2D	DQ28
12	9P	DQ12		49	3F	DQ18
13	8M	$\overline{CQ}$(3)		50	1D	DQ30
14	9M	DQ3		51	2F	CQ(3)
15	7K	DQ9		52	1F	DQ21
16	8K	DQ11		53	3H	DQ27
17	9K	DQ13		54	2H	DQ29
18	6L	MODE		55	1H	DQ31
19	5H	$\overline{K}$		56	5A	ZQ(1)
20	5G	K		57	5B	B_1
21	9H	DQ4		58	5K	B_2
22	8H	DQ6		59	5L	B_3
23	7H	DQ8		60	4L	$\overline{LBO}$
24	9F	DQ14		61	1K	DQ22
25	8F	CQ(3)		62	2K	DQ24
26	9D	DQ5		63	3K	DQ26
27	7F	DQ17		64	1M	DQ32
28	8D	DQ7		65	2M	$\overline{CQ}$(3)
29	9B	DQ15		66	1P	DQ23
30	8B	DQ16		67	3M	DQ35
31	7D	SA		68	2P	DQ25
32	7C	SA		69	1T	DQ33
33	7B	SA		70	2T	DQ34
34	7A	SA		71	3R	V_{DD}(2)
35	6D	V_{SS}(2)		72	3T	SA
36	6C	SA		73	4R	SA
37	6A	SA		74	7U	NC

* Reserved for Mode Pin

BOUNDARY SCAN EXIT ORDER(x18)

1	5P	V_{DD}(2)		28	5C	SA
2	5R	SA_1		29	4A	SA
3	5T	SA_0		30	4C	SA
4	6R	SA		31	4D	V_{SS}(2)
5	7T	SA		32	3A	SA
6	7R	V_{DD}(2)		33	3B	SA
7	7P	SA		34	3C	SA
8	8T	DQ1		35	3D	SA
				36	2B	DQ10
9	9P	DQ2				
10	8M	$\overline{CQ}$(3)		37	1D	DQ11
				38	2F	CQ(3)
11	7K	DQ0				
				39	3H	DQ9
12	9K	DQ3				
13	6L	MODE		40	1H	DQ12
14	5H	$\overline{K}$		41	5A	ZQ(1)
15	5G	K		42	5B	B1
				43	5K	B2
16	8H	DQ6		44	5L	B3
				45	4L	$\overline{LBO}$
17	9F	DQ4				
				46	2K	DQ15
18	7F	DQ8		47	1M	DQ13
19	8D	DQ7				
20	9B	DQ5				
				48	3M	DQ17
21	7D	SA		49	2P	DQ16
22	7C	SA		50	1T	DQ14
23	7B	SA		51	3P	SA
24	7A	SA		52	3R	V_{DD}(2)
25	6D	V_{SS}(2)		53	3T	SA
26	6C	SA		54	4R	SA
27	6A	SA		55	7U	NC

* Reserved for Mode Pin

NOTE :
1. If pin is connected as they should, TDO will be low. If pin is open, TDO will be high
2. This pin is place holder for higher density. TDO will be low for V_{SS} and high for V_{DD}
3. CQ and $\overline{CQ}$ are outputs during boundary scan. CQ reflects the input to K and $\overline{CQ}$ outputs the inverted value of K. It is prohibited to force CQ and $\overline{CQ}$. And TDO is 'X'.(Don't Care)

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1M x 36	3 bits	1 bits	32 bits	74 bits
2M x 18	3 bits	1 bits	32 bits	55 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
1M x 36	0000	01000 00100	XXXXXX	00001001110	1
2M x 18	0000	01001 00011	XXXXXX	00001001110	1

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	2.5	2.6	V	
Input High Level	V_{IH}	0.65*V_{DD}	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.35*V_{DD}	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	0.75*V_{DD}	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.25*V_{DD}	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

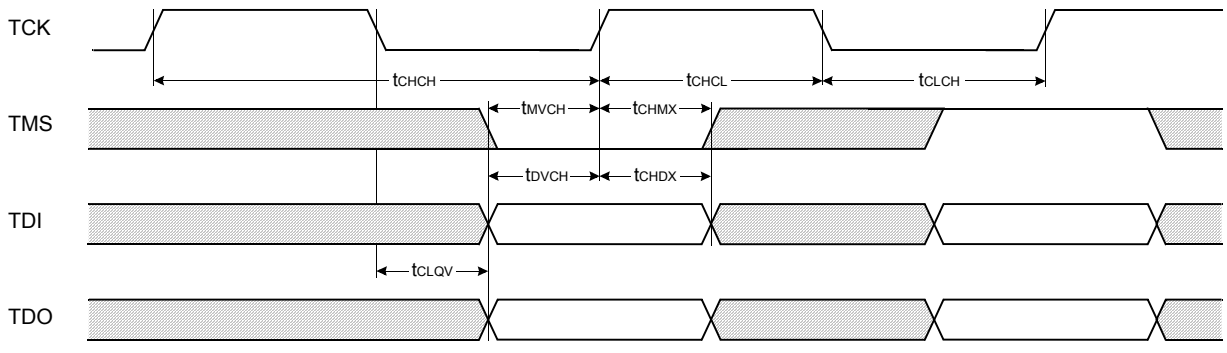
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	V_{DD}/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		V_{DD}/2	V	1

NOTE : 1. See SRAM AC test output load on page 5.

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

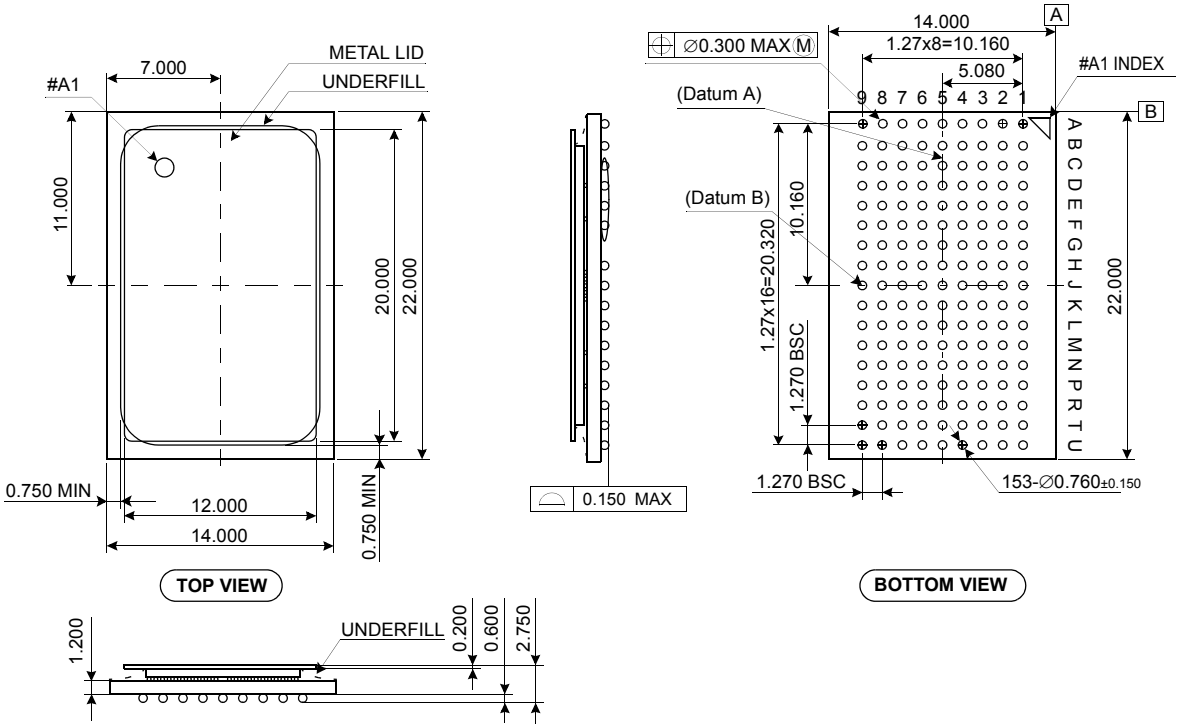
JTAG TIMING DIAGRAM



PACKAGE DIMENSIONS

153-FCBGA-14.00x22.00 LID

Units:millimeters/Inches



153 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Case	θ_{JC}	0.9	°C/W	
Junction to Board	θ_{JB}	6.9	°C/W	
Junction to Ambient(at air flow of 1m/sec)	θ_{JA}	16.1	°C/W	
Junction to Ambient(at still air)	θ_{JA}	19.5	°C/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times \theta_{JA}$ or $T_J = T_C + P_D \times \theta_{JC}$

2. Strongly recommends using a heat sink because it greatly improves the ambient temperature requirement