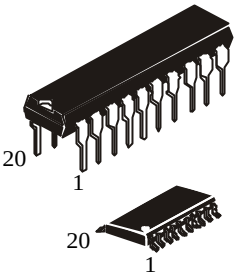
IN74LV273

Octal D Flip-Flop with Common Clock and Reset

The IN74LV273 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT273.
The IN74LV273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (MR) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 1.2 to 5.5 V
- Low input current: 1.0 µÀ; 0.1 µÀ at Ò = 25 °Ñ
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC DIP

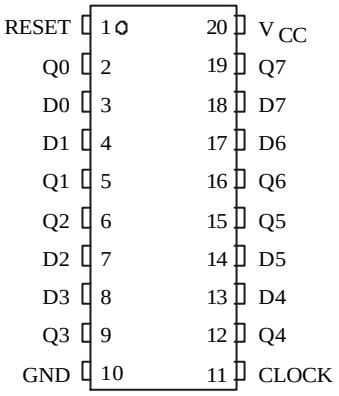
DW SUFFIX
SO

ORDERING INFORMATION

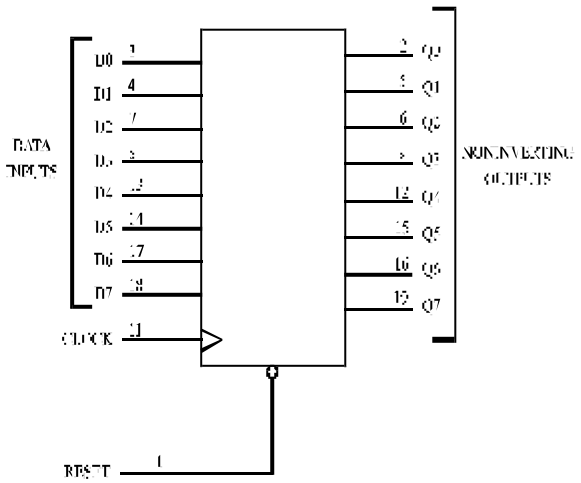
IN74LV273N	Plastic DIP
IN74LV273DW	SOIC
IZ74LV273	chip

T_A = -40° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	no change
H	↓	X	no change

H= high level
L = low level
X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +7.0	V
I_{IK} *1	Input diode current	±20	mA
I_{OK} *2	Output diode current	±50	mA
I_O *3	Output source or sink current	±25	mA
I_{CC}	V_{CC} current	±50	mA
I_{GND}	GND current	±50	mA
P_D	Power dissipation per package: Plastic DIP *4 SO *4	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	5.5	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0 V ≤ V_{CC} ≤ 2.0 V 2.0 V ≤ V_{CC} ≤ 2.7 V 2.7 V ≤ V_{CC} ≤ 3.6 V 3.6 V ≤ V_{CC} ≤ 5.5 V	0 0 0 0	500 200 100 50	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit								Unit
				25°C		-40°C		85°C		125°C		
				min	max	min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	1.4	-	
			2.7	2.0	-	2.0	-	2.0	-	2.0	-	
			3.0	2.0	-	2.0	-	2.0	-	2.0	-	
			3.6	2.0	-	2.0	-	2.0	-	2.0	-	
			4.5	3.15	-	3.15	-	3.15	-	3.15	-	
			5.5	3.85	-	3.85	-	3.85	-	3.85	-	
V_{IL}	LOW level output voltage		1.2	-	0.3	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	-	0.6	
			2.7	-	0.8	-	0.8	-	0.8	-	0.8	
			3.0	-	0.8	-	0.8	-	0.8	-	0.8	
			3.6	-	0.8	-	0.8	-	0.8	-	0.8	
			4.5	-	1.35	-	1.35	-	1.35	-	1.35	
			5.5	-	1.65	-	1.65	-	1.65	-	1.65	
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -100 µA	1.2	1.05	-	1.05	-	1.0	-	1.0	-	V
			2.0	1.85	-	1.85	-	1.8	-	1.8	-	
			2.7	2.55	-	2.55	-	2.5	-	2.5	-	
			3.0	2.85	-	2.85	-	2.8	-	2.8	-	
			3.6	3.45	-	3.45	-	3.4	-	3.4	-	
			4.5	4.35	-	4.35	-	4.3	-	4.3	-	
			5.5	5.35	-	5.35	-	5.3	-	5.3	-	
		$V_I = V_{IH}$ or V_{IL} I_O = -6 mA	3.0	2.48	-	2.48	-	2.40	-	2.20	-	V
		$V_I = V_{IH}$ or V_{IL} I_O = -12 mA	4.5	3.70	-	3.70	-	3.60	-	3.50	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 100 µA	1.2	-	0.15	-	0.15	-	0.2	-	0.2	V
			2.0	-	0.15	-	0.15	-	0.2	-	0.2	
			2.7	-	0.15	-	0.15	-	0.2	-	0.2	
			3.0	-	0.15	-	0.15	-	0.2	-	0.2	
			3.6	-	0.15	-	0.15	-	0.2	-	0.2	
			4.5	-	0.15	-	0.15	-	0.2	-	0.2	
			5.5	-	0.15	-	0.15	-	0.2	-	0.2	
		$V_I = V_{IH}$ or V_{IL} I_O = 6 mA	3.0	-	0.33	-	0.33	-	0.40	-	0.50	V
		$V_I = V_{IH}$ or V_{IL} I_O = 12 mA	4.5	-	0.40	-	0.40	-	0.55	-	0.65	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	5.5	-	±0.1	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V I_O = 0 µA	5.5	-	8.0	-	8.0	-	80	-	160	µA
I_{CC1}	Additional supply current per input	$V_I = V_{CC}$ – 0.6V	2.7	-	0.2	-	0.2	-	0.5		0.85	mA
			3.6									

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_r=t_f=2.5 ns)

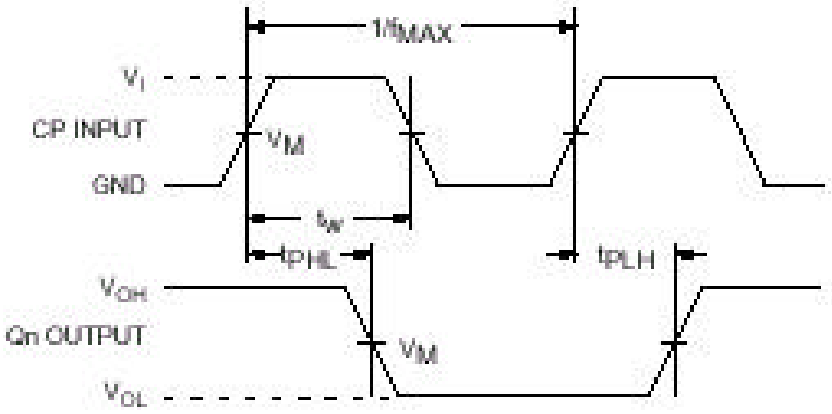
Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , Clock to Q	V_I = 0 V or V_1 Figures 1,4	1.2	-	150	-	150	-	150	ns
			2.0	-	30	-	32	-	41	
			2.7	-	22	-	24	-	30	
			3.0	-	17	-	19	-	24	
			4.5	-	14	-	16	-	20	
t_{PHL}	Propagation delay , Reset to Q	V_I = 0 V or V_1 Figures 2,4	1.2	-	160	-	160	-	160	ns
			2.0	-	40	-	44	-	56	
			2.7	-	30	-	33	-	41	
			3.0	-	23	-	26	-	33	
			4.5	-	19	-	22	-	28	
C_I	Input capacitance		5.0	-	6.0*	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per flip-flop)	V_I = 0 V or V_{CC}	5.5	-	40*	-	-	-	-	pF

* T = 25°C

TIMING REQUIREMENTS (C_L=50 pF, t_r=t_f=2.5 ns)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				-40°C to 25°C		85°C		125°C		
				min	max	min	max	min	max	
t_w	Pulse Width, Clock (low or high), Reset (low)	V_I = 0 V or V_1 Figures 1,2,4	1.2	60	-	70	-	80	-	ns
			2.0	28	-	34	-	41	-	
			2.7	21	-	25	-	30	-	
			3.0	16	-	20	-	24	-	
			4.5	12	-	16	-	20	-	
t_{su}	Setup Time, Data to Clock	V_I = 0 V or V_1 Figures 3,4	1.2	40	-	50	-	60	-	ns
			2.0	18	-	22	-	26	-	
			2.7	13	-	16	-	19	-	
			3.0	11	-	13	-	15	-	
			4.5	9	-	11	-	13	-	
t_{rem}	Removal Time, Reset to Clock	V_I = 0 V or V_1 Figures 2,4	1.2	5	-	5	-	5	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	
t_h	Hold Time, Clock to Data	V_I = 0 V or V_1 Figures 3,4	1.2	50	-	50	-	50	-	ns
			2.0	5	-	5	-	5	-	
			2.7	5	-	5	-	5	-	
			3.0	5	-	5	-	5	-	
			4.5	5	-	5	-	5	-	

f_c	Clock Frequency	V_I = 0 V or V_I Figures 1,4	1.2 2.0 2.7 3.0 4.5	- - - - -	2 17 23 30 32	- - - - -	1 14 19 24 27	- - - - -	1 12 16 20 24	MHz



V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Figure 1. Switching Waveforms

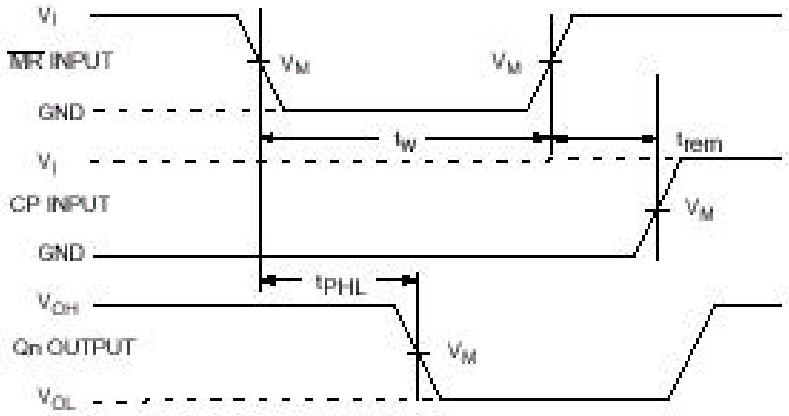


Figure 2. Switching Waveforms

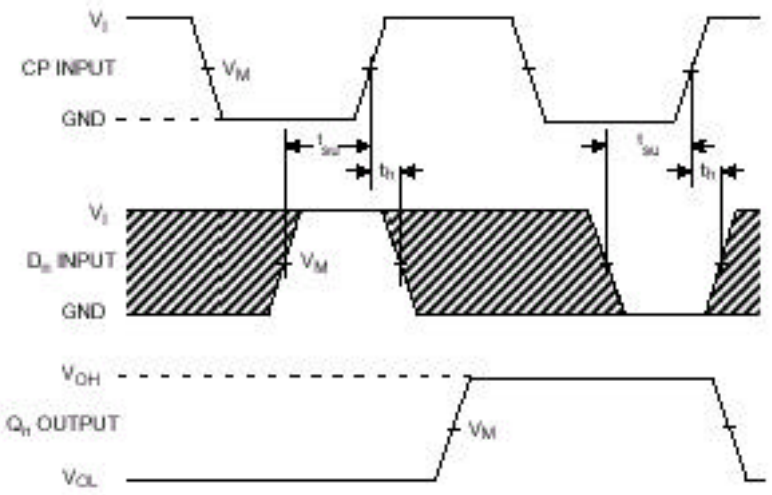
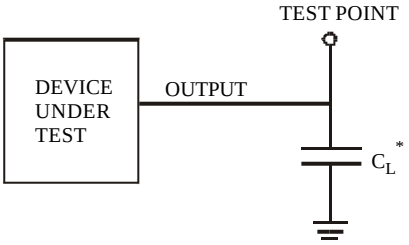


Figure 3. Switching Waveforms

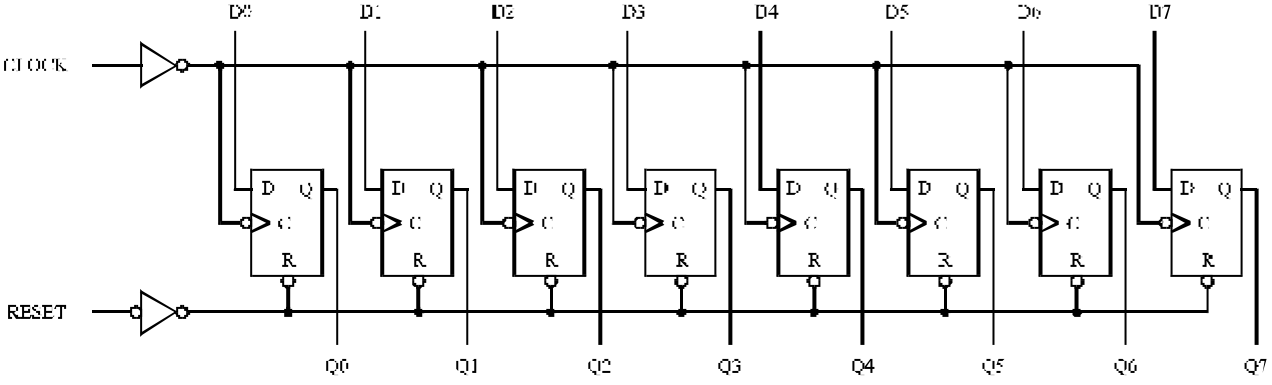
Symbol	Level of a signal, V				
V_{CC}	1,2	2,0	2,7	3,0	4,5
V_I	1,2	2,0	2,7	2,7	4,5
V_M	0,6	1,0	1,5	1,5	2,25



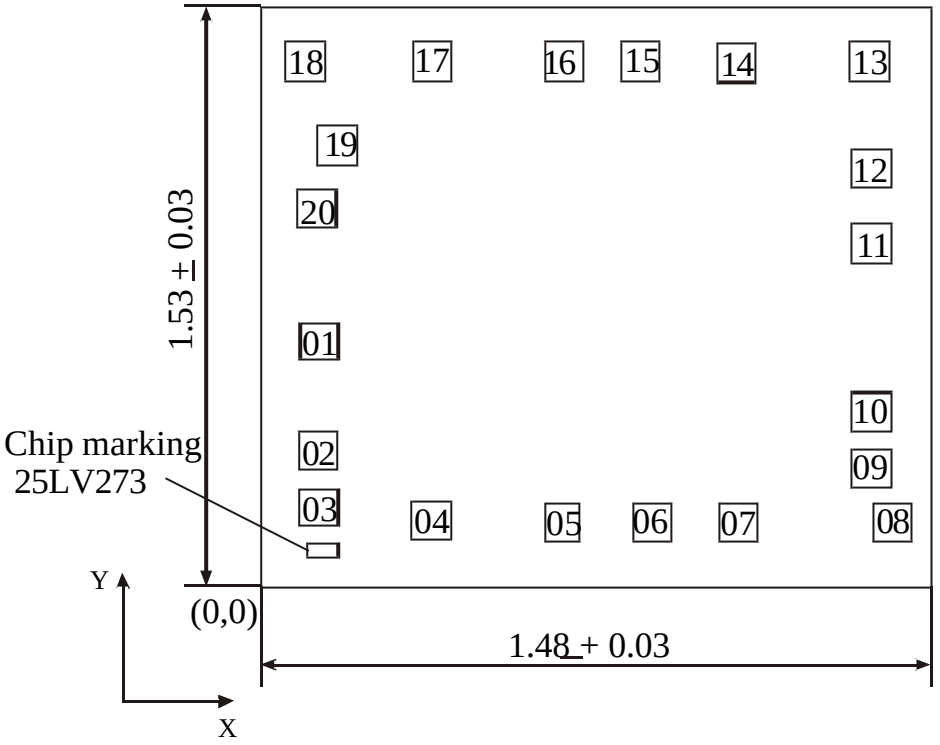
* Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=0.119, y=0.082.

Chip thickness: 0.46 ± 0.02 mm, (0.35 ± 0.02 mm – for SOIC).

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Reset	0.1415	0.6270	0.100 x 0.100
02	Q 0	0.1415	0.3880	0.100 x 0.100
03	D 0	0.1375	0.1515	0.100 x 0.100
04	D 1	0.4535	0.1190	0.100 x 0.100
05	Q 1	0.6245	0.1190	0.100 x 0.100
06	Q 2	0.7800	0.1190	0.100 x 0.100
07	D 2	0.9520	0.1180	0.100 x 0.100
08	D 3	1.2685	0.1185	0.100 x 0.100
09	Q 3	1.2480	0.2960	0.100 x 0.100
10	GND	1.2650	0.5160	0.100 x 0.100
11	Clock	1.2650	0.8430	0.100 x 0.100
12	Q 4	1.2425	1.0820	0.100 x 0.100
13	D 4	1.2465	1.3165	0.100 x 0.100
14	D 5	0.9520	1.3120	0.100 x 0.100
15	Q 5	0.7800	1.3110	0.100 x 0.100
16	Q 6	0.6245	1.3110	0.100 x 0.100
17	D 6	0.4535	1.3110	0.100 x 0.100
18	D 7	0.1160	1.3115	0.100 x 0.100
19	Q 7	0.1440	1.1350	0.100 x 0.100
20	V_{CC}	0.1190	0.9140	0.100 x 0.100

Note: Pad location is given as per passivation layer.