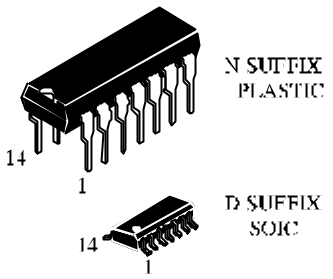
IN74LV00

Quad 2-Input NAND Gate



ORDERING INFORMATION

IN74LV00N	Plastic
IN74LV00D	SOIC
IZ74LV00	Chip

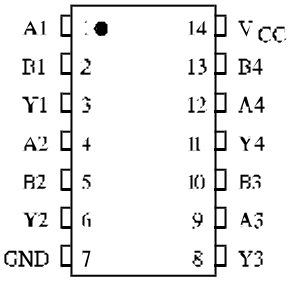
T_A = -40° ? 125° C for all packages

The IN74LV00 is low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT00A.

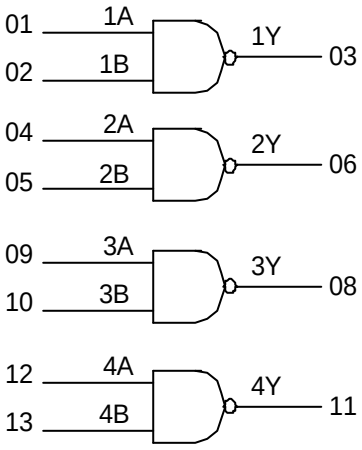
The IN74LV00 provides the 2-Input NAND function.

- Optimized for Low Voltage applications: 1.2 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Low Input Current

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 14 =V_{CC}
PIN 7 = GND

FUNCTION TABLE

Input		Output
A	B	$Y = \overline{A * B}$
L	L	H
L	H	H
H	L	H
H	H	L

H - high level
L - low level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (Referenced to GND)	-0.5 ÷ +5.0	V
I_{IK} *1	DC input diode current	±20	mA
I_{OK} *2	DC output diode current	±50	mA
I_O *3	DC output source or sink current -bus driver outputs	±25	mA
I_{CC}	DC V_{CC} current for types with - bus driver outputs	±50	mA
I_{GND}	DC GND current for types with - bus driver outputs	±50	mA
P_D	Power dissipation per package, plastic DIP+ SOIC package+	750 500	mW
Tstg	Storage temperature	-65 ÷ +150	°C
T_L	Lead temperature, 1.5 mm from Case for 10 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SOIC Package: : - 8 mW/°C from 70° to 125°C
*1: $V_I < -0.5$ or $V_I > V_{CC}+0.5V$
*2: $Vo < -0.5$ or $Vo > V_{CC}+0.5V$
*3: $-0.5V < Vo < V_{CC}+0.5V$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		1.2	3.6	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0 0 0 0	1000 700 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}, V	Guaranteed Limit						Unit
				25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
				min	max	min	max	min	max	
V_{IH}	High-Level Input Voltage		1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	V
V_{IL}	Low -Level Input Voltage		1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	V
V_{OH}	High-Level Output Voltage	$V_I = V_{IL}$ or V_{IH} I_O = -50 µÀ	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	V
		$V_I = V_{IL}$ or V_{IH} I_O = -6.0 mÀ	3.0	2.48	-	2.34	-	2.20	-	V
V_{OL}	Low-Level Output Voltage	$V_I = V_{IL}$ or V_{IH} I_O = 50 µÀ	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.1	- - - -	0.1 0.1 0.1 0.1	V
		$V_I = V_{IL}$ or V_{IH} I_O = 6.0 mÀ	3.0	-	0.33	-	0.4	-	0.5	V
I_{IL}	Low-Level Input Leakage Current	V_I = 0 V	3.6	-	-0.1	-	-1.0	-	-1.0	µA
$I_{Ií}$	High-Level Input Leakage Current	$V_I = V_{CC}$	3.6	-	0.1	-	1.0	-	1.0	µA
$I_{ÑÑ}$	Quiescent Supply Current (per Package)	V_I = 0 Â or V_{CC} I_O = 0 µÀ	3.6	-	2.0	-	20	-	40	µA

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, $t_{LH} = t_{HL}$ = 6.0 ns, V_{IL}=0V, $V_{IH}=V_{CC}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit						Unit
			25°C		-40°C ? 85°C		-40°C ? 125°C		
			min	max	min	max	min	max	
t_{THL}, (t_{TLH})	Output Transition Time, Any Output (Figure 1)	1.2	-	60	-	75	-	90	ns
		2.0	-	16	-	20	-	24	
		*		10	-	13	-	15	
t_{PHL}, (t_{PLH})	Propagation Delay, Input A to Output Y (Figure 1)	1.2	-	135	-	405	-	405	
		2.0	-	23	-	28	-	34	
		*	-	14	-	18	-	21	
C_I	Input Capacitance	3.0	-	7.0	-	-	-	-	pF

C_{PD}	Power Dissipation Capacitance (Per Inverter)	ÒÀ=25°Ñ, V_I=0V?V_{CC}	pF
		44	

* - V_{CC}= (3.3±0.3) V

Used to determine the no-load dynamic power consumption:
$P_D = C_{PD}V_{CC}^2f_I + ?(C_LV_{CC}^2fo)$, f_I-input frequency, fo- output frequency (MHz)

$?(C_LV_{CC}^2fo)$ – sum of the outputs

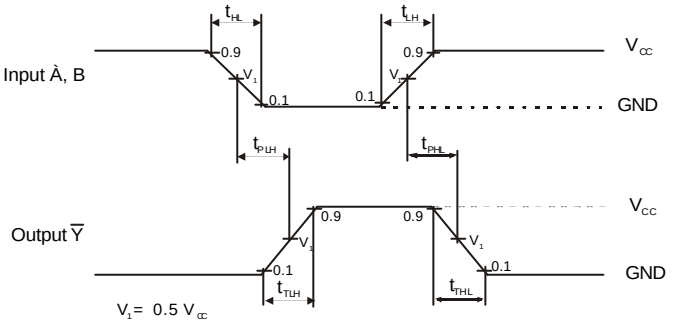
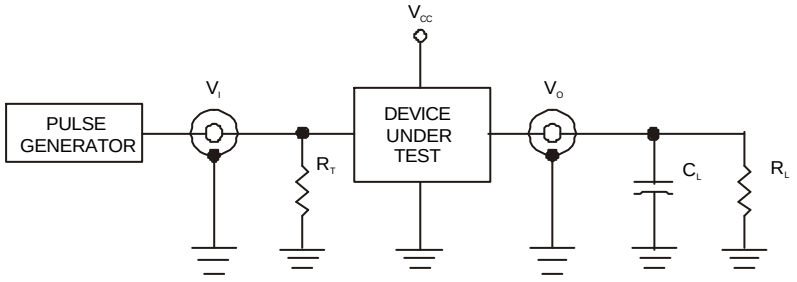


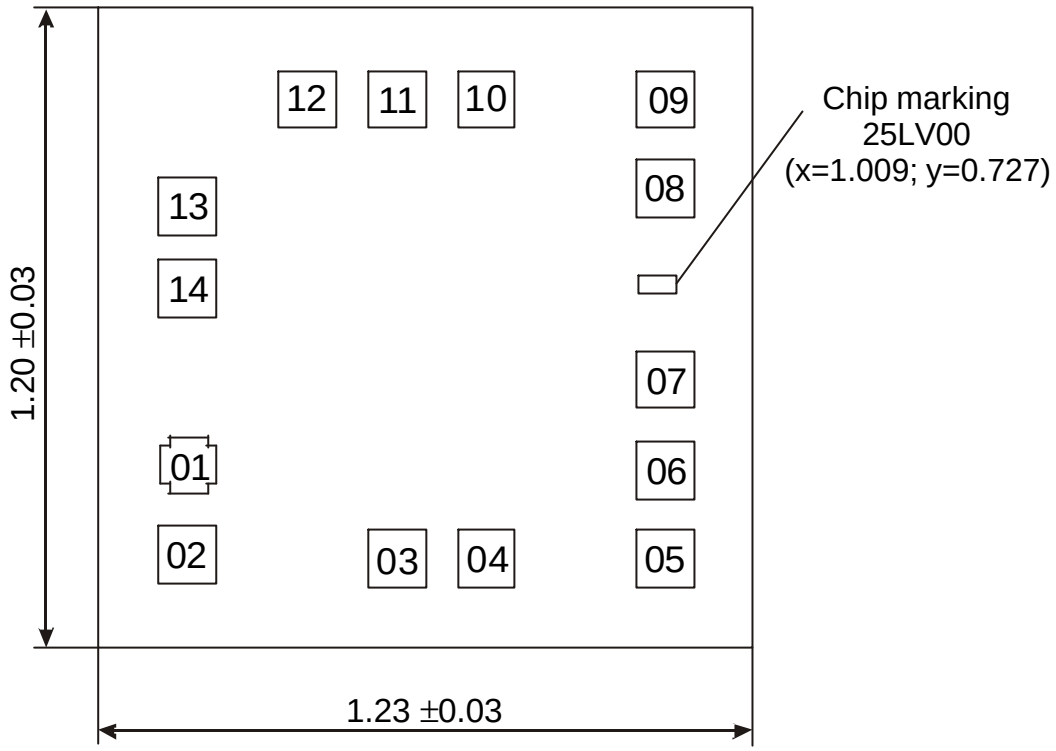
Figure 1. Switching Waveforms



Termination resistance R_T - should be equal to Z_{OUT} pulse generators

Figure 2. Test Circuit

CHIP PAD DIAGRAM IZ74LV00



Pad size 0.108 x 0.108 mm (Pad size is given as per metallization layer)
Thickness of chip 0.46 ± 0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	A1	0.111	0.287
02	B1	0.111	0.119
03	Y1	0.504	0.111
04	A2	0.672	0.111
05	B2	1.009	0.111
06	Y2	1.009	0.277
07	GND	1.009	0.447
08	Y3	1.009	0.806
09	A3	1.009	0.974
10	B3	0.672	0.974
11	Y4	0.504	0.974
12	A4	0.336	0.974
13	B4	0.111	0.772
14	Vcc	0.111	0.618