IW4053B

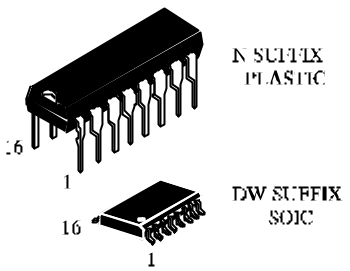
Analog Multiplexer Demultiplexer
High-Performance Silicon-Gate CMOS

The IW4053B analog multiplexer/demultiplexer is digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20V (if V_{CC} - GND = 3V, a V_{CC} - V_{EE} of up to 13 V can be controlled; for V_{CC} - V_{EE} level differences above 13V a V_{CC} - GND of at least 4.5V is required).

These multiplexer circuits dissipate extremely low quiescent power over the full V_{CC} -GND and V_{CC} - V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1"is present at the ENABLE input terminal all channels are off.

The IW4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an enable input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply

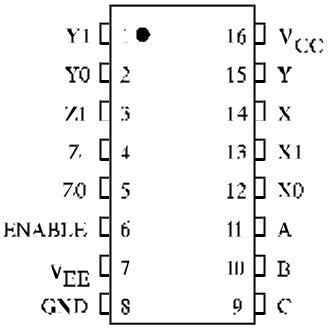


ORDERING INFORMATION

IW4053BN	Plastic DIP
IW4053BD	SOIC
IZ4053B	chip

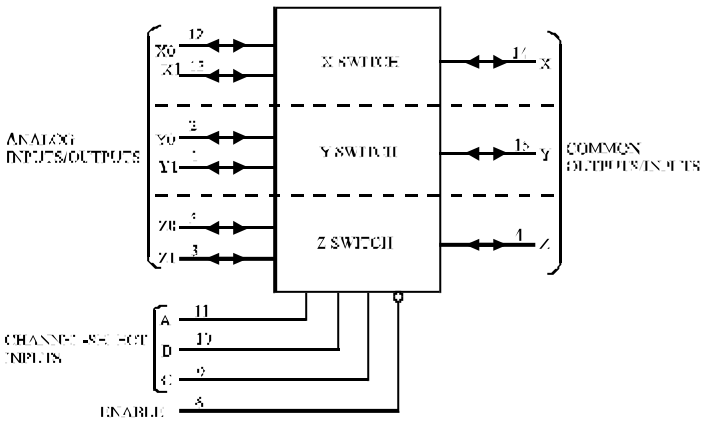
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM

Triple Single-Pole, Double-Position
Plus Common Off



PIN 16 =V_{CC}
PIN 7 = V_{EE}
PIN 8 = GND

FUNCTION TABLE

Control Inputs				ON Channels		
Enable	Select					
	C	B	A			
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	None		

H = high level
L = low level
X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air	500*[1]	mW
P_{tot}	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SO Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*[1] - for Plastic DIP from -55° to +100°C, for SO Package from -55° to +65°C.
+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SO Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}	DC Input Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused digital pins must be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated.

DC ELECTRICAL CHARACTERISTICS Digital Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ³ -55 °C	Guaranteed Limit £ 25 °C	Guaranteed Limit £ 125 °C	Unit
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$V_{IS}=V_{CC}$ thru 1kΩ V_{EE}=GND=0 I_{IS}<2μA on all OFF Chanels R_L=1kΩ to GND	5 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs	$V_{IS}=V_{CC}$ thru 1kΩ V_{EE}=GND=0 I_{IS}<2μA on all OFF Chanels R_L=1kΩ to GND	5 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
I_{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{IN}=V_{CC}$ or GND V_{EE}=GND=0	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V_{CC} or GND V_{EE}=GND=0	5 10 15 20	5 10 20 100	5 10 20 100	150 300 600 3000	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ³ -55 °C	Guaranteed Limit £ 25 °C	Guaranteed Limit £ 125 °C	Unit
R_{ON}	Maximum "ON" Resistance	V_{EE}=GND=0 V_{IS} = GND to V_{CC}	5 10 15	800 310 200	1050 400 240	1150 550 320	Ω
ΔR_{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V_{EE}=GND=0	5 10 15	- - -	10* 15* 5*	- - -	Ω
I_{OFF}	Maximum Off- Channel Leakage Current, Any One Channel	V_{EE}=GND=0	18	±100	±100	±1000	nA
	Maximum Off- Channel Leakage Current, Common Channel	V_{EE}=GND=0	18	±100	±100	±1000	

* - Typical Value

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=20.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ³ -55 °C	Guaranteed Limit £ 25 °C	Guaranteed Limit £ 125 °C	Unit
t_{PHL}(t_{PLH})	Maximum Propagation Delay , Analog Input to Analog Output (Figure 1) R_L=200kΩ, V_{EE}=GND=0	5 10 15	60 30 20	60 30 20	70 40 30	ns
t_{PHL1}(t_{PLH1})	Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 1) R_L=200 kΩ, V_{EE}=GND=0	5 10 15	350 200 160	350 200 160	400 250 200	ns
t_{PZL1}(t_{PZH1})	Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 2) R_L=10 kΩ V_{EE}=GND=0	5 10 15	720 320 240	720 320 240	720 320 240	ns
	V_{EE}=-5Â, GND=0	5	450	450	450	
t_{PZL2}(t_{PZH2})	Maximum Propagation Delay , Enable to Analog Output (Figure 2) R_L=10 kΩ V_{EE}=GND=0	5 10 15	720 320 240	720 320 240	720 320 240	ns
	V_{EE}=-10Â, GND=0	5	400	400	400	
t_{PLZ1}(t_{PHZ1})	Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 2) R_L=10 kΩ V_{EE}=GND=0	5 10 15	720 320 240	720 320 240	720 320 240	ns
	V_{EE}=-5Â, GND=0	5	450	450	450	
t_{PLZ2}(t_{PHZ2})	Maximum Propagation Delay , Enable to Analog Output (Figure 2) R_L=1,0 kΩ V_{EE}=GND=0	5 10 15	450 210 160	450 210 160	450 210 160	ns
	V_{EE}=-10Â, GND=0	5	300	300	600	
C_{IN}	Maximum Input Capacitance, Channel-Select or Enable Inputs	-	-	7.5	-	pF
$C_{I/O}$	Maximum Capacitance V_{EE}=GND=-5V C_{IS}	5	-	5*	-	pF
	C_{OS}	5	-	9*	-	
	Feedthrough C_{IOS}	5	-	0.2*	-	

ADDITIONAL APPLICATION CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	V_{IS}** V	Limits Typical Value 25 °C	Unit
B_W	Maximum On-Channel Bandwidth or Minimum Frequency Response (-3db)	V_{EE}=GND=0 R_L=1kΩ 20 log(V_{OS}/V_{IS})=-3db V_{OS} at Common OUT/IN	10	2,5	30	MHz
		V_{OS} at Any Channel	10	2,5	60	
f_1	(-40db) Feedthrough Frequency (All Channels OFF)	V_{EE}=GND=0 R_L=1kΩ 20 log(V_{OS}/V_{IS})=-40db V_{OS} at Common OUT/IN	10	2,5	8	MHz
		V_{OS} at Any Channel	10	2,5	8	
f_2	(-40db) Signal Crosstalk Frequency	V_{EE}=GND=0 R_L=1kΩ 20 log(V_{OS}/V_{IS})=-40db Between any 2 Sections : In Pin 2, Out Pin 14 In Pin 15, Out Pin 14	 10 10	 2,5 2,5	 2.5 6	MHz
THD	Total Harmonic Distortion	V_{EE}=GND=0 f_{IS}=1kHz sine wave	5 10 15	1 1,5 2,5	0.3 0.2 0.12	%
$V_{AO/I}$	Address-or Enable to Signal Crosstalk	V_{EE}=GND=0, R_L=10kΩ*** t_r,t_f=20ns Square Wave	10	-	65	mV (Peak)

** Peak-to-peak voltage symmetrical about (V_{CC}-V_{EE})/2.

*** Both ends of channel.

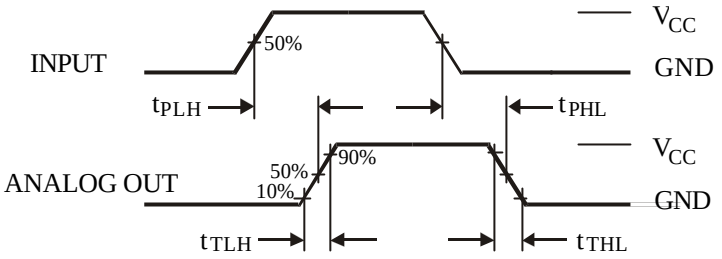


Figure 1. Switching Waveforms

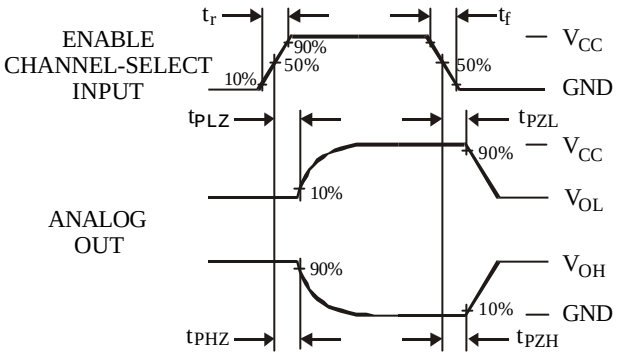
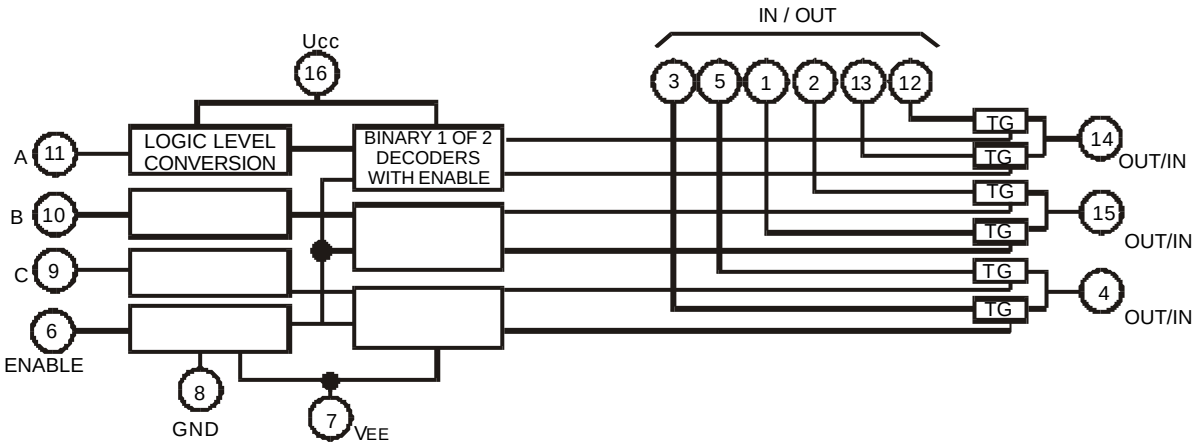
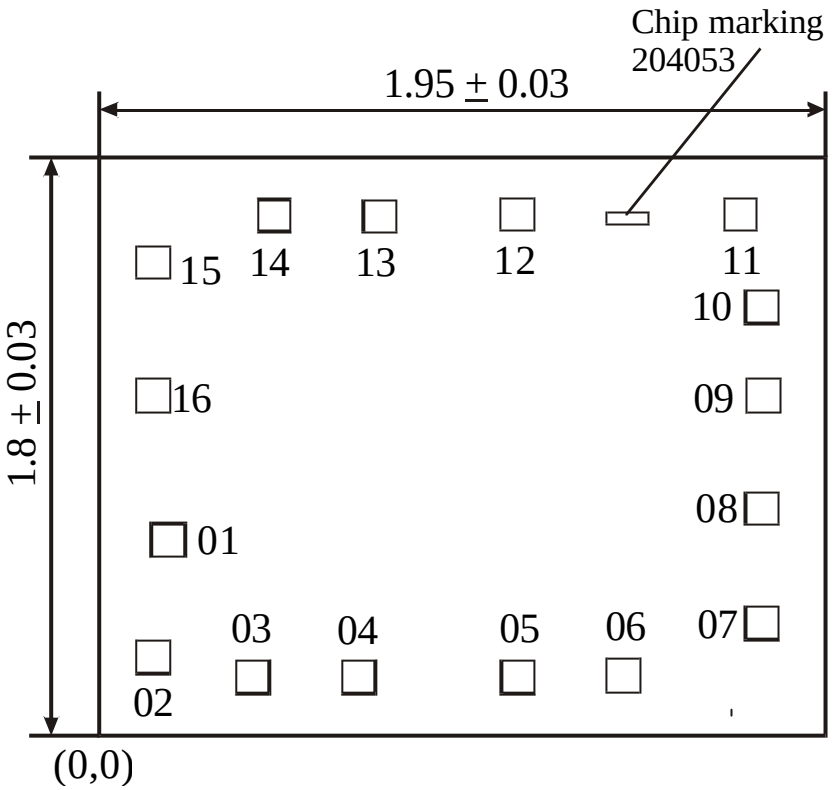


Figure 2. Switching Waveforms

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=1.361, y=1.592; right higher corner x=1.423, y=1.652.
Chip thickness: 0.46±0.02mm
PAD LOCATION

Pad No	Pin No	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	01	0.116	0.453	0.100 x 0.100
02	02	0.116	0.175	0.100 x 0.100
03	03	0.362	0.116	0.100 x 0.100
04	04	0.669	0.116	0.100 x 0.100
05	05	1.074	0.116	0.100 x 0.100
06	06	1.287	0.115	0.100 x 0.100
07	07	1.699	0.290	0.100 x 0.100
08	08	1.699	0.620	0.100 x 0.100
09	09	1.699	0.973	0.100 x 0.100
10	10	1.700	1.268	0.100 x 0.100
11	11	1.640	1.583	0.100 x 0.100
12	12	1.063	1.583	0.100 x 0.100
13	13	0.756	1.583	0.100 x 0.100
14	14	0.429	1.583	0.100 x 0.100
15	15	0.116	1.445	0.100 x 0.100
16	16	0.116	0.942	0.100 x 0.100

Note: Pad location is given as per passivation layer