

IRLR8711CPbF

Applications

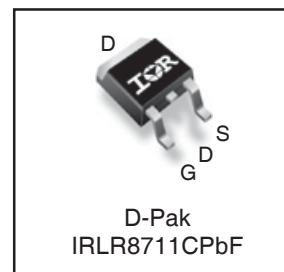
- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification

HEXFET® Power MOSFET

V_{DS}	$R_{DS(on)}$ max	Qg
25V	5.6mΩ	13nC

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	84④	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	60④	
I_{DM}	Pulsed Drain Current ①	340	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation ⑤	68	W
$P_D @ T_C = 100^\circ\text{C}$	Maximum Power Dissipation ⑤	34	
	Linear Derating Factor	0.45	W/°C
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	2.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤⑥	—	50	
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	110	

Notes ① through ⑥ are on page 10

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	16	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.5	5.6	mΩ	$V_{GS} = 10V, I_D = 21A$ ③
		—	6.2	7.8		$V_{GS} = 4.5V, I_D = 17A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	$V_{DS} = V_{GS}, I_D = 50\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.3	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	86	—	—	S	$V_{DS} = 13V, I_D = 17A$
Q_g	Total Gate Charge	—	13	20	nC	$V_{DS} = 13V$ $V_{GS} = 4.5V$ $I_D = 17A$ See Fig.16
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	3.0	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.9	—		
Q_{gd}	Gate-to-Drain Charge	—	4.3	—		
Q_{godr}	Gate Charge Overdrive	—	3.8	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	6.2	—		
Q_{oss}	Output Charge	—	6.4	—	nC	$V_{DS} = 10V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.5	3.4	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	9.7	—	ns	$V_{DD} = 13V, V_{GS} = 4.5V$ ③ $I_D = 17A$ Clamped Inductive Load
t_r	Rise Time	—	29	—		
$t_{d(off)}$	Turn-Off Delay Time	—	10	—		
t_f	Fall Time	—	4.4	—		
C_{iss}	Input Capacitance	—	1640	—	pF	$V_{GS} = 0V$ $V_{DS} = 13V$ $f = 1.0MHz$
C_{oss}	Output Capacitance	—	430	—		
C_{rss}	Reverse Transfer Capacitance	—	210	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	47	mJ
I_{AR}	Avalanche Current ①	—	17	A
E_{AR}	Repetitive Avalanche Energy ①	—	6.8	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	84 ④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	340		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 17A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	13	20	ns	$T_J = 25^\circ\text{C}, I_F = 17A, V_{DD} = 13V$
Q_{rr}	Reverse Recovery Charge	—	8.0	12	nC	$di/dt = 300A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

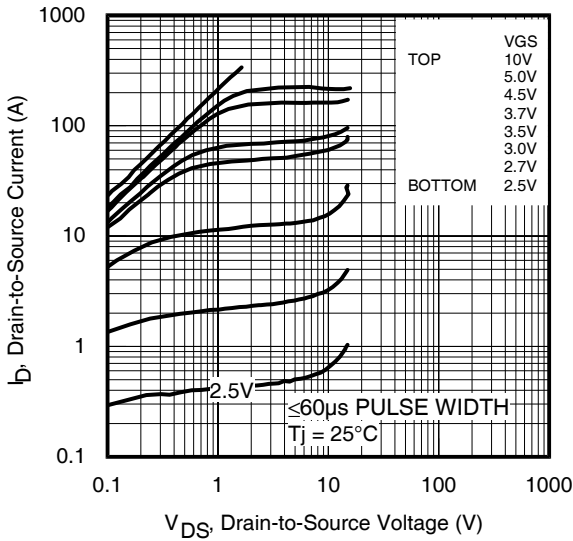


Fig 1. Typical Output Characteristics

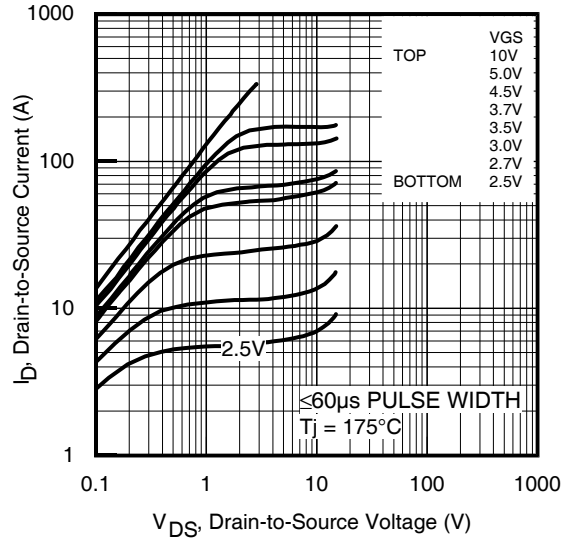


Fig 2. Typical Output Characteristics

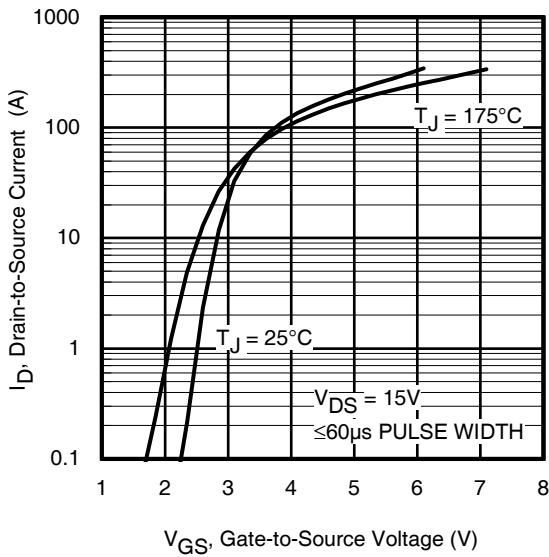


Fig 3. Typical Transfer Characteristics

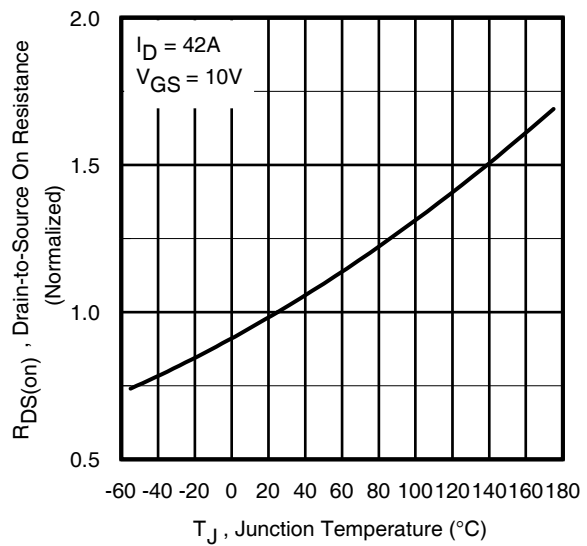


Fig 4. Normalized On-Resistance vs. Temperature

IRLR8711CPbF

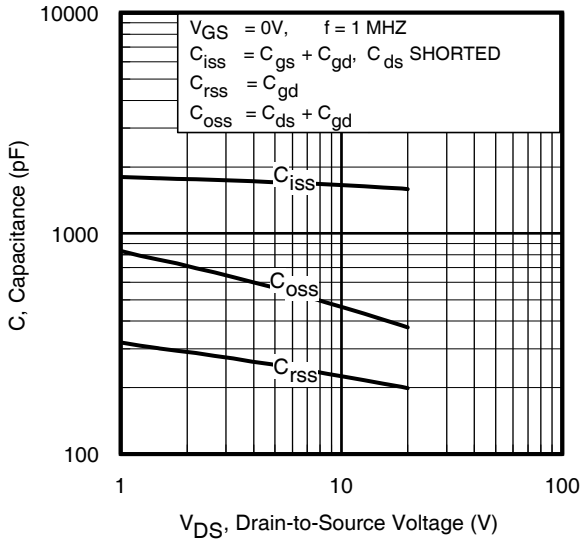


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

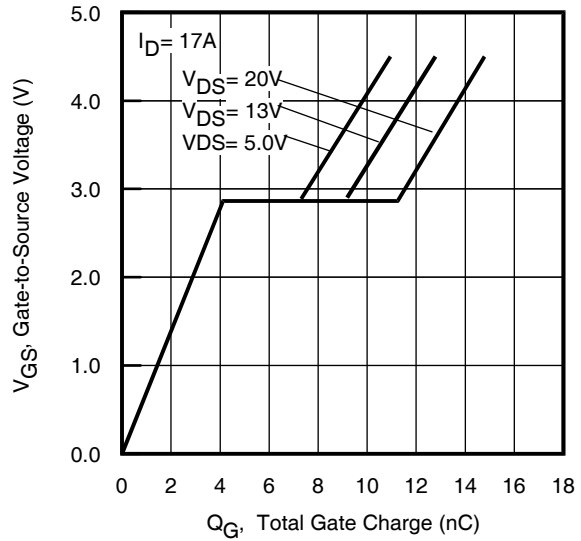


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

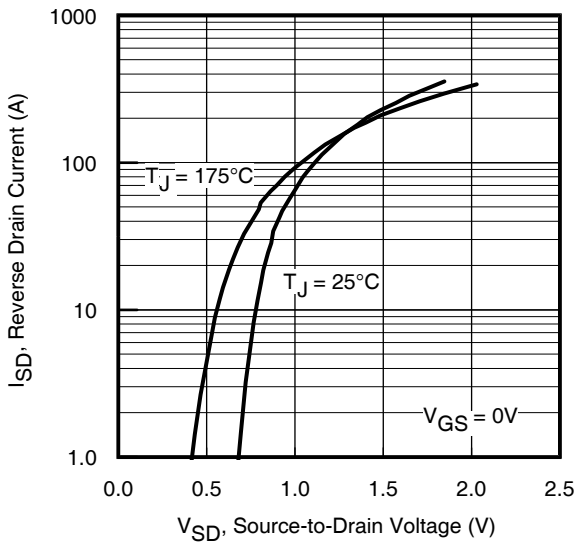


Fig 7. Typical Source-Drain Diode Forward Voltage

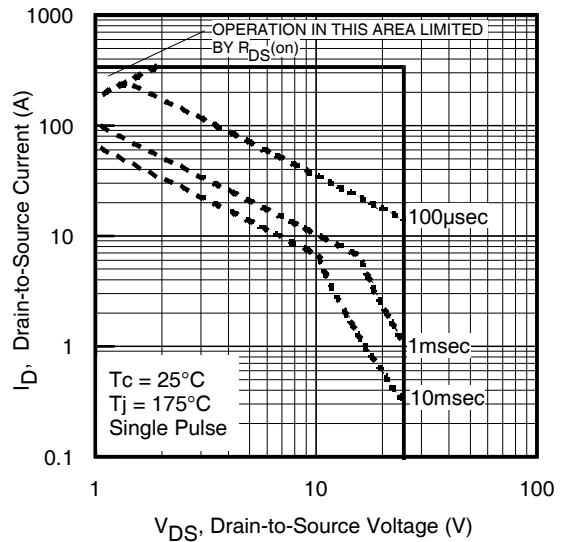


Fig 8. Maximum Safe Operating Area

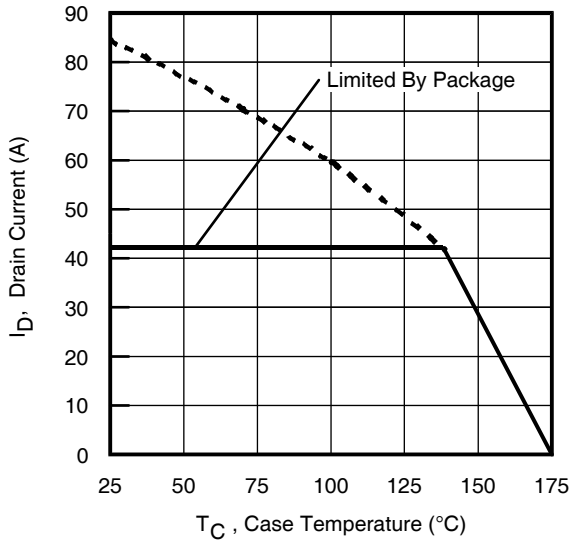


Fig 9. Maximum Drain Current vs. Case Temperature

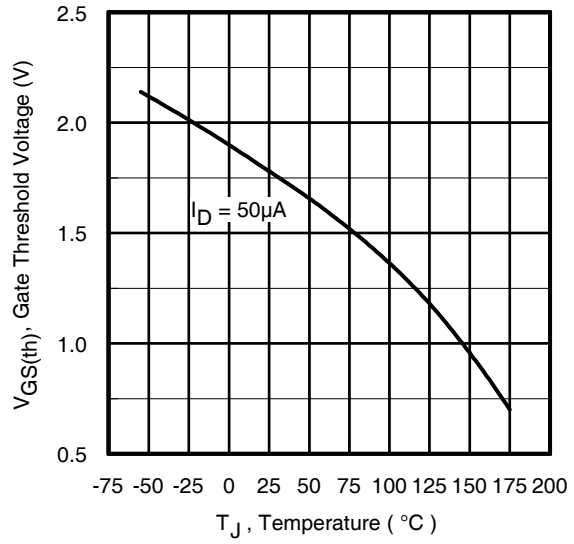


Fig 10. Threshold Voltage vs. Temperature

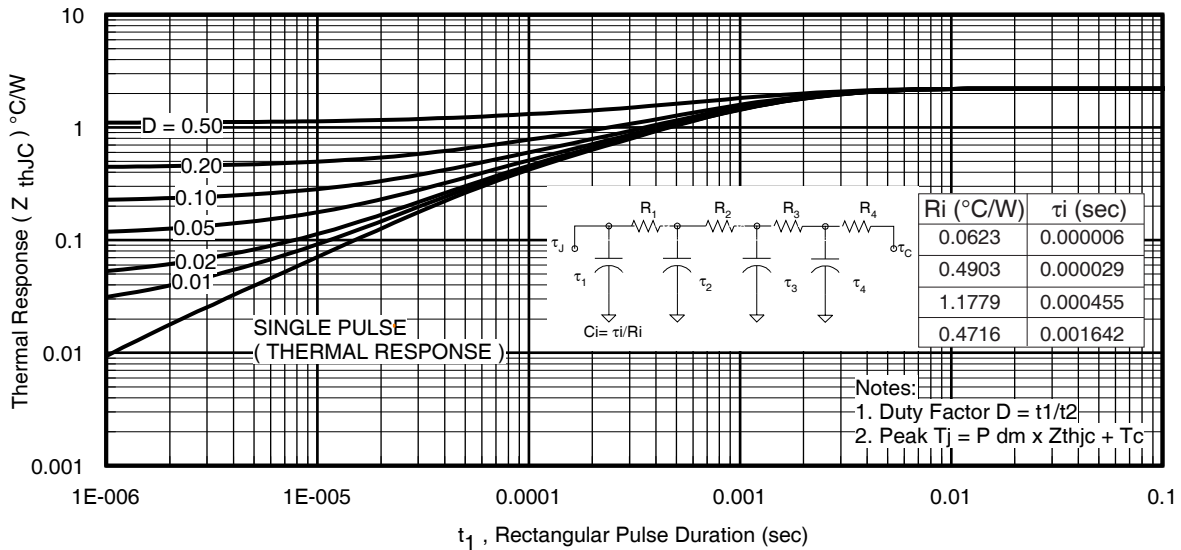


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRLR8711CPbF

International
IR Rectifier

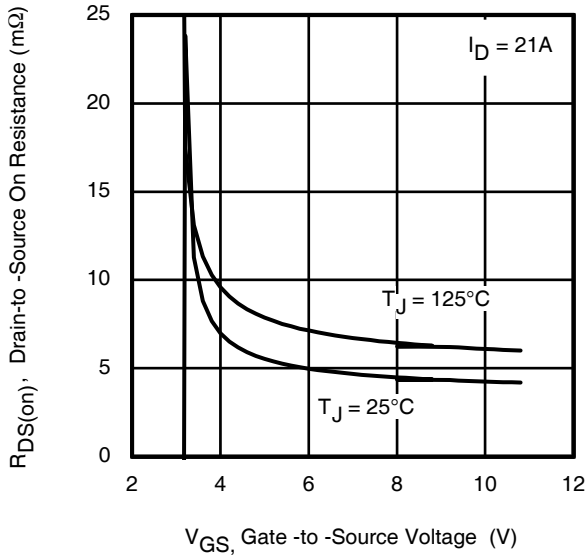


Fig 12. On-Resistance vs. Gate Voltage

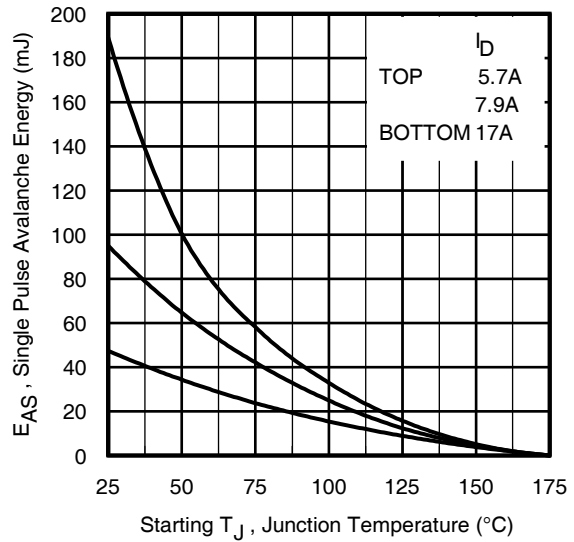


Fig 13. Maximum Avalanche Energy vs. Drain Current

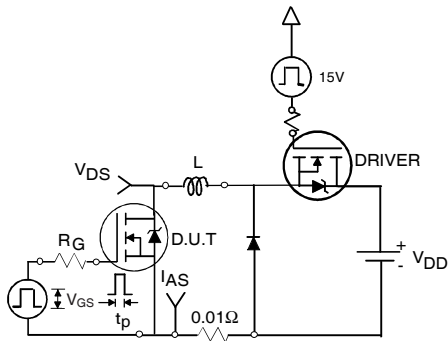


Fig 14a. Unclamped Inductive Test Circuit

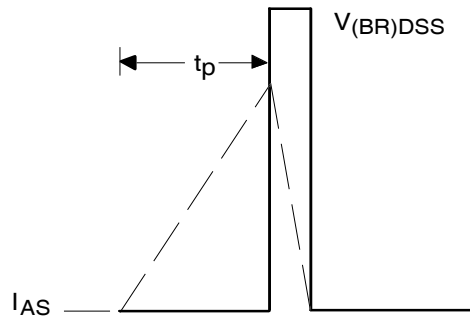


Fig 14b. Unclamped Inductive Waveforms

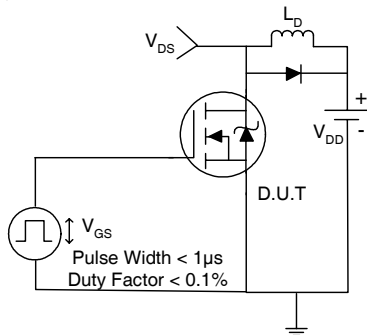


Fig 15a. Switching Time Test Circuit

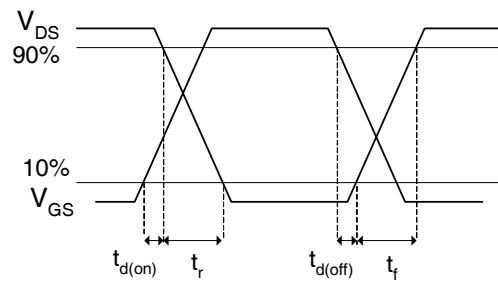


Fig 15b. Switching Time Waveforms

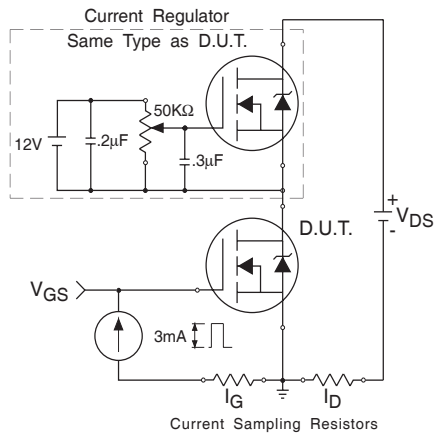


Fig 16a. Gate Charge Test Circuit

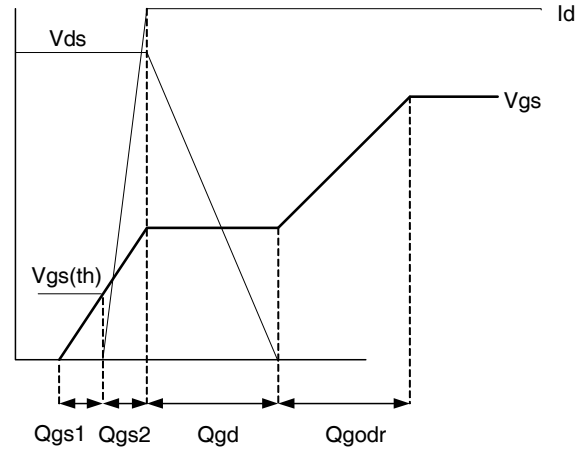
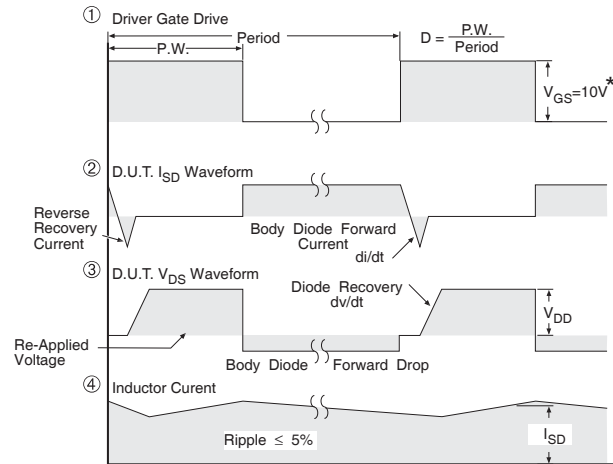
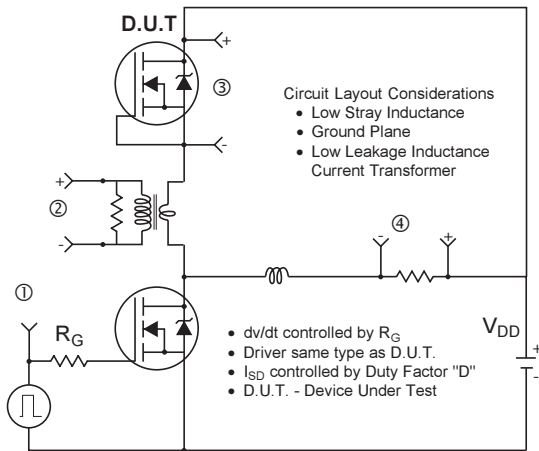


Fig 16b. Gate Charge Waveform



* $V_{GS} = 5V$ for Logic Level Devices

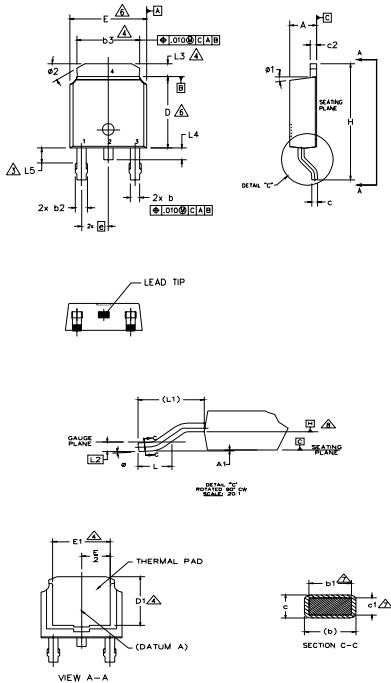
Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

IRLR8711CPbF

International
IR Rectifier

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
 - 3.- LEAD DIMENSION UNCONTROLLED IN L5.
 - 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
 - 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 - 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
 - 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFEEET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

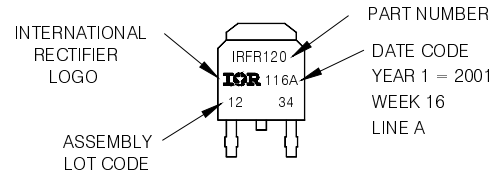
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

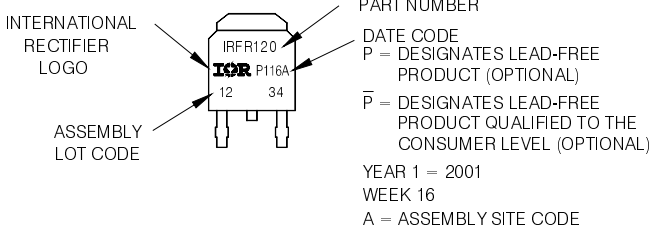
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position
indicates 'Lead-Free'

'P̄' in assembly line position indicates
'Lead-Free' qualification to the consumer-level

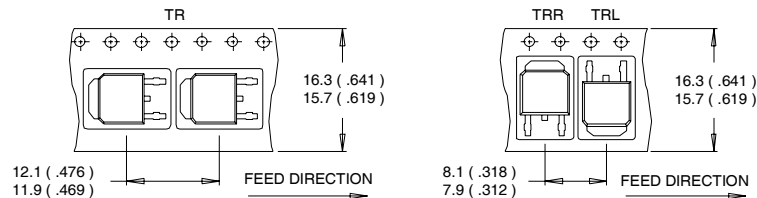


OR

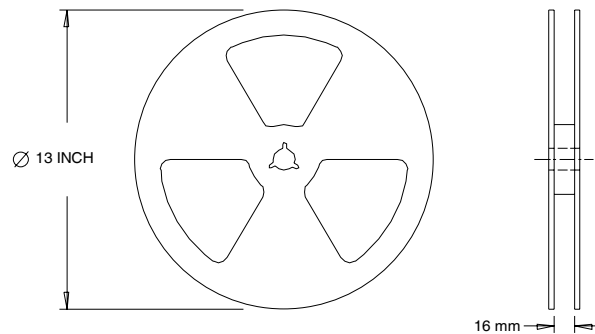


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.34\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 17\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ R_θ is measured at T_J approximately at 90°C .

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualification Standards can be found on IR's Web site.