PD-97062

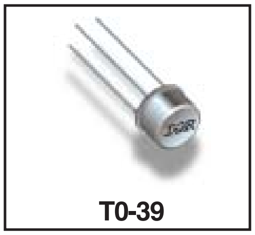
International
IOR Rectifier

# RADIATION HARDENED LOGIC LEVEL POWER MOSFET THRU-HOLE (TO-39)

**IRHLF77110**
**100V, N-CHANNEL**
**R7™ TECHNOLOGY**

## Product Summary

| Part Number | Radiation Level | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| IRHLF77110 | 100K Rads (Si) | 0.30Ω | 6.0A |
| IRHLF73110 | 300K Rads (Si) | 0.30Ω | 6.0A |



**T0-39**

International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

## Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

## Absolute Maximum Ratings

**Pre-Irradiation**

|  | Parameter |  | Units |
|---|---|---|---|
| $I_D$ @ $V_{GS}$ = 4.5V, $T_C$=25°C | Continuous Drain Current | 6.0 | A |
| $I_D$ @ $V_{GS}$ = 4.5V, $T_C$=100°C | Continuous Drain Current | 3.7 |  |
| $I_{DM}$ | Pulsed Drain Current ① | 24 |  |
| $P_D$ @ $T_C$ = 25°C | Max. Power Dissipation | 23 | W |
|  | Linear Derating Factor | 0.18 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±10 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 43 | mJ |
| $I_{AR}$ | Avalanche Current ① | 6.0 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 2.3 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 4.9 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction<br>Storage Temperature Range | -55 to 150 | °C |
|  | Lead Temperature | 300 (0.063in/1.6mm from case for 10s) |  |
|  | Weight | 0.98 (Typical) | g |

For footnotes refer to the last page

## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta BV_{DSS}/\Delta T_J$ | Temperature Coefficient of Breakdown Voltage | — | 0.10 | — | V/°C | Reference to 25°C, $I_D$ = 1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-State Resistance | — | — | 0.30 | Ω | $V_{GS}$ = 4.5V, $I_D$ = 3.7A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 2.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Coefficient | — | -5.7 | — | mV/°C | |
| $g_{fs}$ | Forward Transconductance | 3.0 | — | — | S | $V_{DS}$ = 10V, $I_{DS}$ = 3.7A ④ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | — | 1.0 | µA | $V_{DS}$= 80V ,$V_{GS}$= 0V |
| | | — | — | 10 | | $V_{DS}$ = 80V,<br>$V_{GS}$ = 0V, $T_J$ =125°C |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | — | 100 | nA | $V_{GS}$ = 10V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | — | -100 | | $V_{GS}$ = -10V |
| $Q_g$ | Total Gate Charge | — | — | 9.0 | nC | $V_{GS}$ = 4.5V, $I_D$ = 6.0A<br>$V_{DS}$ = 50V |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 3.2 | | |
| $Q_{gd}$ | Gate-to-Drain ('Miller') Charge | — | — | 4.8 | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | — | 12 | ns | $V_{DD}$ = 50V, $I_D$ = 6.0A,<br>$V_{GS}$ = 5.0V, $R_G$ = 7.5Ω |
| $t_r$ | Rise Time | — | — | 83 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | — | 34 | | |
| $t_f$ | Fall Time | — | — | 8.0 | | |
| $L_S + L_D$ | Total Inductance | — | 7.0 | — | nH | Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.)with Source wire internally bonded from Source pin to Drain pad |
| $C_{iss}$ | Input Capacitance | — | 577 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V<br>f = 1.0MHz |
| $C_{oss}$ | Output Capacitance | — | 117 | — | | |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 1.6 | — | | |
| $R_g$ | Gate Resistance | — | 6.6 | — | Ω | f = 1.0MHz, open drain |

## Source-Drain Diode Ratings and Characteristics

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 6.0 | A | |
| $I_{SM}$ | Pulse Source Current (Body Diode) ① | — | — | 24 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.2 | V | $T_j$ = 25°C, $I_S$ = 6.0A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | — | 260 | ns | $T_j$ = 25°C, $I_F$ = 6.0A, di/dt ≤ 100A/µs<br>$V_{DD}$ ≤ 25V ④ |
| $Q_{RR}$ | Reverse Recovery Charge | — | — | 904 | nC | |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S$ + $L_D$. | | | | |

## Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{thJC}$ | Junction-to-Case | — | — | 5.5 | °C/W | |

**Note: Corresponding Spice and Saber models are available on International Rectifier Web site.**

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

| | Parameter | Up to 300K Rads(Si)[1] | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 100 | — | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | 2.0 | | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA |
| $I_{GSS}$ | Gate-to-Source Leakage Forward | — | 100 | nA | $V_{GS}$ = 10V |
| $I_{GSS}$ | Gate-to-Source Leakage Reverse | — | -100 | | $V_{GS}$ = -10V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | — | 1.0 | μA | $V_{DS}$= 80V, $V_{GS}$= 0V |
| $R_{DS(on)}$ | Static Drain-to-Source ④<br>On-State Resistance (TO-39) | — | 0.30 | Ω | $V_{GS}$ = 4.5V, $I_D$ = 3.7A |
| $V_{SD}$ | Diode Forward Voltage ④ | — | 1.2 | V | $V_{GS}$ = 0V, $I_D$ = 6.0A |

1. Part numbers IRHLF77110, IRHLF73110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Single Event Effect Safe Operating Area**

| Ion | LET | Energy | Range | VDS (V) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | (MeV/(mg/cm$^2$)) | (MeV) | (µm) | @VGS= 0V | @VGS= -1V | @VGS= -2V | @VGS= -4V | @VGS= -5V | @VGS= -6V | @VGS= -7V | @VGS= -8V |
| Br | 37 | 305 | 39 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| I | 60 | 370 | 34 | 100 | 100 | 100 | 100 | 100 | 100 | - | - |
| Au | 84 | 390 | 30 | 100 | 100 | 100 | 100 | 100 | - | - | - |

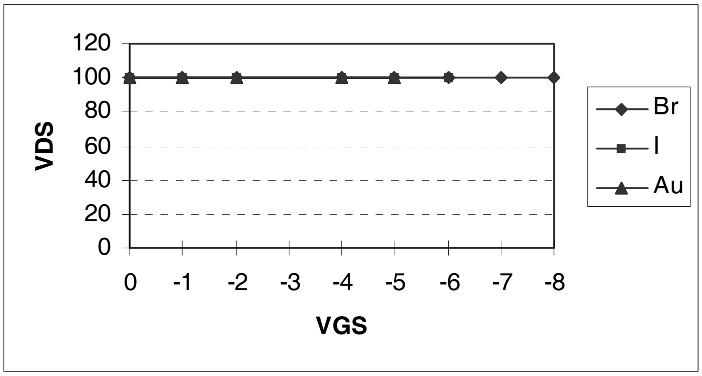


**Fig a.** Single Event Effect, Safe Operating Area

For footnotes refer to the last page

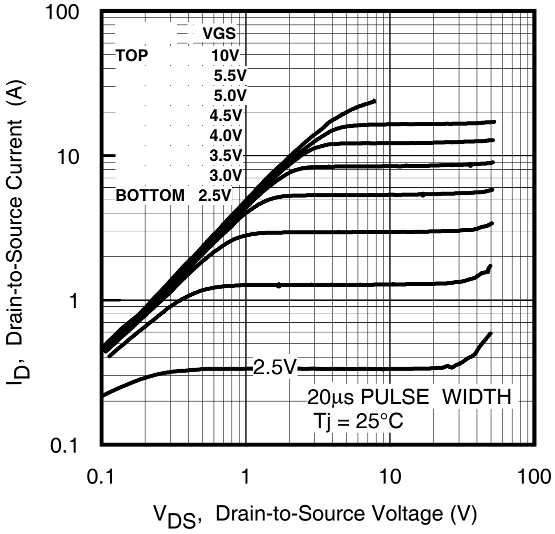


**Fig 1.** Typical Output Characteristics

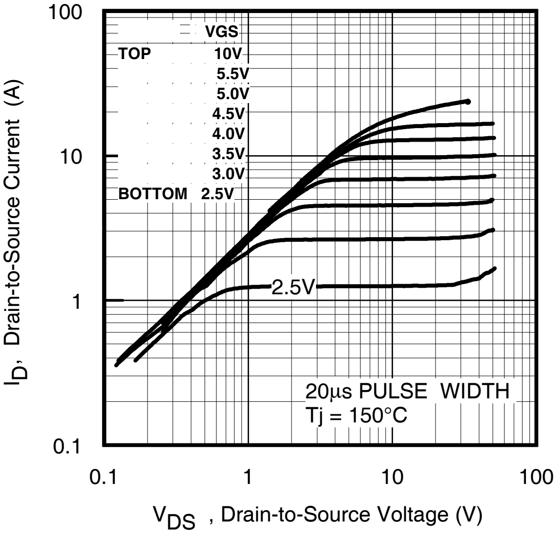


**Fig 2.** Typical Output Characteristics

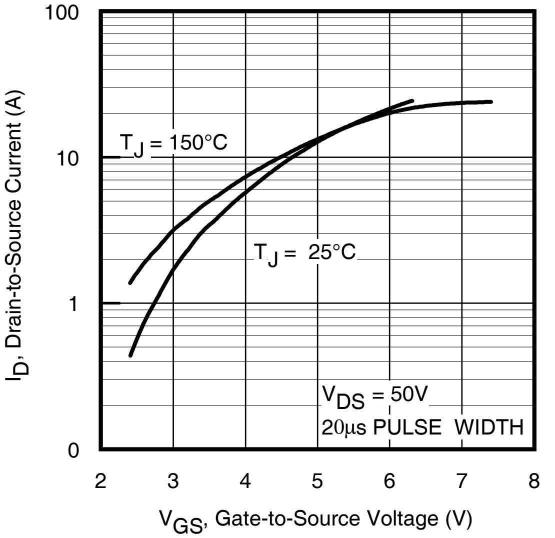


**Fig 3.** Typical Transfer Characteristics

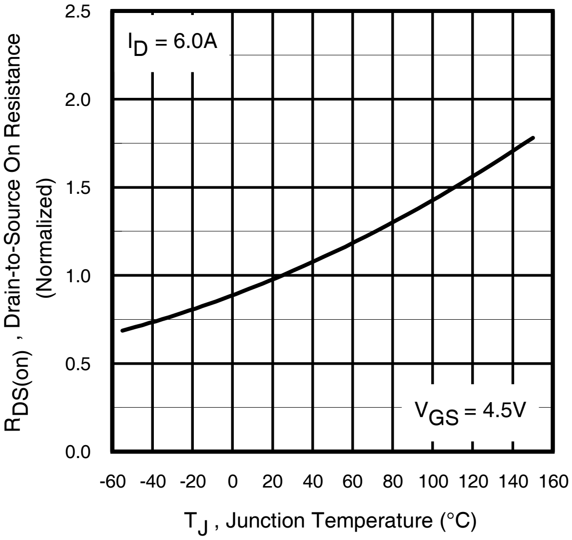


**Fig 4.** Normalized On-Resistance Vs. Temperature

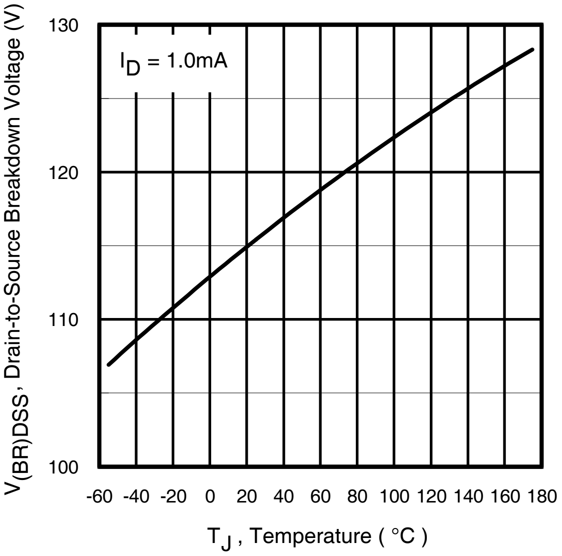


**Fig 5.** Typical Drain-to-Source Breakdown Voltage Vs Temperature

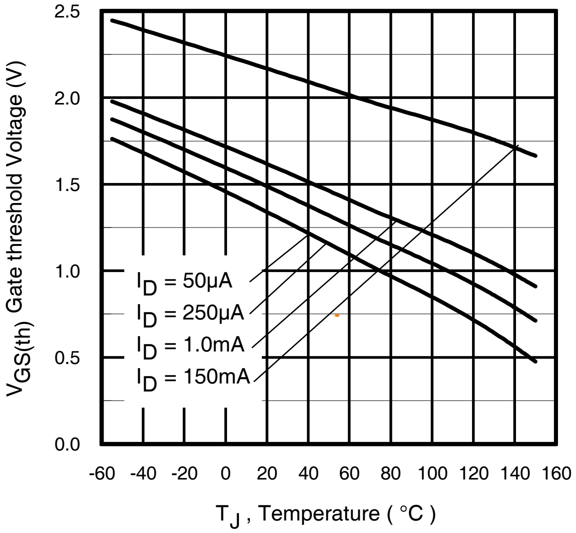


**Fig 6.** Typical Threshold Voltage Vs Temperature

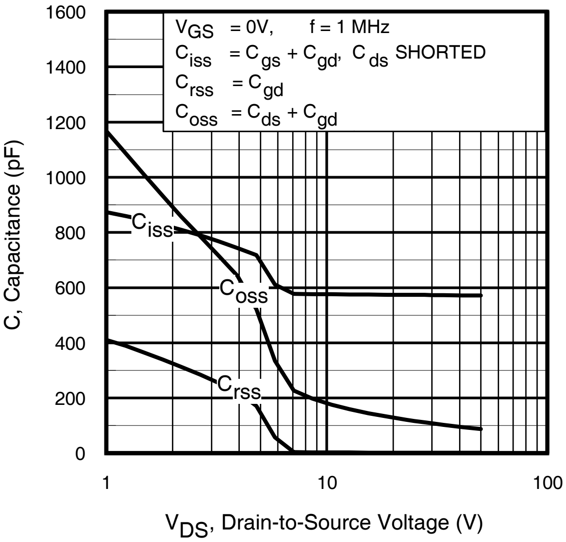


**Fig 7.** Typical Capacitance Vs. Drain-to-Source Voltage

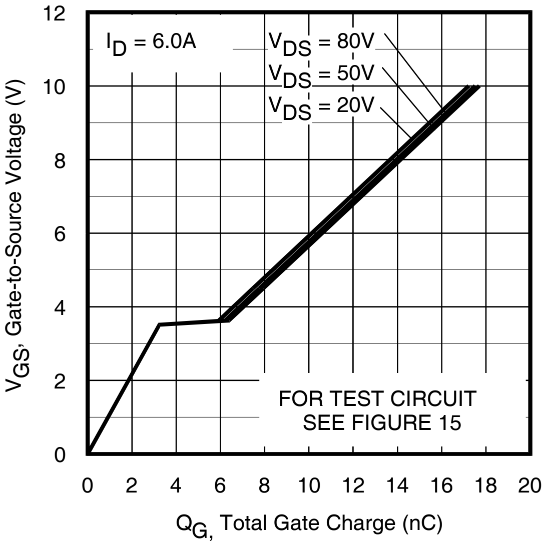


**Fig 8.** Typical Gate Charge Vs. Gate-to-Source Voltage

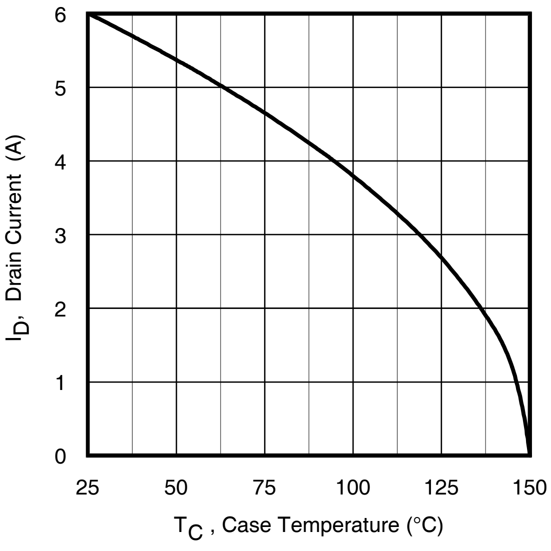


**Fig 9.** Maximum Drain Current Vs. Case Temperature

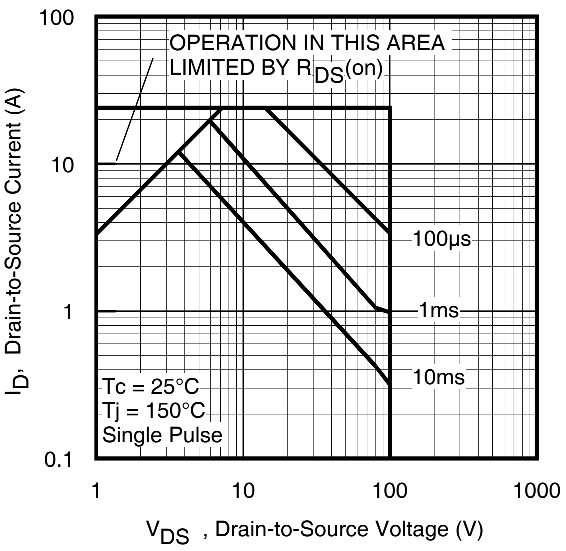


**Fig 10.** Maximum Safe Operating Area

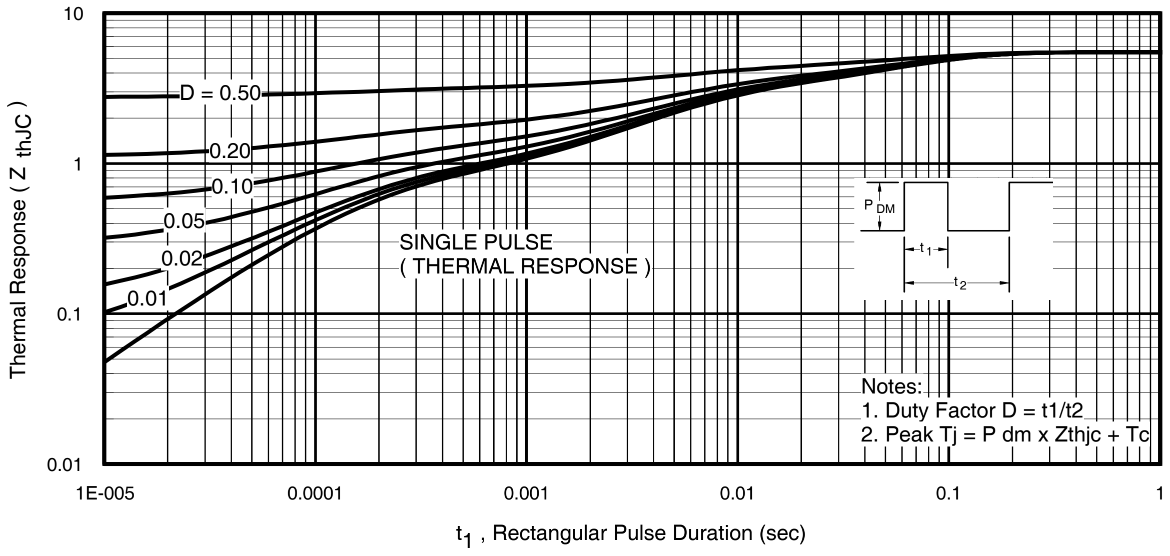


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

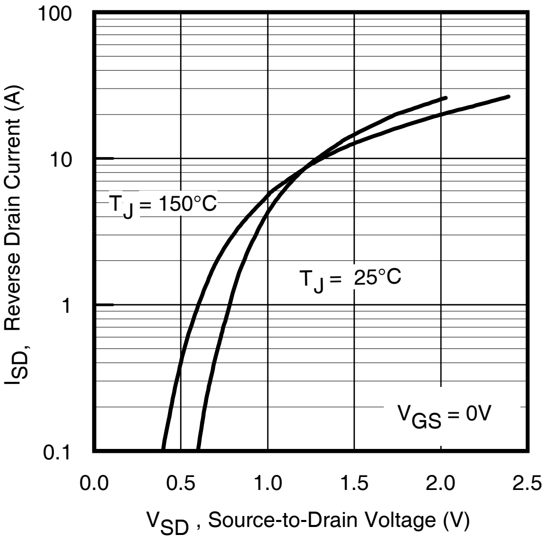


**Fig 12.** Typical Source-to-Drain Diode Forward Voltage

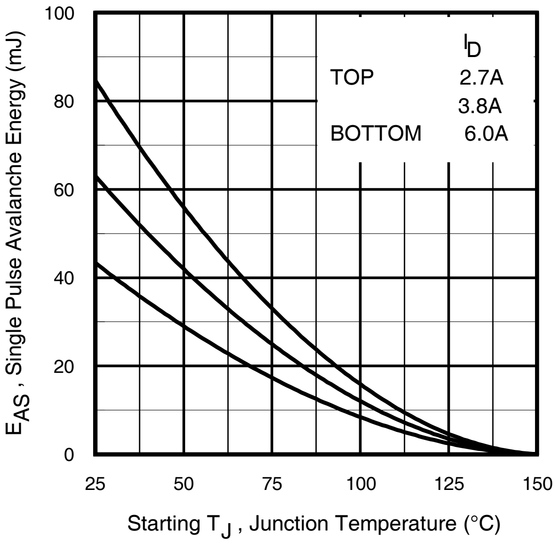


**Fig 13a** Maximum Avalanche Energy Vs. Drain Current

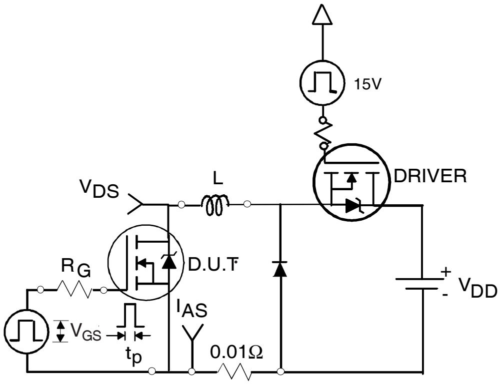


**Fig 13b.** Unclamped Inductive Test Circuit

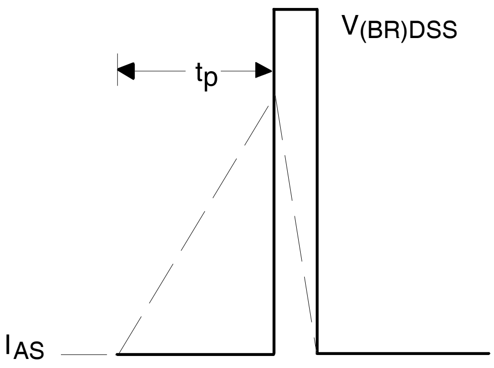


**Fig 13c.** Unclamped Inductive Waveforms

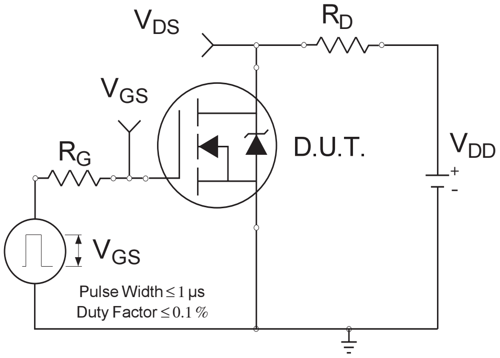


**Fig 14a.** Switching Time Test Circuit

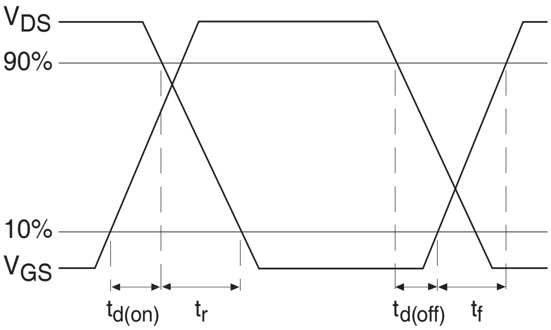


**Fig 14b.** Switching Time Waveforms

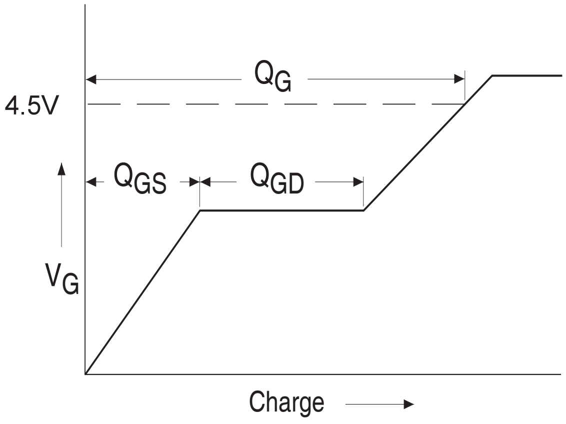


**Fig 15a.** Basic Gate Charge Waveform

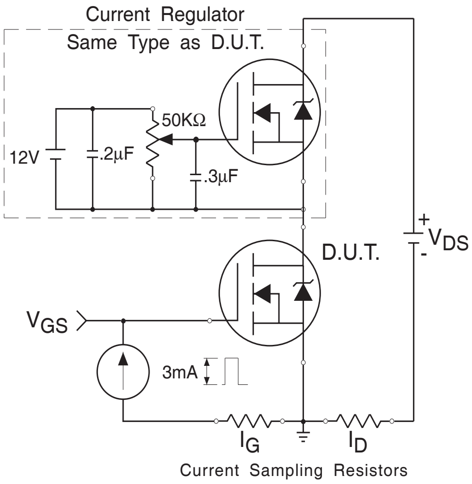


**Fig 15b.** Gate Charge Test Circuit

## Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② $V_{DD}$ = 25V, starting $T_J$ = 25°C, L= 2.4 mH
Peak $I_L$ = 6.0A, $V_{GS}$ = 10V

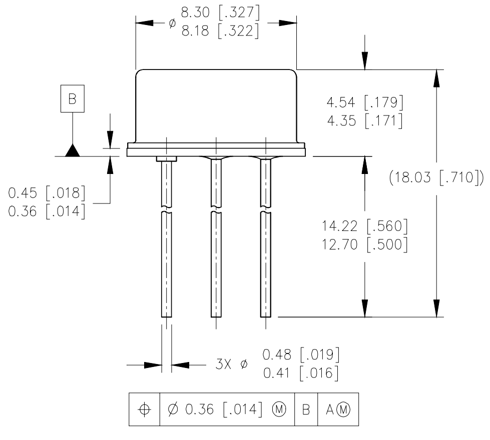
③ $I_{SD} \leq 6.0A$, $di/dt \leq 190A/\mu s$,
$V_{DD} \leq 100V$, $T_J \leq 150°C$

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

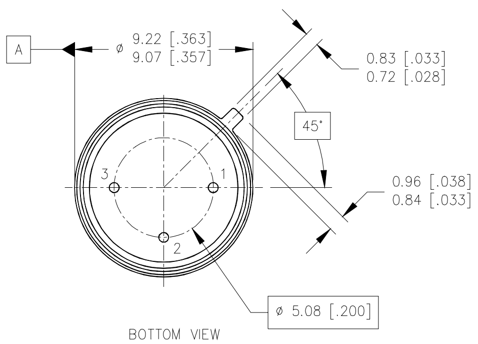
⑤ **Total Dose Irradiation with $V_{GS}$ Bias.**
10 volt $V_{GS}$ applied and $V_{DS}$ = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with $V_{DS}$ Bias.**
80 volt $V_{DS}$ applied and $V_{GS}$ = 0 during irradiation per MIL-STD-750, method 1019, condition A.

## Case Outline and Dimensions — TO-205AF (Modified TO-39)



SIDE VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND
1- SOURCE
2- GATE
3- DRAIN

International
IOR Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
**IR LEOMINSTER :** 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.
*Data and specifications subject to change without notice. 12/2006*