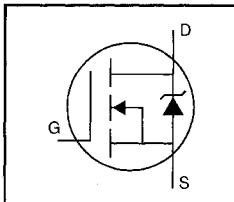


### HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 250V$$

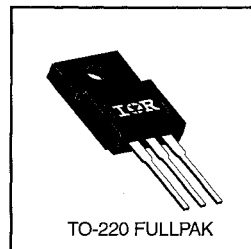
$$R_{DS(on)} = 2.0\Omega$$

$$I_D = 2.1A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



DATA SHEETS


### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.1	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	1.3	
$I_{DM}$	Pulsed Drain Current ①	8.4	
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	23	W
	Linear Derating Factor	0.18	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy ②	61	mJ
$I_{AR}$	Avalanche Current ①	2.1	A
$E_{AR}$	Repetitive Avalanche Energy ①	2.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.0	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to +150	°C
$T_{STG}$	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	


### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

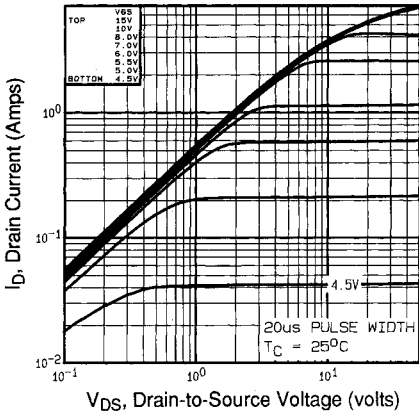
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	250	—	—	V	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.39	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	2.0	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=1.3\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$
$g_{fs}$	Forward Transconductance	0.80	—	—	S	$V_{DS}=50\text{V}$ , $I_D=1.3\text{A}$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{DS}=250\text{V}$ , $V_{GS}=0\text{V}$
		—	—	250		$V_{DS}=200\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20\text{V}$
$Q_g$	Total Gate Charge	—	—	8.2	nC	$I_D=2.7\text{A}$
$Q_{GS}$	Gate-to-Source Charge	—	—	1.8		$V_{DS}=200\text{V}$
$Q_{GD}$	Gate-to-Drain ("Miller") Charge	—	—	4.5		$V_{GS}=10\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	7.0	—	ns	$V_{DD}=125\text{V}$
$t_r$	Rise Time	—	7.6	—		$I_D=2.7\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		$R_G=24\Omega$
$t_f$	Fall Time	—	7.0	—		$R_D=45\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{ISS}$	Input Capacitance	—	140	—	pF	$V_{GS}=0\text{V}$
$C_{OSS}$	Output Capacitance	—	42	—		$V_{DS}=25\text{V}$
$C_{RSS}$	Reverse Transfer Capacitance	—	9.6	—		$f=1.0\text{MHz}$ See Figure 5
$C$	Drain to Sink Capacitance	—	12	—		$f=1.0\text{MHz}$

## Source-Drain Ratings and Characteristics

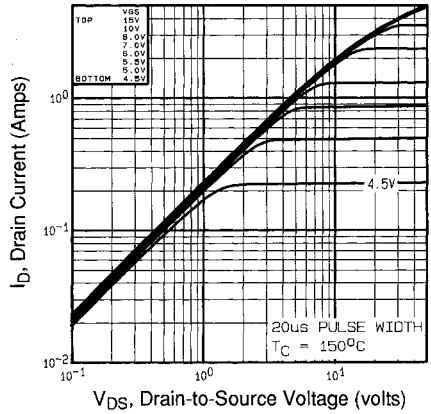
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	2.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	8.4		
$V_{SD}$	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}$ , $I_S=2.1\text{A}$ , $V_{GS}=0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	190	390	ns	$T_J=25^\circ\text{C}$ , $I_F=2.7\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	0.64	1.3	$\mu\text{C}$	$di/dt=100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

## Notes:

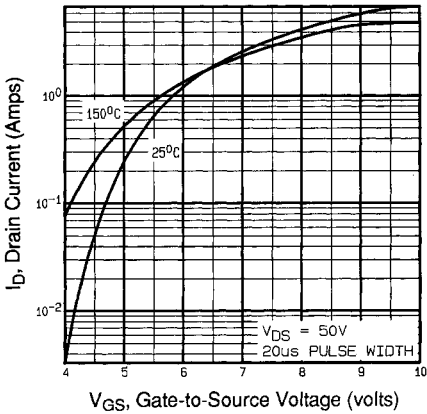
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=50\text{V}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=22\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=2.1\text{A}$  (See Figure 12)
- ③  $I_{SD}\leq 2.7\text{A}$ ,  $di/dt\leq 65\text{A}/\mu\text{s}$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$
- ⑤  $t=60\text{s}$ ,  $f=60\text{Hz}$



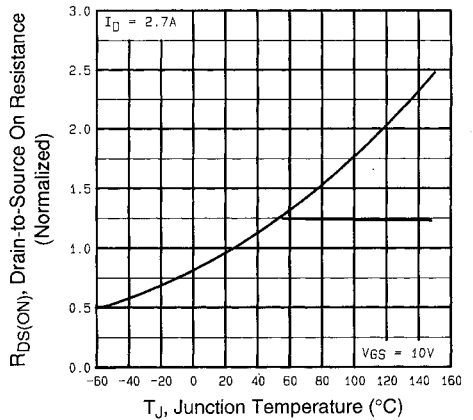
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



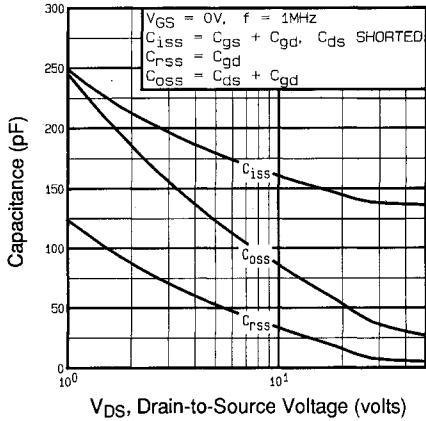
**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$



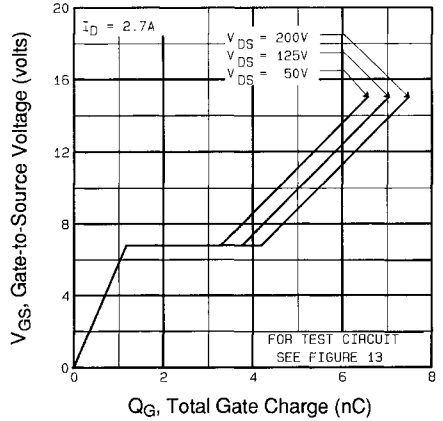
**Fig 3.** Typical Transfer Characteristics



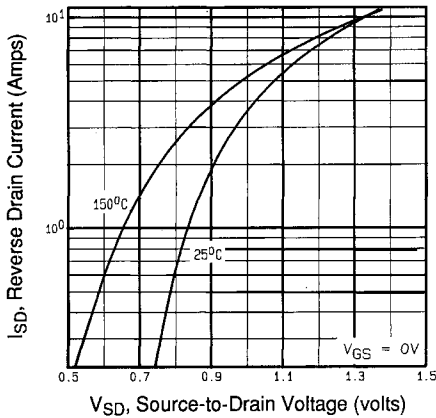
**Fig 4.** Normalized On-Resistance  
Vs. Temperature



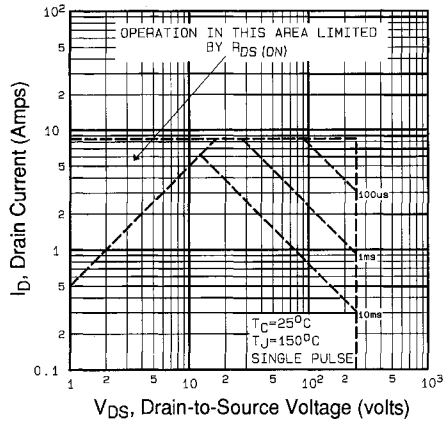
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



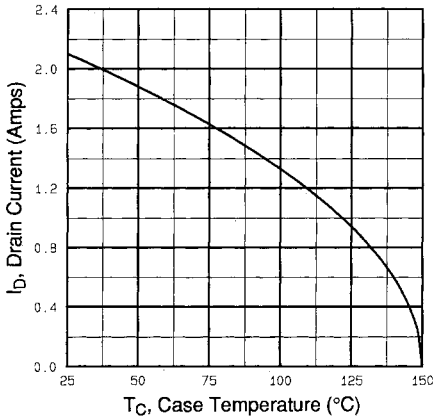
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



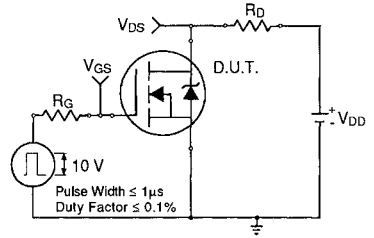
**Fig 7.** Typical Source-Drain Diode Forward Voltage



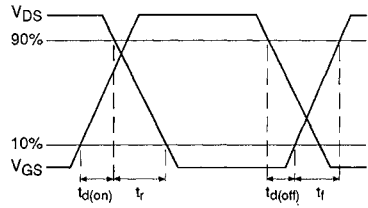
**Fig 8.** Maximum Safe Operating Area



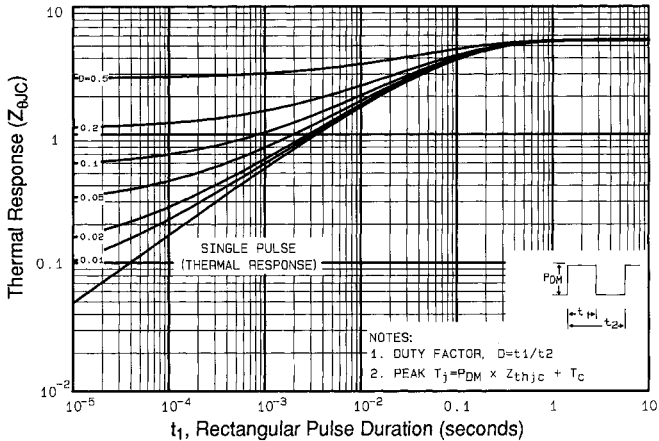
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

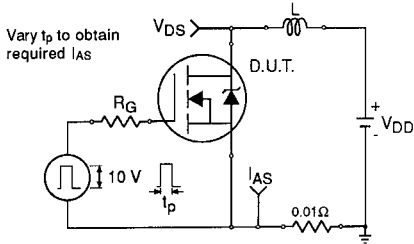


**Fig 10b.** Switching Time Waveforms

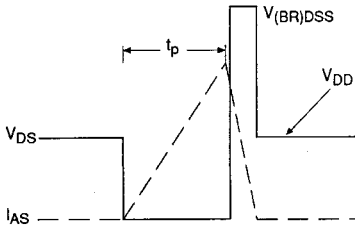


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

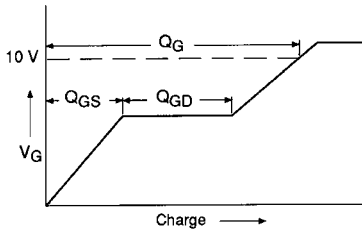
DATA SHEETS



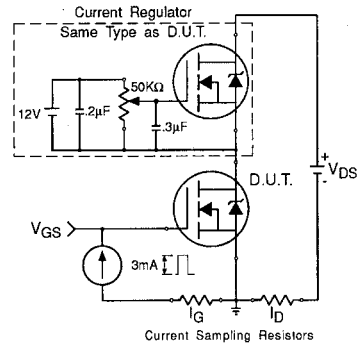
**Fig 12a.** Unclamped Inductive Test Circuit



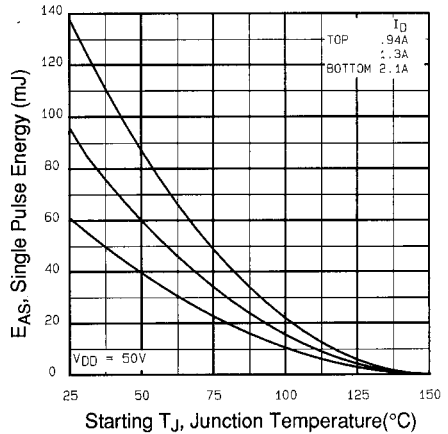
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517