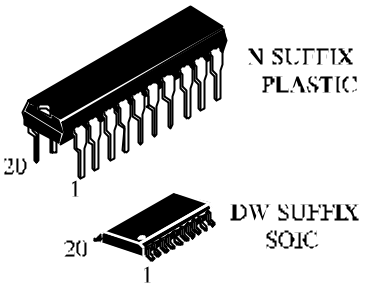
IN74LV640

Octal 3-State Inverting Bus Transceiver

The 74LV640 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT640.

The 74LV640 provides six inverting buffers with Schmitt-trigger action.

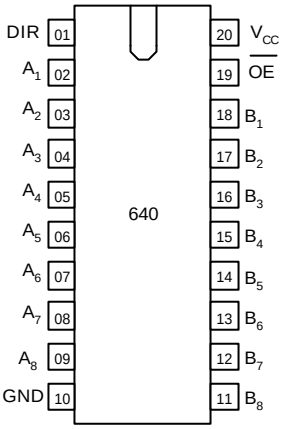
- Wide Operating Voltage: 1.2 to 3.6 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} =2.7 V and V_{CC} =3.6 V
- Low input current



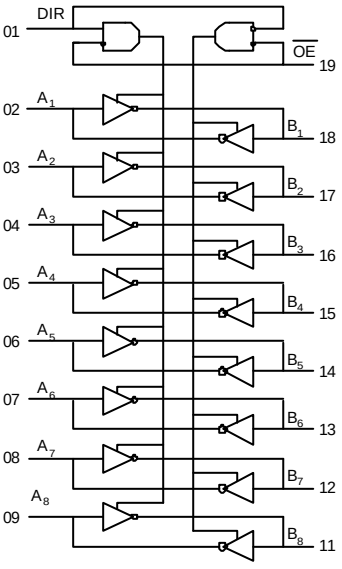
ORDERING INFORMATION

IN74LV640N Plastic
IN74LV640D SOIC
IZ74LV640 Chip
T_A = -40° to 125° C for all packages

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs		Inputs/Outputs	
$\overline{OE}$	DIR	À	Â
L	L	$\overline{A}$=B	input
L	H	input	$\overline{B}$=A
H	X	Z	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (Referenced to GND)	-0.5 ÷ +5.0	V
I_{IK}*[1]	DC input diode current	±20	mA
I_{OK}*[2]	DC output diode current	±50	mA
Io*[3]	DC output source or sink current -bus driver outputs	±35	mA
I_{GND}	DC GND current for types with - bus driver outputs	±70	mA
I_{CC}	DC V_{CC} current for types with - bus driver outputs	±70	mA
P_D	Power dissipation per paskade, plastic DIP+ SOIC package+	750 500	mW
Tstg	Storage temperature	-65 ÷ +150	°C
T_L	Lead temperature, 1.5 mm from Case for 10 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 12 mW/°C from 65° to 125°C
SOIC Package: : - 8 mW/°C from 65° to 125°C
*[1]: $V_I < -0.5V$ or $V_I > V_{CC}+0.5V$
*[2]: $Vo < -0.5V$ or $Vo > V_{CC}+0.5V$
*[3]: $-0.5V < Vo < V_{CC}+0.5V$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		1.2	3.6	V
V_{IN}, V_{OUT}	DC Input Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_{LH}, t_{HL}	Input Rise and Fall Time	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0	1000 700 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
				min	max	min	max	min	max	
V_{IH}	High-Level Input Voltage	$V_O = V_{CC}$-0.1 V	1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	V
V_{IL}	Low -Level Input Voltage		1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	V
V_{OH}	High-Level Output Voltage	$V_I = V_{IH}$ –or V_{IL} I_O = -50 µA	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	V
		$V_I = V_{IH}$ –or V_{IL} I_O = -8.0 mA	3.0	2.48	-	2.34	-	2.20	-	
V_{OL}	Low-Level Output Voltage	$V_I = V_{IH}$ –or V_{IL} I_O = 50 µA	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.09	- - - -	0.1 0.1 0.1 0.09	V
		$V_I = V_{IH}$ –or V_{IL} I_O = 8.0 mA	3.0	-	0.33	-	0.40	-	0.50	
I_{IL}	Low-Level Input Leakage Current	V_I=0 V	*	-	-0.1	-	-1.0	-	-1.0	µA
I_{IH}	High-Level Input Leakage Current	$V_I = V_{ÑÑ}$	*	-	0.1	-	1.0	-	1.0	µA
I_{OZ}	Maximum Three-State Leakage Current	$V_I = V_{IL}$ or V_{IH} $V_O = V_{CC}$ or GND	1.2 *	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	Quiescent Supply Current (per Package)	V_I=0 V or $V_{ÑÑ}$ I_O = 0 µA	*	-	8.0	-	80.0	-	180.0	µA

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_{LH} =t_{HL} = 6.0 ns, R_L=1 k?)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C ÷ 85°C		-40°C ÷ 125°C		
				min	max	min	max	min	max	
t_{PLH}, t_{PHL}	Propagation Delay, A to B , B to A	V_{IL}=0 V V_{IH}=V_{CC} t_{LH} = t_{HL} =6.0 ns Ñ$_L$ = 50 pF	1.2 2.0 *	- - -	100 23 14	- - -	125 28 18	- - -	140 34 21	ns
t_{PLZ}, t_{PHZ}	Propagation Delay , Direction or Output Enable to A or B	V_{IL}=0 V V_{IH}=V_{CC} t_{LH} = t_{HL} =6.0 ns Ñ$_L$ = 50 pF	1.2 2.0 *	- - -	120 30 20	- - -	140 37 24	- - -	160 43 28	ns
t_{PZL}, t_{PZH}	Propagation Delay , Direction or Output Enable to A or B	V_{IL}=0 V V_{IH}=V_{CC} t_{LH} = t_{HL} =6.0 ns Ñ$_L$ = 50 pF	1.2 2.0 *	- - -	120 28 17	- - -	140 35 21	- - -	160 43 26	ns
t_{TLH}, t_{THL}	Output Transition Time, Any Output	V_{IL}=0 V V_{IH}=V_{CC} t_{LH} = t_{HL} =6.0 ns Ñ$_L$ = 50 pF	1.2 2.0 *	- - -	60 16 10	- - -	75 20 13	- - -	90 24 15	ns
C_I	Input Capacitance (Pin 1 or Pin 19)		3.0	-	7.0	-	-	-	-	pF
$C_{I/O}$	Input Capacitance (Pin 2-9 or Pin 11-18)		3.0	-	20.0	-	-	-	-	pF
C_{PD}		V_I=0 V or $V_{ÑÑ}$		-	50	-	-	-	-	pF

* - V_{CC}=3.3±0.3V

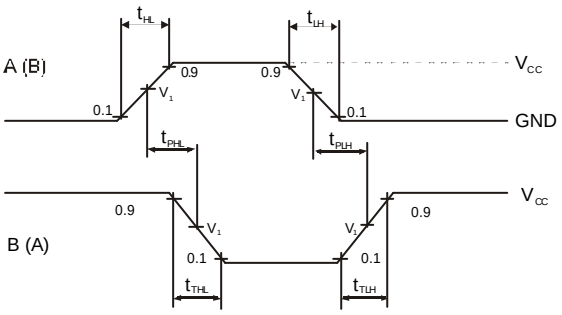
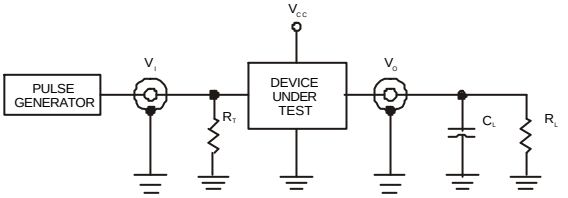


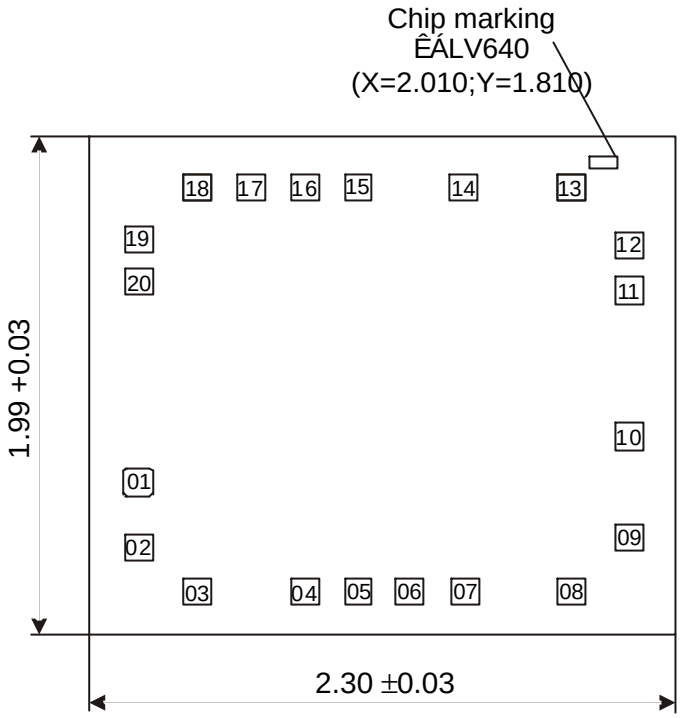
Figure 1. Switching Waveforms



Termination resistance R_T – should be equal to Z_{OUT} of pulse generators

Figure 2. Test Circuit

CHIP PAD DIAGRAM IZ74LV640



Pad size 0.108 x 0.108 mm (Pad size is given as per metallization layer)
Thickness of chip 0.46 ± 0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	DIR	0.140	0.573
02	A1	0.140	0.315
03	A2	0.370	0.140
04	A3	0.790	0.140
05	A4	1.000	0.140
06	A5	1.200	0.140
07	A6	1.417	0.140
08	A7	1.833	0.140
09	A8	2.060	0.354
10	GND	2.060	0.760
11	B8	2.060	1.340
12	B7	2.060	1.520
13	B6	1.833	1.750
14	B5	1.415	1.750
15	B4	1.000	1.750
16	B3	0.790	1.750
17	B2	0.580	1.750
18	B1	0.370	1.750
19	$\overline{OE}$	0.140	1.544
20	V_{CC}	0.140	1.375