



2.5V ZERO DELAY PLL CLOCK DRIVER TERA CLOCK™

IDT5T2010

FEATURES:

- 2.5V_{DD}
- 5 pairs of outputs
- Low skew: 50ps same pair, 100ps all outputs
- Selectable positive or negative edge synchronization
- Tolerant of spread spectrum input clock
- Synchronous output enable
- Selectable inputs
- Input frequency: 4.17MHz to 250MHz
- Output frequency: 12.5MHz to 250MHz
- 1.8V / 2.5V LVTTTL: up to 250MHz
- HSTL / eHSTL: up to 250MHz
- Hot insertable and over-voltage tolerant inputs
- 3-level inputs for selectable interface
- 3-level inputs for feedback divide selection with multiply ratios of (1-6, 8, 10, 12)
- Selectable HSTL, eHSTL, 1.8V/2.5V LVTTTL, or LVEPECL input interface
- Selectable differential or single-ended inputs and ten single-ended outputs
- PLL bypass for DC testing
- External differential feedback, internal loop filter
- Low Jitter: <75ps cycle-to-cycle
- Power-down mode
- Lock indicator
- Available in BGA and VFQFPN packages

DESCRIPTION:

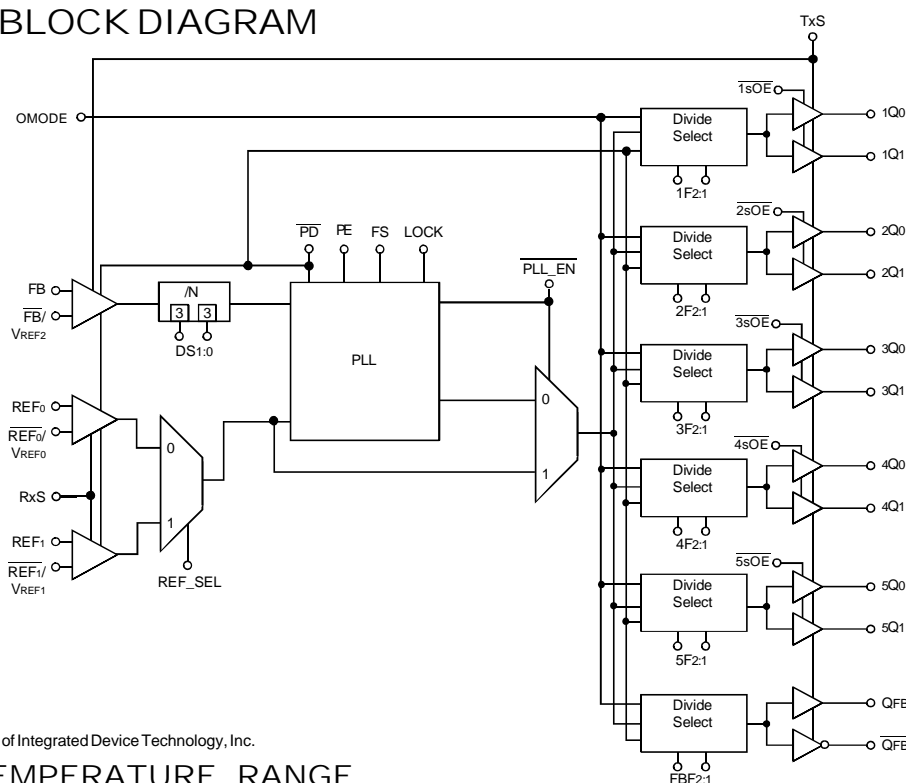
The IDT5T2010 is a 2.5V PLL clock driver intended for high performance computing and data-communications applications. The IDT5T2010 has ten outputs in five banks of two, plus a dedicated differential feedback. The redundant input capability allows for a smooth change over to a secondary clock source when the primary clock source is absent.

The feedback bank allows divide-by-functionality from 1 to 12 through the use of the DS[1:0] inputs. This provides the user with frequency multiplication 1 to 12 without using divided outputs for feedback. Each output bank also allows for a divide-by functionality of 2 or 4.

The IDT5T2010 features a user-selectable, single-ended or differential input to ten single-ended outputs. The clock driver also acts as a translator from a differential HSTL, eHSTL, 1.8V/2.5V LVTTTL, LVEPECL, or single-ended 1.8V/2.5V LVTTTL input to HSTL, eHSTL, or 1.8V/2.5V LVTTTL outputs. Selectable interface is controlled by 3-level input signals that may be hard-wired to appropriate high-mid-low levels. The outputs can be synchronously enabled/disabled.

Furthermore, when PE is held high, all the outputs are synchronized with the positive edge of the REF clock input. When PE is held low, all the outputs are synchronized with the negative edge of REF.

FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

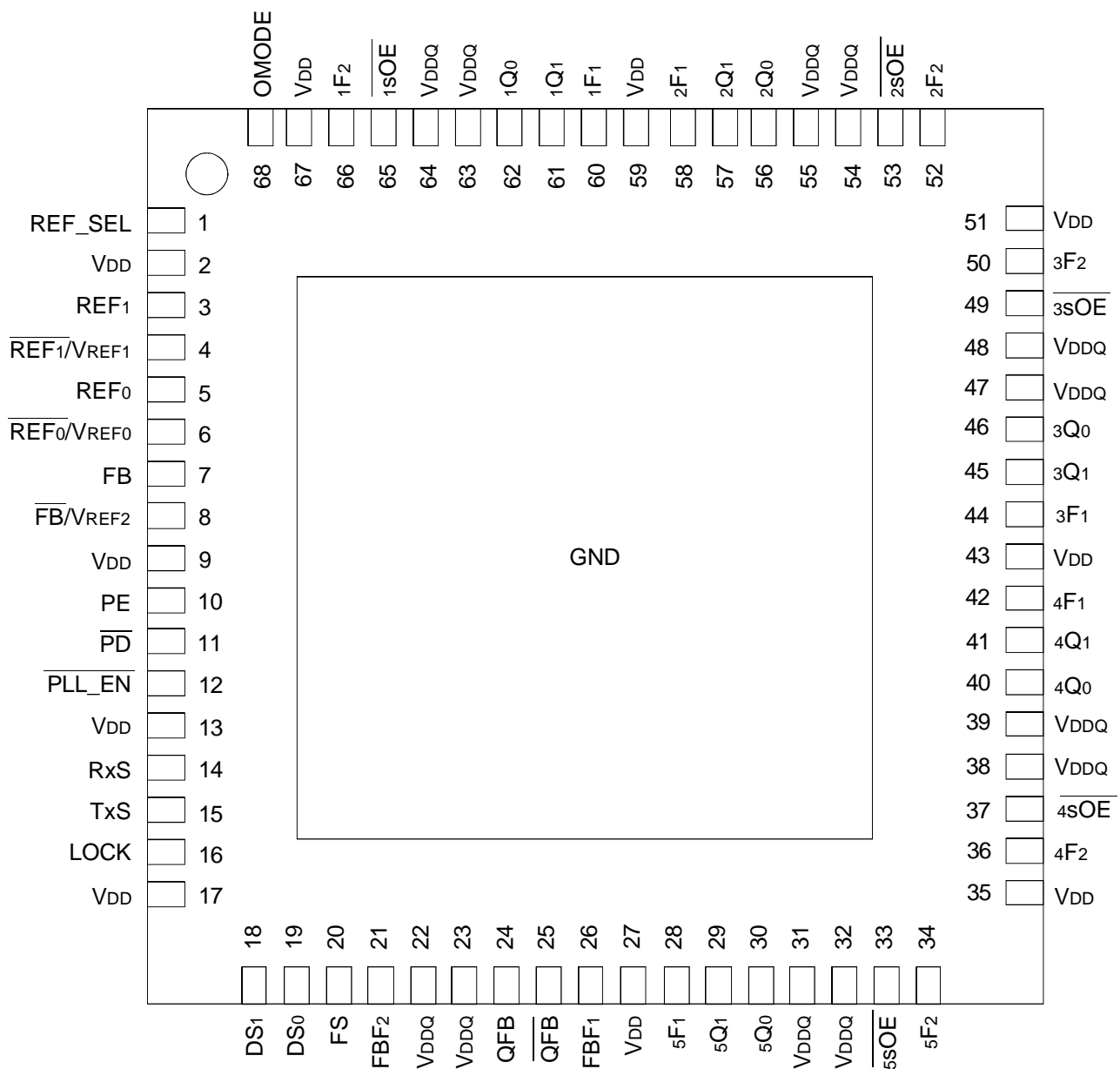
MAY 2003

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VDD	1F2	$\overline{1sOE}$	1Q0	1Q1	GND	GND	2Q1	2Q0	$\overline{2sOE}$	2F2	VDDQ	A
B	VDD	VDD	VDD	NC	1F1	GND	GND	2F1	NC	VDDQ	VDDQ	3F2	B
C	OMODE	VDD	VDD	VDD	GND	GND	GND	GND	VDDQ	VDDQ	VDDQ	$\overline{3sOE}$	C
D	REF_SEL	GND	VDD	VDD	GND	GND	GND	GND	VDDQ	VDDQ	NC	3Q0	D
E	REF1	$\overline{REF1}/VREF1$	NC	VDD	GND	GND	GND	GND	VDDQ	VDDQ	3F1	3Q1	E
F	REF0	$\overline{REF0}/VREF0$	VDD	VDD	GND	GND	GND	GND	VDDQ	VDDQ	VDDQ	VDDQ	F
G	FB	$\overline{FB}/VREF2$	VDD	VDD	GND	GND	GND	GND	VDDQ	VDDQ	VDDQ	VDDQ	G
H	\overline{PD}	$\overline{PLL_EN}$	PE	VDD	GND	GND	GND	GND	VDDQ	VDDQ	4F1	4Q1	H
J	RxS	TxS	VDD	VDD	GND	GND	GND	GND	VDDQ	VDDQ	NC	4Q0	J
K	LOCK	VDD	VDD	VDD	GND	GND	GND	GND	VDDQ	VDDQ	VDDQ	$\overline{4sOE}$	K
L	VDD	VDD	FS	NC	FBF1	GND	GND	5F1	NC	VDDQ	VDDQ	4F2	L
M	DS1	DS0	FBF2	QFB	\overline{QFB}	GND	GND	5Q1	5Q0	$\overline{5sOE}$	5F2	VDDQ	M
	1	2	3	4	5	6	7	8	9	10	11	12	

BGA
TOP VIEW

PIN CONFIGURATION



VFQFPN
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{DDQ} , V _{DD}	Power Supply Voltage ⁽²⁾	-0.5 to +3.6	V
V _I	Input Voltage	-0.5 to +3.6	V
V _O	Output Voltage	-0.5 to V _{DDQ} +0.5	V
V _{REF}	Reference Voltage ⁽³⁾	-0.5 to +3.6	V
T _J	Junction Temperature	150	°C
T _{STG}	Storage Temperature	-65 to +165	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DDQ} and V_{DD} internally operate independently. No power sequencing requirements need to be met.
- Not to exceed 3.6V.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Min.	Typ.	Max.	Unit
C _{IN}	Input Capacitance	2.5	3	3.5	pF
C _{OUT}	Output Capacitance	—	6.3	7	pF

NOTE:

- Capacitance applies to all inputs except RxS, TxS, nF[2:1], FBF[2:1], and DS[1:0].

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T _A	Ambient Operating Temperature	-40	+25	+85	°C
V _{DD} ⁽¹⁾	Internal Power Supply Voltage	2.3	2.5	2.7	V
V _{DDQ} ⁽¹⁾	HSTL Output Power Supply Voltage	1.4	1.5	1.6	V
	Extended HSTL and 1.8V LVTTTL Output Power Supply Voltage	1.65	1.8	1.95	V
	2.5V LVTTTL Output Power Supply Voltage		V _{DD}		V
V _T	Termination Voltage		V _{DDQ} / 2		V

NOTE:

- All power supplies should operate in tandem. If V_{DD} or V_{DDQ} is at maximum, then V_{DDQ} or V_{DD} (respectively) should be at maximum, and vice-versa.

PIN DESCRIPTION

Symbol	I/O	Type	Description
REF[1:0]	I	Adjustable ⁽¹⁾	Clock input. REF[1:0] is the "true" side of the differential clock input. If operating in single-ended mode, REF[1:0] is the clock input.
$\overline{\text{REF}}[1:0]$ / V _{REF} [1:0]	I	Adjustable ⁽¹⁾	Complementary clock input. $\overline{\text{REF}}[1:0]$ /V _{REF} [1:0] is the "complementary" side of REF[1:0] if the input is in differential mode. If operating in single-ended mode, $\overline{\text{REF}}[1:0]$ /V _{REF} [1:0] is left floating. For single-ended operation in differential mode, $\overline{\text{REF}}[1:0]$ /V _{REF} [1:0] should be set to the desired toggle voltage for REF[1:0]: 2.5V LVTTTL V _{REF} = 1250mV (SSTL2 compatible) 1.8V LVTTTL, eHSTL V _{REF} = 900mV HSTL V _{REF} = 750mV LVEPECL V _{REF} = 1082mV
FB	I	Adjustable ⁽¹⁾	Clock input. FB is the "true" side of the differential feedback clock input. If operating in single-ended mode, FB is the feedback clock input.
$\overline{\text{FB}}/V_{\text{REF}2}$	I	Adjustable ⁽¹⁾	Complementary feedback clock input. $\overline{\text{FB}}/V_{\text{REF}2}$ is the "complementary" side of FB if the input is in differential mode. If operating in single-ended mode, $\overline{\text{FB}}/V_{\text{REF}2}$ is left floating. For single-ended operation in differential mode, $\overline{\text{FB}}/V_{\text{REF}2}$ should be set to the desired toggle voltage for FB: 2.5V LVTTTL V _{REF} = 1250mV (SSTL2 compatible) 1.8V LVTTTL, eHSTL V _{REF} = 900mV HSTL V _{REF} = 750mV LVEPECL V _{REF} = 1082mV

NOTE:

- Inputs are capable of translating the following interface standards. User can select between:

Single-ended 2.5V LVTTTL levels
 Single-ended 1.8V LVTTTL levels
 or
 Differential 2.5V/1.8V LVTTTL levels
 Differential HSTL and eHSTL levels
 Differential LVEPECL levels

PIN DESCRIPTION, CONTINUED

Symbol	I/O	Type	Description
REF_SEL	I	LVTTL ⁽¹⁾	Reference clock select. When LOW, selects REF ₀ and $\overline{\text{REF}}_0/\text{V}_{\text{REF}0}$. When HIGH, selects REF ₁ and $\overline{\text{REF}}_1/\text{V}_{\text{REF}1}$.
$\overline{\text{nsOE}}$	I	LVTTL ⁽¹⁾	Synchronous output enable. When $\overline{\text{nsOE}}$ is HIGH, nQ[1:0] are synchronously stopped. OMODE selects whether the outputs are gated LOW/HIGH or tri-stated. When OMODE is HIGH, PE determines the level at which the outputs stop. When PE is LOW/HIGH, the nQ[1:0] is stopped in a HIGH/LOW state. When OMODE is LOW, the outputs are tri-stated. Set $\overline{\text{nsOE}}$ LOW for normal operation.
QFB	O	Adjustable ⁽²⁾	Feedback clock output
$\overline{\text{QFB}}$	O	Adjustable ⁽²⁾	Complementary feedback clock output
nQ[1:0]	O	Adjustable ⁽²⁾	Five banks of two outputs
RxS	I	3-Level ⁽³⁾	Selects single-ended 2.5V LVTTL (HIGH), 1.8V LVTTL (MID) REF clock input or differential (LOW) REF clock input
TxS	I	3-Level ⁽³⁾	Sets the drive strength of the output drivers and feedback inputs to be 2.5V LVTTL (HIGH), 1.8V LVTTL (MID) or HSTL/eHSTL (LOW) compatible. Used in conjunction with V _{DD0} to set the interface levels.
PE	I	LVTTL ⁽¹⁾	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock (has internal pull-up).
nF[2:1]	I	LVTTL ⁽¹⁾	Function select inputs for divide-by-2, divide-by-4, zero delay, or invert on each bank (See Control Summary table)
FBF[2:1]	I	LVTTL ⁽¹⁾	Function select inputs for divide-by-2, divide-by-4, zero delay, or invert on the feedback bank (See Control Summary table)
FS	I	LVTTL ⁽¹⁾	Selects appropriate oscillator circuit based on anticipated frequency range. (See VCO Frequency Range Select.)
DS[1:0]	I	3-Level ⁽³⁾	3-level inputs for feedback input divider selection (See Divide Selection table)
$\overline{\text{PLL_EN}}$	I	LVTTL ⁽¹⁾	PLL enable/disable control. Set LOW for normal operation. When $\overline{\text{PLL_EN}}$ is HIGH, the PLL is disabled and REF[1:0] goes to all outputs.
$\overline{\text{PD}}$	I	LVTTL ⁽¹⁾	Power down control. When $\overline{\text{PD}}$ is LOW, the inputs are disabled and internal switching is stopped. OMODE selects whether the outputs are gated LOW/HIGH or tri-stated. When OMODE is HIGH, PE determines the level at which the outputs stop. When PE is LOW/HIGH, the nQ[1:0] and QFB are stopped in a HIGH/LOW state, while the $\overline{\text{QFB}}$ is stopped in a LOW/HIGH state. When OMODE is LOW, the outputs are tri-stated. Set $\overline{\text{PD}}$ HIGH for normal operation.
LOCK	O	LVTTL	PLL lock indication signal. HIGH indicates lock. LOW indicates that the PLL is not locked and outputs may not be synchronized to the inputs. The output will be 2.5V LVTTL.
OMODE	I	LVTTL ⁽¹⁾	Output disable control. Determines the outputs' disable state. Used in conjunction with $\overline{\text{nsOE}}$ and $\overline{\text{PD}}$. (See Output Enable/Disable and Powerdown tables.)
V _{DD0}		PWR	Power supply for output buffers. When using 2.5V LVTTL, V _{DD0} should be connected to V _{DD} .
V _{DD}		PWR	Power supply for phase locked loop, lock output, inputs, and other internal circuitry
GND		PWR	Ground

NOTES:

1. Pins listed as LVTTL inputs will accept 2.5V signals under all conditions. If the output is operating at 1.8V or 1.5V, the LVTTL inputs will accept 1.8V LVTTL signals as well.
2. Outputs are user selectable to drive 2.5V, 1.8V LVTTL, eHSTL, or HSTL interface levels when used with the appropriate V_{DD0} voltage.
3. 3-level inputs are static inputs and must be tied to V_{DD} or GND or left floating. These inputs are not hot-insertable or over voltage tolerant.

OUTPUT ENABLE/DISABLE

$\overline{\text{nsOE}}$	OMODE	Output
L	X	Normal Operation
H	L	Tri-State
H	H	Gated ⁽¹⁾

NOTE:

1. PE determines the level at which the outputs stop. When PE is LOW/HIGH, the nQ[1:0] is stopped in a HIGH/LOW state.

POWERDOWN

$\overline{\text{PD}}$	OMODE	Output
H	X	Normal Operation
L	L	Tri-State
L	H	Gated ⁽¹⁾

NOTE:

1. PE determines the level at which the outputs stop. When PE is LOW/HIGH, the nQ[1:0] and QFB are stopped in a HIGH/LOW state, while the $\overline{\text{QFB}}$ is stopped in a LOW/HIGH state.

VCO FREQUENCY RANGE SELECT

FS ⁽¹⁾	Min.	Max.	Unit
LOW	50	125	MHz
HIGH	100	250	MHz

NOTE:

1. The level to be set on FS is determined by the nominal operating frequency of the VCO. The VCO frequency (F_{NOM}) always appears at nQ[1:0] outputs when they are operated in their undivided modes. The frequency appearing at the REF[1:0] and $\overline{\text{REF}}[1:0]/\text{V}_{\text{REF}1:0}$ and FB and $\overline{\text{FB}}/\text{V}_{\text{REF}2}$ inputs will be F_{NOM} when the QFB and $\overline{\text{QFB}}$ are undivided and DS[1:0] = MM. The frequency of REF[1:0] and $\overline{\text{REF}}[1:0]/\text{V}_{\text{REF}1:0}$ and FB and $\overline{\text{FB}}/\text{V}_{\text{REF}2}$ inputs will be F_{NOM}/2 or F_{NOM}/4 when the part is configured for frequency multiplication by using a divided QFB and $\overline{\text{QFB}}$ and setting DS[1:0] = MM. Using the DS[1:0] inputs allows a different method for frequency multiplication (see Divide Selection table).

EXTERNAL DIFFERENTIAL FEEDBACK

By providing a dedicated external differential feedback, the IDT5T2010 gives users flexibility with regard to divide selection. The FB and $\overline{\text{FB}}$ /VREF2 signals are compared with the input REF[1:0] and $\overline{\text{REF}}$ [1:0]/VREF[1:0] signals at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

DIVIDE SELECTION TABLE

DS [1:0]	Divide-by-n	Permitted Output Divide-by-n connected to FB and $\overline{\text{FB}}$ /VREF2 ⁽¹⁾
LL	2	1, 2
LM	3	1
LH	4	1, 2
ML	5	1, 2
MM	1	1, 2, 4
MH	6	1, 2
HL	8	1
HM	10	1
HH	12	1

NOTE:
1. Permissible output division ratios connected to FB and $\overline{\text{FB}}$ /VREF2. The frequencies of the REF[1:0] and $\overline{\text{REF}}$ [1:0]/VREF[1:0] inputs will be F_{NOM}/N when the parts are configured for frequency multiplication by using an undivided output for FB and $\overline{\text{FB}}$ /VREF2 and setting DS[1:0] to N (N = 1-6, 8, 10, 12).

CONTROL SUMMARY TABLE FOR ALL OUTPUTS

nF2/FBF2	nF1/FBF1	Output Skew
L	L	Divide by 2
L	H	Zero Delay
H	L	Inverted
H	H	Divide by 4

INPUT/OUTPUT SELECTION⁽¹⁾

Input	Output	Input	Output		
2.5V LVTTTL SE	2.5V LVTTTL	2.5V LVTTTL SE	eHSTL		
1.8V LVTTTL SE		1.8V LVTTTL SE			
2.5V LVTTTL DSE		2.5V LVTTTL DSE			
1.8V LVTTTL DSE		1.8V LVTTTL DSE			
LVEPECL DSE		LVEPECL DSE			
eHSTL DSE		eHSTL DSE			
HSTL DSE		HSTL DSE			
2.5V LVTTTL DIF		2.5V LVTTTL DIF			
1.8V LVTTTL DIF		1.8V LVTTTL DIF			
LVEPECL DIF		LVEPECL DIF			
eHSTL DIF		eHSTL DIF			
HSTL DIF		HSTL DIF			
2.5V LVTTTL SE		1.8V LVTTTL		2.5V LVTTTL SE	HSTL
1.8V LVTTTL SE				1.8V LVTTTL SE	
2.5V LVTTTL DSE	2.5V LVTTTL DSE				
1.8V LVTTTL DSE	1.8V LVTTTL DSE				
LVEPECL DSE	LVEPECL DSE				
eHSTL DSE	eHSTL DSE				
HSTL DSE	HSTL DSE				
2.5V LVTTTL DIF	2.5V LVTTTL DIF				
1.8V LVTTTL DIF	1.8V LVTTTL DIF				
LVEPECL DIF	LVEPECL DIF				
eHSTL DIF	eHSTL DIF				
HSTL DIF	HSTL DIF				

NOTE:
1. The INPUT/OUTPUT SELECTION Table describes the total possible combinations of input and output interfaces. Single-Ended (SE) inputs in a single-ended mode require the REF_[1:0]/VREF_[1:0] and FB/VREF₂ pins to be left floating. Differential Single-Ended (DSE) is for single-ended operation in differential mode, requiring VREF_[1:0] and VREF₂. Differential (DIF) inputs are used only in differential mode.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Max	Unit
V _{IHH}	Input HIGH Voltage Level ⁽¹⁾	3-Level Inputs Only	V _{DD} - 0.4	—	V
V _{IMM}	Input MID Voltage Level ⁽¹⁾	3-Level Inputs Only	V _{DD} /2 - 0.2	V _{DD} /2 + 0.2	V
V _{ILL}	Input LOW Voltage Level ⁽¹⁾	3-Level Inputs Only	—	0.4	V
I ₃	3-Level Input DC Current (RxS, TxS, DS _[1:0])	V _{IN} = V _{DD} HIGH Level	—	200	μA
		V _{IN} = V _{DD} /2 MID Level	-50	+50	
		V _{IN} = GND LOW Level	-200	—	
I _{PU}	Input Pull-Up Current (PE)	V _{DD} = Max., V _{IN} = GND	-100	—	μA

NOTE:
1. These inputs are normally wired to V_{DD}, GND, or left floating. Internal termination resistors bias unconnected inputs to V_{DD}/2. If these inputs are switched dynamically after powerup, the function and timing of the outputs may be glitched, and the PLL may require additional t_{LOCK} time before all datasheet limits are achieved.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR HSTL⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽⁷⁾	Max	Unit
Input Characteristics						
I _{IH}	Input HIGH Current	V _{DD} = 2.7V V _I = V _{DDQ} /GND	—	—	±5	μA
I _{IL}	Input LOW Current	V _{DD} = 2.7V V _I = GND/V _{DDQ}	—	—	±5	
V _{IK}	Clamp Diode Voltage	V _{DD} = 2.3V, I _{IN} = -18mA	—	-0.7	-1.2	V
V _{IN}	DC Input Voltage		-0.3		+3.6	V
V _{DIF}	DC Differential Voltage ^(2,8)		0.2		—	V
V _{CM}	DC Common Mode Input Voltage ^(3,8)		680	750	900	mV
V _{IH}	DC Input HIGH ^(4,5,8)		V _{REF} + 100		—	mV
V _{IL}	DC Input LOW ^(4,6,8)		—		V _{REF} - 100	mV
V _{REF}	Single-Ended Reference Voltage ^(4,8)		—	750	—	mV
Output Characteristics						
V _{OH}	Output HIGH Voltage	I _{OH} = -8mA	V _{DDQ} - 0.4		—	V
		I _{OH} = -100μA	V _{DDQ} - 0.1		—	
V _{OL}	Output LOW Voltage	I _{OL} = 8mA	—		0.4	V
		I _{OL} = 100μA	—		0.1	
V _{OX}	FB/FB Output Crossing Point		V _{DDQ} /2 - 150	V _{DDQ} /2	V _{DDQ} /2 + 150	mV

NOTES:

- See RECOMMENDED OPERATING RANGE table.
- V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) / 2. Differential mode only.
- For single-ended operation, in differential mode, $\overline{\text{REF}}_{[1:0]}/V_{\text{REF}[1:0]}$ is tied to the DC voltage V_{REF[1:0]}.
- Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.5V, +25°C ambient.
- The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. (See Input/Output Selection table.)

POWER SUPPLY CHARACTERISTICS FOR HSTL OUTPUTS⁽¹⁾

Symbol	Parameter	Test Conditions ⁽²⁾	Typ.	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current ⁽³⁾	V _{DDQ} = Max., REF = LOW, $\overline{\text{PD}}$ = HIGH, $\overline{\text{nSOE}}$ = LOW, $\overline{\text{PLL_EN}}$ = HIGH, DS[1:0] = MM, nF[2:1] = LH, FBF[2:1] = LH, Outputs enabled, All outputs unloaded	15	25	mA
I _{DDQQ}	Quiescent V _{DDQ} Power Supply Current ⁽³⁾	V _{DDQ} = Max., REF = LOW, $\overline{\text{PD}}$ = HIGH, $\overline{\text{nSOE}}$ = LOW, $\overline{\text{PLL_EN}}$ = HIGH, DS[1:0] = MM, nF[2:1] = LH, FBF[2:1] = LH, Outputs enabled, All outputs unloaded	0.7	50	μA
I _{DDPD}	Power Down Current	V _{DD} = Max., $\overline{\text{PD}}$ = LOW, $\overline{\text{nSOE}}$ = LOW, $\overline{\text{PLL_EN}}$ = HIGH	0.8	3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	13	20	μA/MHz
I _{DDQD}	Dynamic V _{DDQ} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	16	25	μA/MHz
I _{TOT}	Total Power V _{DD} Supply Current ⁽⁴⁾	V _{DDQ} = 1.5V, F _{VCO} = 100MHz, C _L = 15pF	35	55	mA
		V _{DDQ} = 1.5V, F _{VCO} = 250MHz, C _L = 15pF	55	85	
I _{TOTQ}	Total Power V _{DDQ} Supply Current ⁽⁴⁾	V _{DDQ} = 1.5V, F _{VCO} = 100MHz, C _L = 15pF	45	70	mA
		V _{DDQ} = 1.5V, F _{VCO} = 250MHz, C _L = 15pF	80	120	

NOTES:

- These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
- The termination resistors are excluded from these measurements.
- If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
- FS = HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

Symbol	Parameter	Value	Units
V _{DIF}	Input Signal Swing ⁽¹⁾	1	V
V _X	Differential Input Signal Crossing Point ⁽²⁾	750	mV
V _{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁽⁴⁾	1	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR eHSTL⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽⁷⁾	Max	Unit
Input Characteristics						
I _{IH}	Input HIGH Current	V _{DD} = 2.7V V _I = V _{DDQ} /GND	—	—	±5	μA
I _{IL}	Input LOW Current	V _{DD} = 2.7V V _I = GND/V _{DDQ}	—	—	±5	μA
V _{IK}	Clamp Diode Voltage	V _{DD} = 2.3V, I _{IN} = -18mA	—	-0.7	-1.2	V
V _{IN}	DC Input Voltage		-0.3		+3.6	V
V _{DIF}	DC Differential Voltage ^(2,8)		0.2		—	V
V _{CM}	DC Common Mode Input Voltage ^(3,8)		800	900	1000	mV
V _{IH}	DC Input HIGH ^(4,5,8)		V _{REF} + 100		—	mV
V _{IL}	DC Input LOW ^(4,6,8)		—		V _{REF} - 100	mV
V _{REF}	Single-Ended Reference Voltage ^(4,8)		—	900	—	mV

Output Characteristics

V _{OH}	Output HIGH Voltage	I _{OH} = -8mA	V _{DDQ} - 0.4	—	V	
		I _{OH} = -100μA	V _{DDQ} - 0.1	—	V	
V _{OL}	Output LOW Voltage	I _{OL} = 8mA	—	0.4	V	
		I _{OL} = 100μA	—	0.1	V	
V _{OX}	FB/ $\overline{\text{FB}}$ Output Crossing Point		V _{DDQ} /2 - 150	V _{DDQ} /2	V _{DDQ} /2 + 150	mV

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation, in a differential mode, $\overline{\text{REF}}_{[1:0]}/\text{VREF}_{[1:0]}$ is tied to the DC voltage V_{REF}[1:0].
5. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
6. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
7. Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.8V, +25°C ambient.
8. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. (See Input/Output Selection table.)

POWER SUPPLY CHARACTERISTICS FOR eHSTL OUTPUTS⁽¹⁾

Symbol	Parameter	Test Conditions ⁽²⁾	Typ.	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current ⁽³⁾	V _{DDQ} = Max., REF = LOW, \overline{PD} = HIGH, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH, DS[1:0] = MM, nF[2:1] = LH, FBF[2:1] = LH, Outputs enabled, All outputs unloaded	15	25	mA
I _{DDQQ}	Quiescent V _{DDQ} Power Supply Current ⁽³⁾	V _{DDQ} = Max., REF = LOW, \overline{PD} = HIGH, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH, DS[1:0] = MM, nF[2:1] = LH, FBF[2:1] = LH, Outputs enabled, All outputs unloaded	1.7	50	μA
I _{DDPD}	Power Down Current	V _{DD} = Max., \overline{PD} = LOW, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH	0.8	3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	13	20	μA/MHz
I _{DDQD}	Dynamic V _{DDQ} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	20	30	μA/MHz
I _{TOT}	Total Power V _{DD} Supply Current ⁽⁴⁾	V _{DDQ} = 1.8V, F _{VCO} = 100MHz, C _L = 15pF	35	55	mA
		V _{DDQ} = 1.8V, F _{VCO} = 250MHz, C _L = 15pF	55	85	
I _{TOTO}	Total Power V _{DDQ} Supply Current ⁽⁴⁾	V _{DDQ} = 1.8V, F _{VCO} = 100MHz, C _L = 15pF	50	75	mA
		V _{DDQ} = 1.8V, F _{VCO} = 250MHz, C _L = 15pF	115	175	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
4. FS = HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

Symbol	Parameter	Value	Units
V _{DIF}	Input Signal Swing ⁽¹⁾	1	V
V _X	Differential Input Signal Crossing Point ⁽²⁾	900	mV
V _{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁽⁴⁾	1	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVEPECL⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽²⁾	Max	Unit
Input Characteristics						
I _{IH}	Input HIGH Current	V _{DD} = 2.7V V _I = V _{DDQ} /GND	—	—	±5	μA
I _{IL}	Input LOW Current	V _{DD} = 2.7V V _I = GND/V _{DDQ}	—	—	±5	μA
V _{IK}	Clamp Diode Voltage	V _{DD} = 2.3V, I _{IN} = -18mA	—	-0.7	-1.2	V
V _{IN}	DC Input Voltage		-0.3	—	3.6	V
V _{CM}	DC Common Mode Input Voltage ^(3,5)		915	1082	1248	mV
V _{REF}	Single-Ended Reference Voltage ^(4,5)		—	1082	—	mV
V _{IH}	DC Input HIGH		1275	—	1620	mV
V _{IL}	DC Input LOW		555	—	875	mV

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V_{DD} = 2.5V, +25°C ambient.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation while in differential mode, REF_[1:0]/VREF_[1:0] is tied to the DC voltage VREF_[1:0].
5. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. (See Input/Output Selection table.)

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL

Symbol	Parameter	Value	Units
V _{DIF}	Input Signal Swing ⁽¹⁾	732	mV
V _X	Differential Input Signal Crossing Point ⁽²⁾	1082	mV
V _{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁽⁴⁾	1	V/ns

NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 1082mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR 2.5V LVTTTL⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽⁸⁾	Max	Unit
Input Characteristics						
I _{IH}	Input HIGH Current	V _{DD} = 2.7V V _I = V _{DDQ} /GND	—	—	±5	μA
I _{IL}	Input LOW Current	V _{DD} = 2.7V V _I = GND/V _{DDQ}	—	—	±5	
V _{IK}	Clamp Diode Voltage	V _{DD} = 2.3V, I _{IN} = -18mA	—	-0.7	-1.2	V
V _{IN}	DC Input Voltage		-0.3		+3.6	V
Single-Ended Inputs⁽²⁾						
V _{IH}	DC Input HIGH		1.7		—	V
V _{IL}	DC Input LOW		—		0.7	V
Differential Inputs						
V _{DIF}	DC Differential Voltage ^(3,9)		0.2		—	V
V _{CM}	DC Common Mode Input Voltage ^(4,9)		1150	1250	1350	mV
V _{IH}	DC Input HIGH ^(5,6,9)		V _{REF} + 100		—	mV
V _{IL}	DC Input LOW ^(5,7,9)		—		V _{REF} - 100	mV
V _{REF}	Single-Ended Reference Voltage ^(5,9)		—	1250	—	mV
Output Characteristics						
V _{OH}	Output HIGH Voltage	I _{OH} = -12mA	V _{DDQ} - 0.4		—	V
		I _{OH} = -100μA	V _{DDQ} - 0.1		—	V
V _{OL}	Output LOW Voltage	I _{OL} = 12mA	—		0.4	V
		I _{OL} = 100μA	—		0.1	V

NOTES:

- See RECOMMENDED OPERATING RANGE table.
- For 2.5V LVTTTL single-ended operation, the RxS pin is tied HIGH and $\overline{\text{REF}}_{[1:0]}/\text{VREF}_{[1:0]}$ is left floating. If TxS is HIGH, $\overline{\text{FB}}/\text{VREF}_2$ should be left floating.
- V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) / 2. Differential mode only.
- For single-ended operation, in differential mode, $\overline{\text{REF}}_{[1:0]}/\text{VREF}_{[1:0]}$ is tied to the DC voltage V_{REF}[1:0].
- Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- Typical values are at V_{DD} = 2.5V, V_{DDQ} = V_{DD}, +25°C ambient.
- The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. (See Input/Output Selection table.)

POWER SUPPLY CHARACTERISTICS FOR 2.5V LVTTTL OUTPUTS⁽¹⁾

Symbol	Parameter	Test Conditions ⁽²⁾	Typ.	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current ⁽³⁾	V _{DDQ} = Max., REF = LOW, \overline{PD} = HIGH, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH, DS _[1:0] = MM, nF _[2:1] = LH, FBF _[2:1] = LH, Outputs enabled, All outputs unloaded	15	25	mA
I _{DDQQ}	Quiescent V _{DDQ} Power Supply Current ⁽³⁾	V _{DDQ} = Max., REF = LOW, \overline{PD} = HIGH, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH, DS _[1:0] = MM, nF _[2:1] = LH, FBF _[2:1] = LH, Outputs enabled, All outputs unloaded	12	50	μA
I _{DDPD}	Power Down Current	V _{DD} = Max., \overline{PD} = LOW, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH	0.5	3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	15	25	μA/MHz
I _{DDQD}	Dynamic V _{DDQ} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	30	40	μA/MHz
I _{TOT}	Total Power V _{DD} Supply Current ⁽⁴⁾	V _{DDQ} = 2.5V., F _{VCO} = 100MHz, C _L = 15pF	40	60	mA
		V _{DDQ} = 2.5V., F _{VCO} = 250MHz, C _L = 15pF	60	90	
I _{TOTO}	Total Power V _{DDQ} Supply Current ⁽⁴⁾	V _{DDQ} = 2.5V., F _{VCO} = 100MHz, C _L = 15pF	80	120	mA
		V _{DDQ} = 2.5V., F _{VCO} = 250MHz, C _L = 15pF	200	300	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
4. FS = HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR 2.5V LVTTTL

Symbol	Parameter	Value	Units
V _{DIF}	Input Signal Swing ⁽¹⁾	V _{DD}	V
V _X	Differential Input Signal Crossing Point ⁽²⁾	V _{DD} /2	V
V _{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁽⁴⁾	2.5	V/ns

NOTES:

1. A nominal 2.5V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 1.25V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2.5V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

SINGLE-ENDED INPUT AC TEST CONDITIONS FOR 2.5V LVTTTL

Symbol	Parameter	Value	Units
V _{IH}	Input HIGH Voltage	V _{DD}	V
V _{IL}	Input LOW Voltage	0	V
V _{THI}	Input Timing Measurement Reference Level ⁽¹⁾	V _{DD} /2	V
t _R , t _F	Input Signal Edge Rate ⁽²⁾	2	V/ns

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR 1.8V LVTTTL⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽⁶⁾	Max	Unit
Input Characteristics						
I _{IH}	Input HIGH Current	V _{DD} = 2.7V V _I = V _{DDQ} /GND	—	—	±5	μA
I _{IL}	Input LOW Current	V _{DD} = 2.7V V _I = GND/V _{DDQ}	—	—	±5	μA
V _{IK}	Clamp Diode Voltage	V _{DD} = 2.3V, I _{IN} = -18mA	—	-0.7	-1.2	V
V _{IN}	DC Input Voltage		-0.3		V _{DDQ} + 0.3	V
Single-Ended Inputs⁽²⁾						
V _{IH}	DC Input HIGH		1.073 ⁽¹⁰⁾		—	V
V _{IL}	DC Input LOW		—		0.683 ⁽¹¹⁾	V
Differential Inputs						
V _{DIF}	DC Differential Voltage ^(3,9)		0.2		—	V
V _{CM}	DC Common Mode Input Voltage ^(4,9)		825	900	975	mV
V _{IH}	DC Input HIGH ^(5,6,9)		V _{REF} + 100		—	mV
V _{IL}	DC Input LOW ^(5,7,9)		—		V _{REF} - 100	mV
V _{REF}	Single-Ended Reference Voltage ^(5,9)		—	900	—	mV
Output Characteristics						
V _{OH}	Output HIGH Voltage	I _{OH} = -6mA	V _{DDQ} - 0.4		—	V
		I _{OH} = -100μA	V _{DDQ} - 0.1		—	V
V _{OL}	Output LOW Voltage	I _{OL} = 6mA	—		0.4	V
		I _{OL} = 100μA	—		0.1	V

NOTES:

- See RECOMMENDED OPERATING RANGE table.
- For 1.8V LVTTTL single-ended operation, the RxS pin is MID and $\overline{\text{REF}}_{[1:0]}/\text{V}_{\text{REF}[1:0]}$ is left floating. If TxS is MID, $\overline{\text{FB}}/\text{V}_{\text{REF}2}$ should be left floating.
- V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) / 2. Differential mode only.
- For single-ended operation in differential mode, $\overline{\text{REF}}_{[1:0]}/\text{V}_{\text{REF}[1:0]}$ is tied to the DC voltage V_{REF[1:0]}. The input is guaranteed to toggle within ±200mV of V_{REF[1:0]} when V_{REF[1:0]} is constrained within +600mV and V_{DDI}-600mV, where V_{DDI} is the nominal 1.8V power supply of the device driving the REF_[1:0] input. To guarantee switching in voltage range specified in the JEDEC 1.8V LVTTTL interface specification, V_{REF[1:0]} must be maintained at 900mV with appropriate tolerances.
- Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- Typical values are at V_{DD} = 2.5V, V_{DDQ} = 1.8V, +25°C ambient.
- The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. (See Input/Output Selection table.)
- This value is the worst case minimum V_{IH} over the specification range of the 1.8V power supply. The 1.8V LVTTTL specification is V_{IH} = 0.65 * V_{DD} where V_{DD} is 1.8V ± 0.15V. However, the LVTTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value (V_{IH} = 0.65 * [1.8 - 0.15V]) rather than reference against a nominal 1.8V supply.
- This value is the worst case maximum V_{IL} over the specification range of the 1.8V power supply. The 1.8V LVTTTL specification is V_{IL} = 0.35 * V_{DD} where V_{DD} is 1.8V ± 0.15V. However, the LVTTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value (V_{IL} = 0.35 * [1.8 + 0.15V]) rather than reference against a nominal 1.8V supply.

POWER SUPPLY CHARACTERISTICS FOR 1.8V LVTTTL OUTPUTS⁽¹⁾

Symbol	Parameter	Test Conditions ⁽²⁾	Typ.	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current ⁽³⁾	V _{DDQ} = Max., REF = LOW, \overline{PD} = HIGH, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH, DS[1:0] = MM, nF[2:1] = LH, FBF[2:1] = LH, Outputs enabled, All outputs unloaded	15	25	mA
I _{DDOQ}	Quiescent V _{DDO} Power Supply Current ⁽³⁾	V _{DDO} = Max., REF = LOW, \overline{PD} = HIGH, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH, DS[1:0] = MM, nF[2:1] = LH, FBF[2:1] = LH, Outputs enabled, All outputs unloaded	1.5	50	μA
I _{DDPD}	Power Down Current	V _{DD} = Max., \overline{PD} = LOW, \overline{nSOE} = LOW, $\overline{PLL_EN}$ = HIGH	0.5	3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V _{DD} = Max., V _{DDO} = Max., C _L = 0pF	16	25	μA/MHz
I _{DDOQ}	Dynamic V _{DDO} Power Supply Current per Output	V _{DD} = Max., V _{DDO} = Max., C _L = 0pF	22	30	μA/MHz
I _{TOT}	Total Power V _{DD} Supply Current ⁽⁴⁾	V _{DDQ} = 1.8V., F _{VCO} = 100MHz, C _L = 15pF	40	60	mA
		V _{DDQ} = 1.8V., F _{VCO} = 250MHz, C _L = 15pF	70	105	
I _{TOTO}	Total Power V _{DDO} Supply Current ⁽⁴⁾	V _{DDQ} = 1.8V., F _{VCO} = 100MHz, C _L = 15pF	55	85	mA
		V _{DDQ} = 1.8V., F _{VCO} = 250MHz, C _L = 15pF	135	205	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
4. FS = HIGH.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR 1.8V LVTTTL

Symbol	Parameter	Value	Units
V _{DIF}	Input Signal Swing ⁽¹⁾	V _{DDI}	V
V _X	Differential Input Signal Crossing Point ⁽²⁾	V _{DDI} /2	mV
V _{THI}	Input Timing Measurement Reference Level ⁽³⁾	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁽⁴⁾	1.8	V/ns

NOTES:

1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input. A nominal 1.8V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1.8V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

SINGLE-ENDED INPUT AC TEST CONDITIONS FOR 1.8V LVTTTL

Symbol	Parameter	Value	Units
V _{IH}	Input HIGH Voltage ⁽¹⁾	V _{DDI}	V
V _{IL}	Input LOW Voltage	0	V
V _{THI}	Input Timing Measurement Reference Level ⁽²⁾	V _{DDI} /2	mV
t _R , t _F	Input Signal Edge Rate ⁽³⁾	2	V/ns

NOTES:

1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input.
2. A nominal 900mV timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
3. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Min.	Typ.	Max	Unit	
F _{NOM}	VCO Frequency Range	see VCO Frequency Range Select Table				
t _{RPW}	Reference Clock Pulse Width HIGH or LOW	1	—	—	ns	
t _{FPW}	Feedback Input Pulse Width HIGH or LOW	1	—	—	ns	
t _{SK(B)}	Output Matched Pair Skew ^(1,2,4)	—	—	50	ps	
t _{SK(O)}	Output Skew (Rise-Rise, Fall-Fall, Nominal) ^(1,3)	—	—	100	ps	
t _{SK1(ω)}	Multiple Frequency Skew (Rise-Rise, Fall-Fall, Nominal-Divided, Divided-Divided) ^(1,3,4)	—	—	100	ps	
t _{SK2(ω)}	Multiple Frequency Skew (Rise-Fall, Nominal-Divided, Divided-Divided) ^(1,3,4)	—	—	400	ps	
t _{SK1(INV)}	Inverting Skew (Nominal-Inverted) ^(1,3)	—	—	400	ps	
t _{SK2(INV)}	Inverting Skew (Rise-Rise, Fall-Fall, Rise-Fall, Inverted-Divided) ^(1,3,4)	—	—	400	ps	
t _{SK(PR)}	Process Skew ^(1,3,5)	—	—	300	ps	
t(φ)	REF Input to FB Static Phase Offset ⁽⁶⁾	-100	—	100	ps	
t _{ODCV}	Output Duty Cycle Variation from 50% ⁽⁷⁾	HSTL / eHSTL / 1.8V LVTTTL	-375	—	375	ps
		2.5V LVTTTL	-275	—	275	
t _{ORISE}	Output Rise Time ⁽⁸⁾	HSTL / eHSTL / 1.8V LVTTTL	—	—	1.2	ns
		2.5V LVTTTL	—	—	1	
t _{OFALL}	Output Fall Time ⁽⁸⁾	HSTL / eHSTL / 1.8V LVTTTL	—	—	1.2	ns
		2.5V LVTTTL	—	—	1	
t _L	Power-up PLL Lock Time ⁽⁹⁾	—	—	1	ms	
t _{L(ω)}	PLL Lock Time After Input Frequency Change ⁽⁹⁾	—	—	1	ms	
t _{L(REFSEL1)}	PLL Lock Time After Change in REF_SEL ^(9,11)	—	—	100	μs	
t _{L(REFSEL2)}	PLL Lock Time After Change in REF_SEL (REF ₁ and REF ₀ are different frequency) ⁽⁹⁾	—	—	1	ms	
t _{L(PD)}	PLL Lock Time After Asserting \overline{PD} Pin ⁽⁹⁾	—	—	1	ms	
t _{JIT(CC)}	Cycle-to-Cycle Output Jitter (peak-to-peak) ⁽¹⁰⁾	—	50	75	ps	
t _{JIT(PER)}	Period Jitter (peak-to-peak) ⁽¹⁰⁾	—	—	75	ps	
t _{JIT(HP)}	Half Period Jitter (peak-to-peak, QFB/QFB only) ^(10,12)	—	—	125	ps	
t _{JIT(DUTY)}	Duty Cycle Jitter (peak-to-peak) ⁽¹⁰⁾	—	—	100	ps	
V _{OX}	HSTL and eHSTL Differential True and Complementary Output Crossing Voltage Level QFB/QFB only ⁽¹²⁾	V _{DD0} /2 - 150	V _{DD0} /2	V _{DD0} /2 + 150	mV	

NOTES:

- Skew is the time between the earliest and latest output transition among all outputs when all outputs are loaded with the specified load.
- t_{SK(B)} is the skew between a pair of outputs (nQ0 and nQ1) when all outputs are selected as the same class.
- The measurement is made at V_{DD0}/2.
- There are three classes of outputs: nominal (zero delay), inverted, and divided (divide-by-2 or divide-by-4 mode).
- t_{SK(PR)} is the output to corresponding output skew between any two devices operating under the same conditions (V_{DD} and V_{DD0}, ambient temperature, air flow, etc.).
- t(φ) is measured with REF and FB the same type of input, the same rise and fall times. For TxS/RxS = MID or HIGH, the measurement is taken from V_{THI} on REF to V_{THI} on FB. For TxS/RxS = LOW, the measurement is taken from the crosspoint of REF/REF to the crosspoint of FB/FB. All outputs are set to zero delay, FB input divider set to divide-by-one, and FS = HIGH.
- t_{ODCV} is measured with all outputs selected for zero delay.
- Output rise and fall times are measured between 20% to 80% of the actual output voltage swing.
- t_L, t_{L(ω)}, t_{L(REFSEL1)}, t_{L(REFSEL2)}, and t_{L(PD)} are the times that are required before the synchronization is achieved. These specifications are valid only after V_{DD}/V_{DD0} is stable and within the normal operating limits. These parameters are measured from the application of a new signal at REF or FB, or after PD is (re)asserted until t(φ) is within specified limits.
- The jitter parameters are measured with all outputs selected for zero delay, FB input divider is set to divide-by-one, and FS = HIGH.
- Both REF inputs must be the same frequency, but up to ±180° out of phase.
- For HSTL/eHSTL outputs only.

AC DIFFERENTIAL INPUT SPECIFICATIONS⁽¹⁾

Symbol	Parameter	Min.	Typ.	Max	Unit
t _w	Reference/Feedback Input Clock Pulse Width HIGH or LOW (HSTL/eHSTL outputs) ⁽²⁾	1	—	—	ns
	Reference/Feedback Input Clock Pulse Width HIGH or LOW (2.5V / 1.8V LVTTTL outputs) ⁽²⁾	1	—	—	

HSTL/eHSTL/1.8V LVTTTL/2.5V LVTTTL

V _{DIF}	AC Differential Voltage ⁽³⁾	400	—	—	mV
V _{IH}	AC Input HIGH ^(4,5)	V _x + 200	—	—	mV
V _{IL}	AC Input LOW ^(4,6)	—	—	V _x - 200	mV

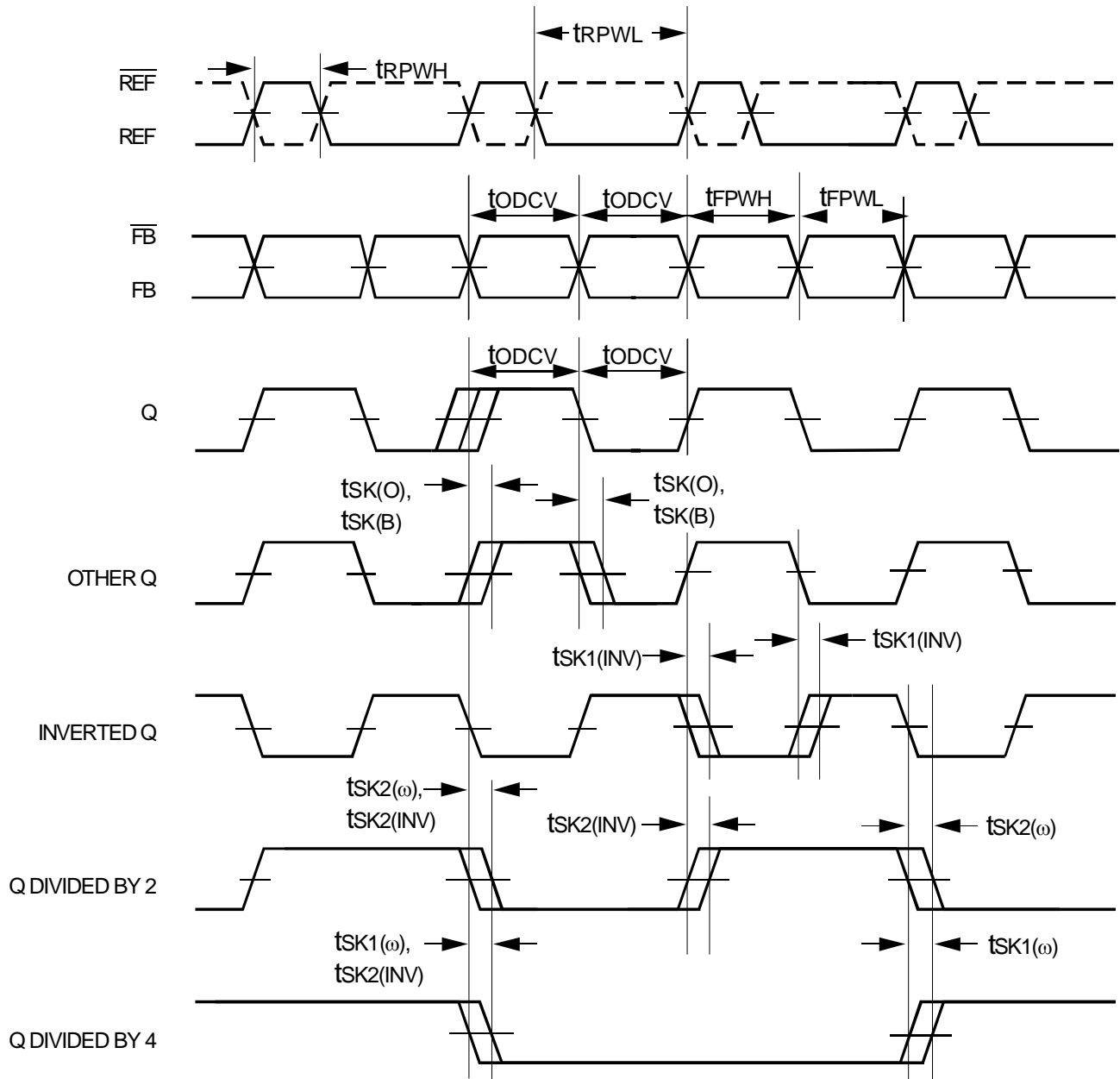
LVEPECL

V _{DIF}	AC Differential Voltage ⁽³⁾	400	—	—	mV
V _{IH}	AC Input HIGH ⁽⁴⁾	1275	—	—	mV
V _{IL}	AC Input LOW ⁽⁴⁾	—	—	875	mV

NOTES:

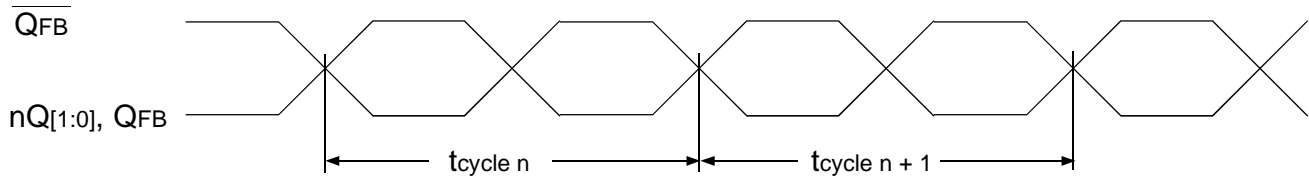
- For differential input mode, RxS is tied to GND.
- Both differential input signals should not be driven to the same level simultaneously. The input will not change state until the inputs have crossed and the voltage range defined by V_{DIF} has been met or exceeded.
- Differential mode only. V_{DIF} specifies the minimum input voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.
- For single-ended operation, $\overline{REF}_{[1:0]}/V_{REF[1:0]}$ is tied to the DC voltage V_{REF[1:0]}}. Refer to each input interface's DC specification for the correct V_{REF[1:0]}} range.
- Voltage required to switch to a logic HIGH, single-ended operation only.
- Voltage required to switch to a logic LOW, single-ended operation only.

AC TIMING DIAGRAM⁽¹⁾



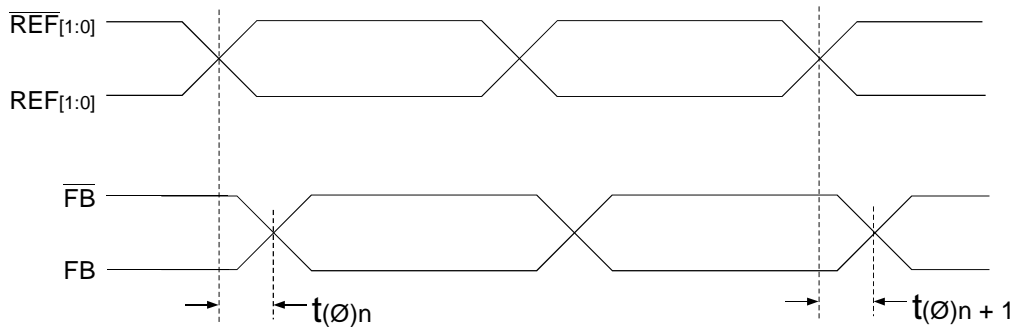
NOTE:
1. The AC TIMING DIAGRAM applies to PE = V_{DD}. For PE = GND, the negative edge of FB aligns with the negative edge of REF_[1:0], divided outputs change on the negative edge of REF_[1:0], and the positive edges of the divide-by-2 and divide-by-4 signals align.

JITTER AND OFFSET TIMING WAVEFORMS



$$t_{jit(cc)} = |t_{cycle\ n} - t_{cycle\ n+1}|$$

Cycle-to-Cycle jitter

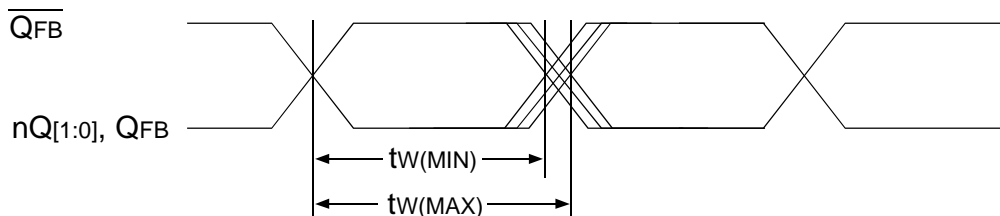


$$t(\emptyset) = \frac{\sum_{n=1}^{n=N} t(\emptyset)_n}{N}$$

(N is a large number of samples)

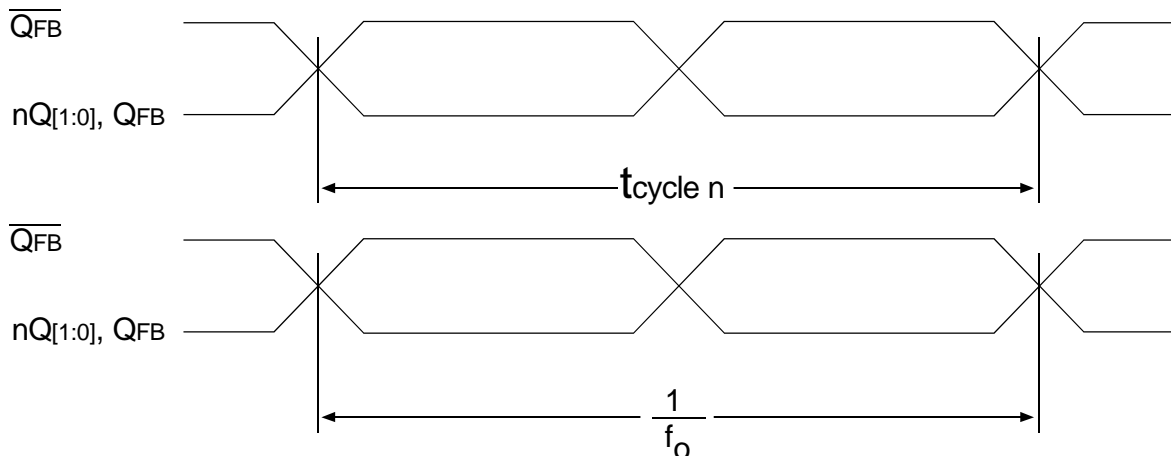
Static Phase Offset

NOTE:
1. Diagram for PE = H and TxS/RxS = L.



$$t_{JIT(DUTY)} = |t_{w(MAX)} - t_{w(MIN)}|$$

Duty-Cycle Jitter

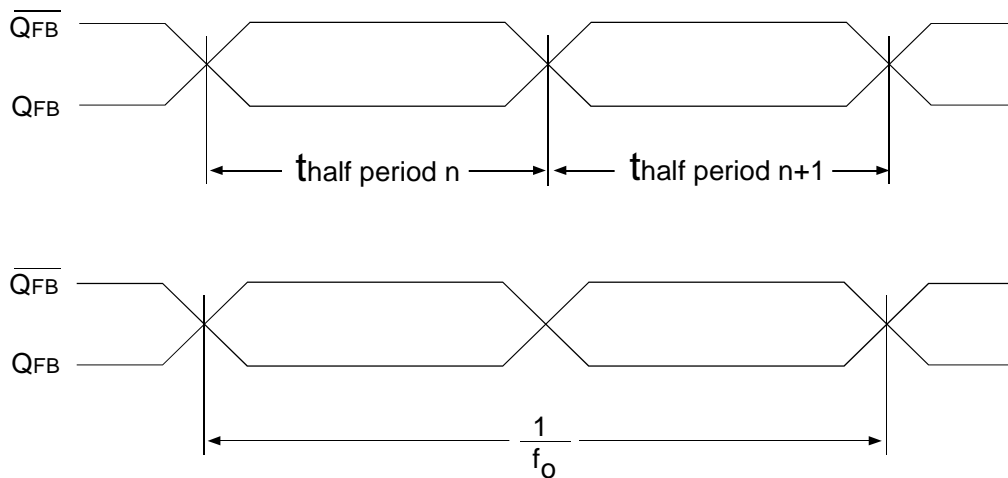


$$t_{jit(per)} = \left| t_{cycle\ n} - \frac{1}{f_o} \right|$$

Period jitter

NOTE:

1. $1/f_o$ = average period.



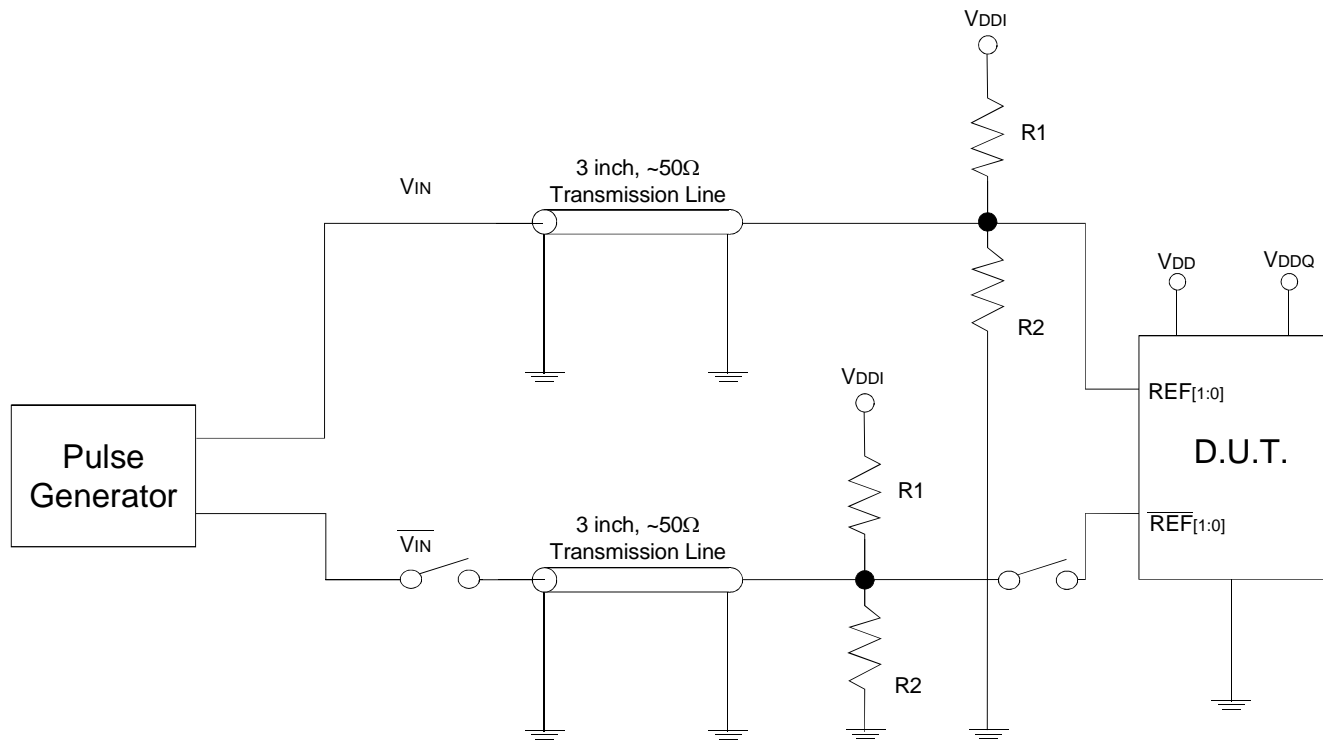
$$t_{jit(hper)} = \left| t_{half\ period\ n} - \frac{1}{2 \cdot f_o} \right|$$

Half-Period jitter

NOTE:

1. $1/f_o$ = average period.

TEST CIRCUITS AND CONDITIONS



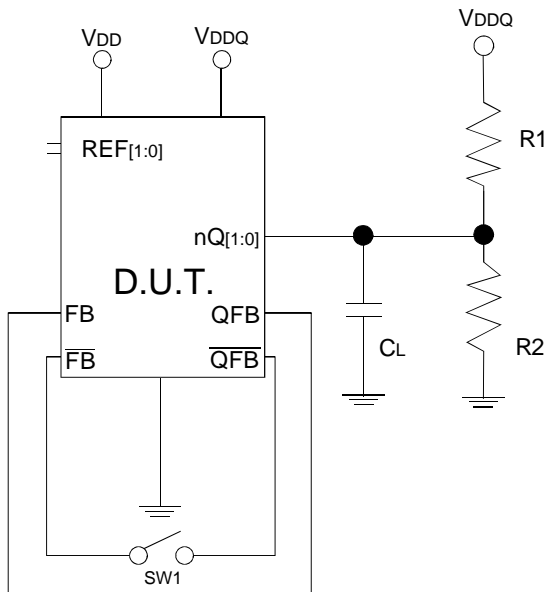
Test Circuit for Differential Input⁽¹⁾

DIFFERENTIAL INPUT TEST CONDITIONS

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
R1	100	Ω
R2	100	Ω
V_{DDI}	$V_{CM} \times 2$	V
V_{THI}	HSTL: Crossing of REF[1:0] and REB[1:0] eHSTL: Crossing of REF[1:0] and REB[1:0] LVEPECL: Crossing of REF[1:0] and REB[1:0] 1.8V LVTTTL: $V_{DDI}/2$ 2.5V LVTTTL: $V_{DD}/2$	V

NOTE:

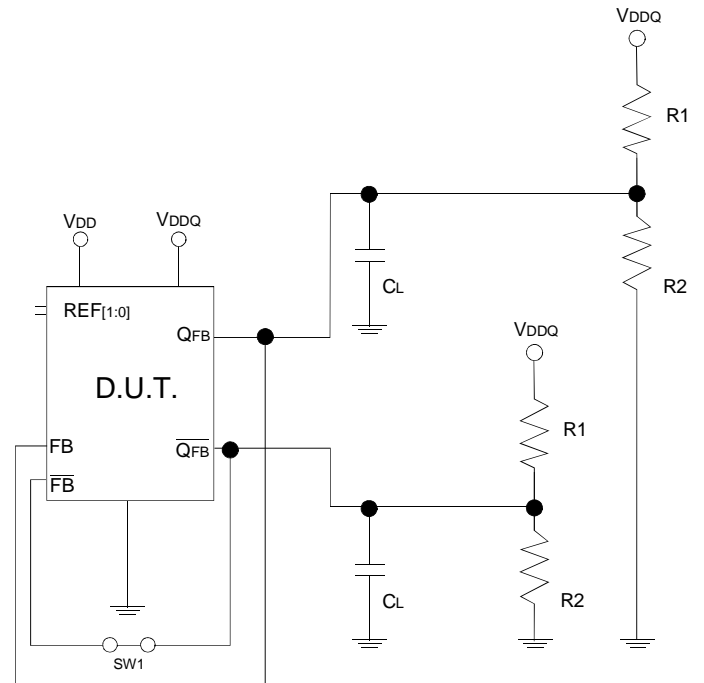
1. This input configuration is used for all input interfaces. For single-ended testing, the REB[1:0] must be left floating. For testing single-ended in differential input mode, the V-IN should be floating.



Test Circuit for Outputs

OUTPUT TEST CONDITIONS

Symbol	$V_{DD} = 2.5V \pm 0.2V$ $V_{DDQ} = \text{Interface Specified}$	Unit
C_L	15	pF
R1	100	Ω
R2	100	Ω
V_{TH0}	$V_{DDQ} / 2$	V
SW1	TxS = MID or HIGH	Open
	TxS = LOW	Closed

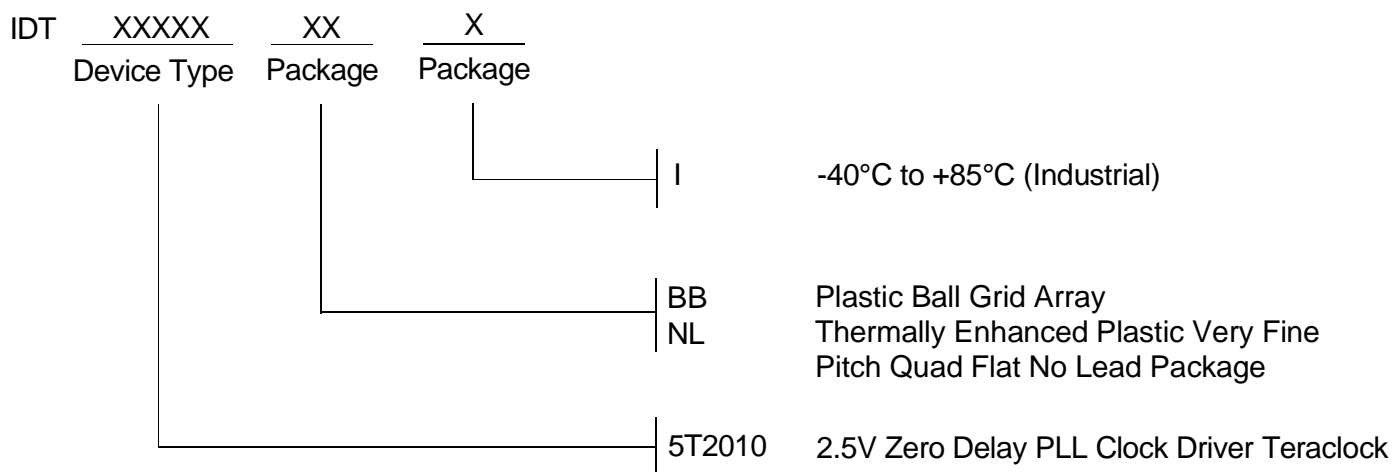


Test Circuit for Differential Feedback

DIFFERENTIAL FEEDBACK TEST CONDITIONS

Symbol	$V_{DD} = 2.5V \pm 0.2V$ $V_{DDQ} = \text{Interface Specified}$	Unit
C_L	15	pF
R1	100	Ω
R2	100	Ω
V_{ox}	HSTL: Crossing of QFB and \overline{QFB} eHSTL: Crossing of QFB and \overline{QFB}	V
V_{TH0}	1.8V LVTTL: $V_{DDQ}/2$ 2.5V LVTTL: $V_{DDQ}/2$	V
SW1	TxS = MID or HIGH	Open
	TxS = LOW	Closed

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