Integrated Circuit Systems, Inc.

# ICS8701-01
## LOW SKEW ÷1, ÷2 CLOCK GENERATOR W/POLARITY CONTROL

## GENERAL DESCRIPTION

The ICS8701-01 is a low skew, ÷1, ÷2 Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

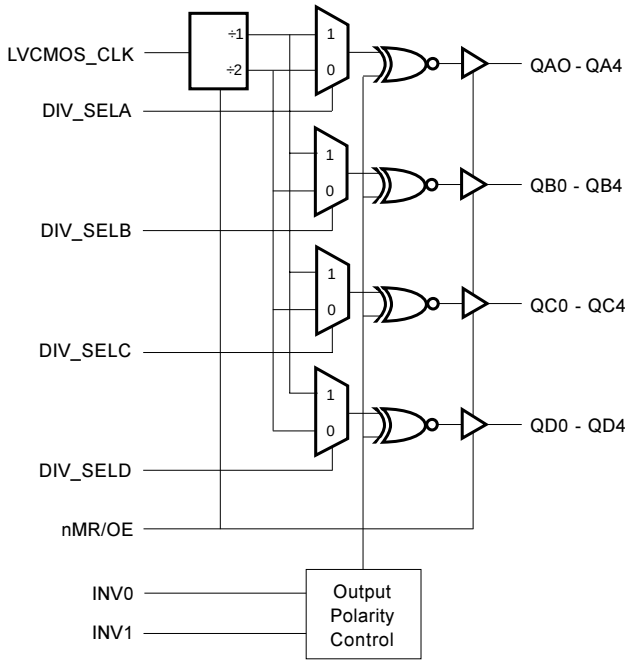
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset/output enable input, nMR/OE, resets the internal dividers and controls the active and high impedance states of all outputs. The output polarity inputs, INV0:1, control the polarity (inverting or non-inverting) of the outputs of each bank. Outputs QA0-QA4 are inverting for every combination of the INV0:1 input. The timing relationship between the inverting and non-inverting outputs at different frequencies is shown in the Timing Diagrams.

The ICS8701-01 is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output and part-to-part skew characteristics make the ICS8701-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

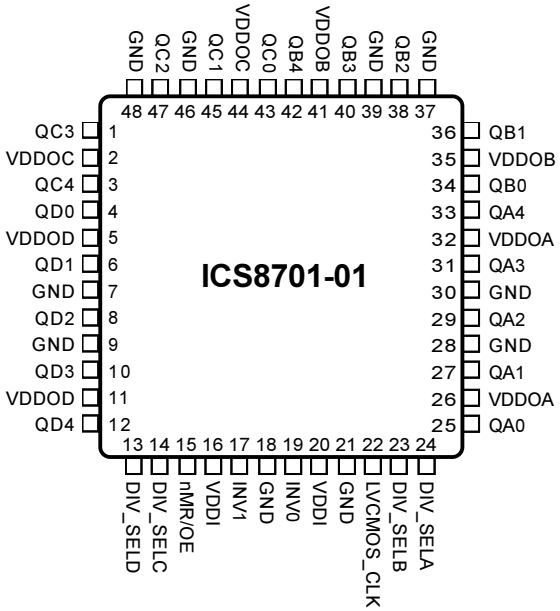
## FEATURES

- 20 LVCMOS outputs, 7Ω typical output impedance
- Output frequency up to 250 MHz
- 250ps bank skew, 300ps output skew, 350ps multiple frequency skew, 700ps part-to-part skew
- Selectable inverting and non-inverting outputs
- LVCMOS / LVTTL clock input
- LVCMOS / LVTTL control inputs
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- 3.3V or mixed 3.3V input, 2.5V output operating supply modes
- 48 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- 0°C to 70°C ambient operating temperature
- Other divide values available on request

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**48-Pin LQFP**
**Y Package**
Top View

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 2, 44 | VDDOC | Power | | Output Bank C power supply. Connect to 3.3V or 2.5V. |
| 5, 11 | VDDOD | Power | | Output Bank D power supply. Connect to 3.3V or 2.5V. |
| 26, 32 | VDDOA | Power | | Output Bank C power supply. Connect to 3.3V or 2.5V. |
| 35, 41 | VDDOB | Power | | Output Bank B power supply. Connect to 3.3V or 2.5V. |
| 7, 9, 18, 21, 28, 30, 37, 39, 46, 48 | GND | Power | | Ground. Connect to ground. |
| 16, 20 | VDDI | Power | | Input power supply. Connect to 3.3V. |
| 25, 27, 29, 31, 33 | QA0, QA1, QA2, QA3, QA4 | Output | | Bank A outputs. LVCMOS interface levels. 7Ω typical output impedance. |
| 34, 36, 38, 40, 42 | QB0, QB1, QB2, QB3, QB4 | Output | | Bank B outputs. LVCMOS interface levels. 7Ω typical output impedance. |
| 43, 45, 47, 1, 3 | QC0, QC1, QC2, QC3, QC4 | Output | | Bank C outputs. LVCMOS interface levels. 7Ω typical output impedance. |
| 4, 6, 8, 10, 12 | QD0, QD1, QD2, QD3, QD4 | Output | | Bank D outputs. LVCMOS interface levels. 7Ω typical output impedance. |
| 22 | LVCMOS_CLK | Input | Pullup | Clock input. LVCMOS interface levels. |
| 13 | DIV_SELD | Input | Pullup | Controls frequency division for bank D outputs. LVCMOS interface levels. |
| 14 | DIV_SELC | Input | Pullup | Controls frequency division for bank C outputs. LVCMOS interface levels. |
| 23 | DIV_SELB | Input | Pullup | Controls frequency division for bank B outputs. LVCMOS interface levels. |
| 24 | DIV_SELA | Input | Pullup | Controls frequency division for bank A outputs. LVCMOS interface levels. |
| 17, 19 | INV1, INV0 | Input | Pullup | Determines polarity of outputs by banks. LVCMOS interface levels. |
| 15 | nMR/OE | Input | Pullup | Master reset and output enable. Resets non-inverting outputs to LOW. Sets inverting outputs to HIGH. Enables and disables all outputs. LVCMOS interface levels. |

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | | | | | pF |
| RPULLUP | Input Pullup Resistor | | | 51 | | KΩ |
| CPD | Power Dissipation Capacitance (per output) | VDDI, VDDOx = 3.465V | | | | pF |
| | | VDDI = 3.465V, VDDOx = 2.625V | | | | pF |
| ROUT | Output Impedance | | | 7 | | Ω |

**TABLE 3. FUNCTION TABLE**

| Inputs | | | | Outputs | | | | |
|---|---|---|---|---|---|---|---|---|
| nMR/OE | DIV_SELx | INV1 | INV0 | BANK A | BANK B | BANK C | BANK D | Qx frequency |
| 0 | X | X | X | Hi Z | Hi Z | Hi Z | Hi Z | zero |
| 1 | 0 | 0 | 0 | Inverting | Non-inverting | Non-inverting | Non-inverting | fIN/2 |
| 1 | 0 | 0 | 1 | Inverting | Inverting | Non-inverting | Non-inverting | fIN/2 |
| 1 | 0 | 1 | 0 | Inverting | Inverting | Inverting | Non-inverting | fIN/2 |
| 1 | 0 | 1 | 1 | Inverting | Inverting | Inverting | Inverting | fIN/2 |
| 1 | 1 | 0 | 0 | Inverting | Non-inverting | Non-inverting | Non-inverting | fIN |
| 1 | 1 | 0 | 1 | Inverting | Inverting | Non-inverting | Non-inverting | fIN |
| 1 | 1 | 1 | 0 | Inverting | Inverting | Inverting | Non-inverting | fIN |
| 1 | 1 | 1 | 1 | Inverting | Inverting | Inverting | Inverting | fIN |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage | 4.6V |
| Inputs | -0.5V to VDDI + 0.5V |
| Outputs | -0.5V to VDDOx + 0.5V |
| Ambient Operating Temperature | 0°C to 70°C |
| Storage Temperature | -65°C to 150°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. DC ELECTRICAL CHARACTERISTICS,** VDDI = VDDOx = 3.3V±5%, TA = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| VDDI | Input Power Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| VDDOx | Output Power Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| VIH | Input High Voltage | All except LVCMOS_CLK | VDDI = 3.465V | 2 | | 3.765 | V |
| | | LVCMOS_CLK | | 2 | | 3.765 | V |
| VIL | Input Low Voltage | All except LVCMOS_CLK | VDDI = 3.135V | -0.3 | | 0.8 | V |
| | | LVCMOS_CLK | | -0.3 | | 1.3 | V |
| IIH | Input High Current | | VDDI = VIN = 3.465V | | | 5 | µA |
| IIL | Input Low Current | | VDDI = VIN = 0V | -150 | | | µA |
| IDD | Quiescent Power Supply Current | | | | | 70 | mA |
| VOH | Output High Voltage | | VDDOx = 3.135V<br>IOH = -36mA | 2.6 | | | V |
| VOL | Output Low Voltage | | VDDOx =3.135V<br>IOL = 36mA | | | 0.5 | V |

**TABLE 5A. AC ELECTRICAL CHARACTERISTICS,** VDDI = VDDOx = 3.3V±5%, TA=0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| fMAX | Maximum Input Frequency | | | | 250 | MHz |
| tpLH | Propagation Delay, Low-to-High | 0MHZ < f ≤ 200MHz | 2.5 | | 3.5 | ns |
| tpHL | Propagation Delay, High-to-Low | 0MHZ < f ≤ 200MHz | 2.5 | | 3.5 | ns |
| tsk(b) | Bank Skew; NOTE 2 | Measured on falling edge at VDDOx/2 | | | 250 | ps |
| tsk(o) | Output Skew; NOTE 3 | Measured on falling edge at VDDOx/2 | | | 300 | ps |
| tsk(ω) | Multiple Frequency Skew; NOTE 4 | Measured on falling edge at VDDOx/2 | | | 350 | ps |
| tsk(pp) | Part to Part Skew; NOTE 5 | Measured on falling edge at VDDOx/2 | | | 700 | ps |
| tR | Output Rise Time; NOTE 6 | | 150 | | 700 | ps |
| tF | Output Fall Time; NOTE 6 | | 150 | | 700 | ps |
| tPW | Output Pulse Width | 0MHZ < f < 200MHz | tCYCLE/2 - 0.5 | tCYCLE/2 | tCYCLE/2 + 0.5 | ns |
| | | f = 200MHz | 2 | 2.5 | 3 | ns |
| tEN | Output Enable Time; NOTE 6 | | | | 6 | ns |
| tDIS | Output Disable Time; NOTE 6 | | | | 6 | ns |

NOTE 1: All parameters measured at 200MHz unless noted otherwise. All outputs terminated with 50Ω to VDDOx/2.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs switching in the same direction at the same supply voltages and with equal load conditions.
NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew at different outputs switching in the same direction on different devices operating at the same supply voltages and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**TABLE 4B. DC ELECTRICAL CHARACTERISTICS,** VDDI = 3.3V±5%, VDDOx = 2.5V±5%, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| VDDI | Input Power Supply Voltage | | | 3.135 | 3.3 | 3.465 | V |
| VDDOx | Output Power Supply Voltage | | | 2.375 | 2.5 | 2.625 | V |
| VIH | Input High Voltage | All except LVCMOS_CLK | VDDI = 3.465V | 2 | | 3.765 | V |
| | | LVCMOS_CLK | | 2 | | 3.765 | V |
| VIL | Input Low Voltage | All except LVCMOS_CLK | VDDI = 3.135V | -0.3 | | 0.8 | V |
| | | LVCMOS_CLK | | -0.3 | | 1.3 | V |
| IIH | Input High Current | | VDDI = VIN = 3.465V | | | 5 | µA |
| IIL | Input Low Current | | VDDI = VIN = 0V | -150 | | | µA |
| IDD | Quiescent Power Supply Current | | | | | 70 | mA |
| VOH | Output High Voltage | | VDDI = 3.135V<br>VDDOx = 2.375V<br>IOH = -27mA | 1.8 | | | V |
| VOL | Output Low Voltage | | VDDI =3.135V<br>VDDOx = 2.375V<br>IOL = 27mA | | | 0.5 | V |

**TABLE 5B. AC ELECTRICAL CHARACTERISTICS,** VD DI = 3.3V±5%, VDDO = 2.5V±5%, $T_A$ = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| fMAX | Maximum Input Frequency | | | | 250 | MHz |
| tpLH | Propagation Delay, Low-to-High | 0MHZ < f ≤ 200MHz | 2.5 | | 3.5 | ns |
| tpHL | Propagation Delay, High-to-Low | 0MHZ < f ≤ 200MHz | 2.5 | | 3.5 | ns |
| tsk(b) | Bank Skew; NOTE 2 | Measured on falling edge at VDDOx/2 | | | 300 | ps |
| tsk(o) | Output Skew; NOTE 3 | Measured on falling edge at VDDOx/2 | | | 300 | ps |
| tsk(ω) | Multiple Frequency Skew; NOTE 4 | Measured on falling edge at VDDOx/2 | | | 350 | ps |
| tsk(pp) | Part to Part Skew; NOTE 5 | Measured on falling edge at VDDOx/2 | | | 700 | ps |
| tR | Output Rise Time; NOTE 6 | | 150 | | 720 | ps |
| tF | Output Fall Time; NOTE 6 | | 150 | | 720 | ps |
| tPW | Output Pulse Width | 0MHZ < f < 200MHz | tCYCLE/2 - 0.5 | tCYCLE/2 | tCYCLE/2 + 0.5 | ns |
| | | f = 200MHz | 2 | 2.5 | 3 | ns |
| tEN | Output Enable Time; NOTE 6 | | | | 6 | ns |
| tDIS | Output Disable Time; NOTE 6 | | | | 6 | ns |

NOTE 1: All parameters measured at 200MHz unless noted otherwise. All outputs terminated with 50Ω to VDDOx/2.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs switching in the same direction at the same supply voltages and with equal load conditions.
NOTE 4: Defined as skew across banks of outputs switching in the same direction operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew at different outputs switching in the same direction on different devices operating at the same supply voltages and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

**FIGURE 1A, 1B - TIMING DIAGRAMS**

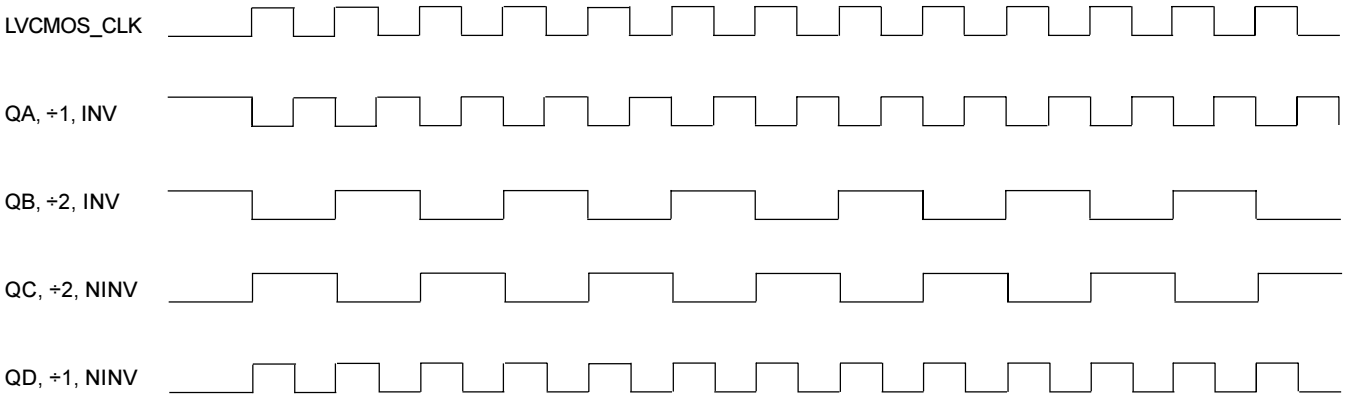



**FIGURE 1A - ACTIVE, ÷1, ÷2, INVERTING AND NON-INVERTING**

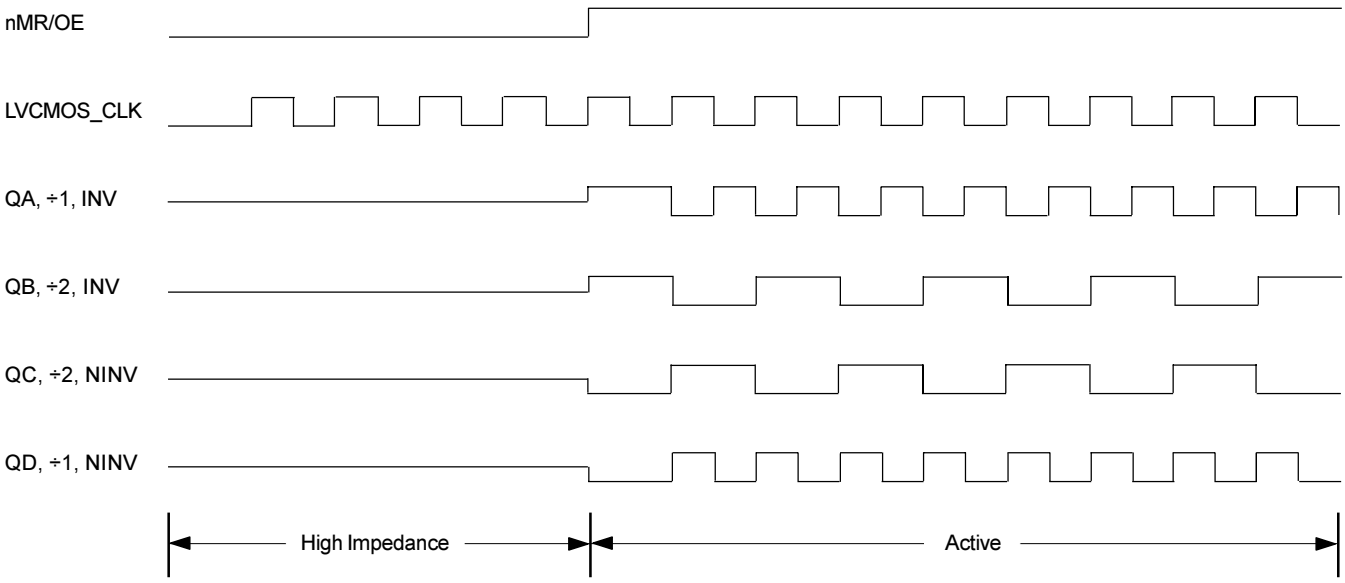



**FIGURE 1B - RESET TO ACTIVE, ÷1, ÷2, INVERTING AND NON-INVERTING**

**FIGURE 2A, 2B - TIMING WAVEFORMS**

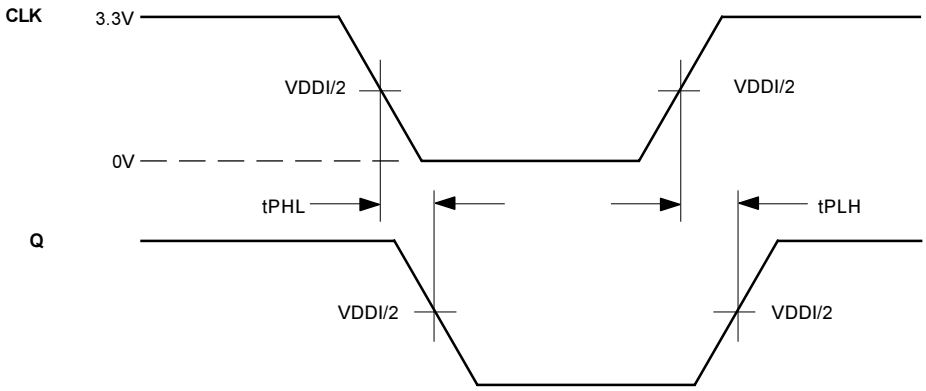



**FIGURE 2A - PROPAGATION DELAYS**

fin = 200MHz, Vamp = 3.3V, tr = tf = 600ps

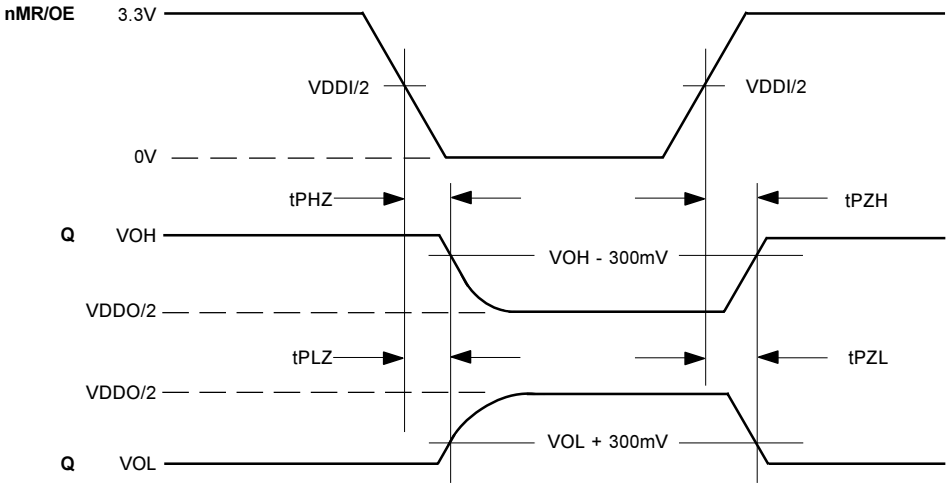



**FIGURE 2B - DISABLE AND ENABLE TIMES**

fin = 10MHz, Vamp = 3.3V, tr = tf = 600ps

**FIGURE 3A, 3B- SKEW DEFINITIONS & WAVEFORMS**

**Bank Skew -** Skew within a bank of outputs at the same supply voltages and with equal load conditions.

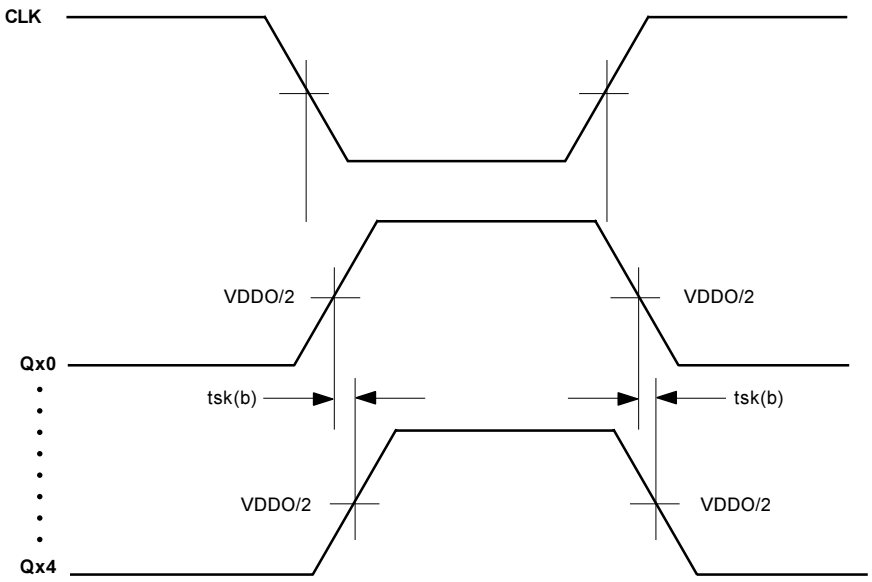



**FIGURE 3A - BANK SKEW**

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

**Output Skew -** Skew across banks of outputs switching in the same direction at the same supply voltages and with equal load conditions.

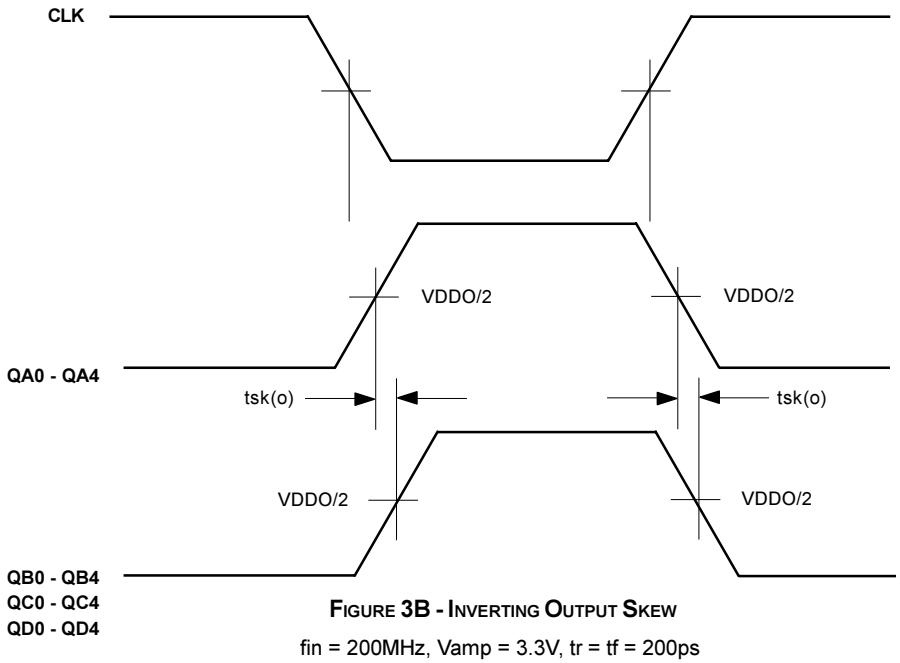



**FIGURE 3B - INVERTING OUTPUT SKEW**

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

**FIGURE 3C, 3D- SKEW DEFINITIONS & WAVEFORMS**

**Multiple Frequency Skew -** Skew across banks of outputs switching in the same direction operating at different frequencies with the same supply voltages and equal load conditions.

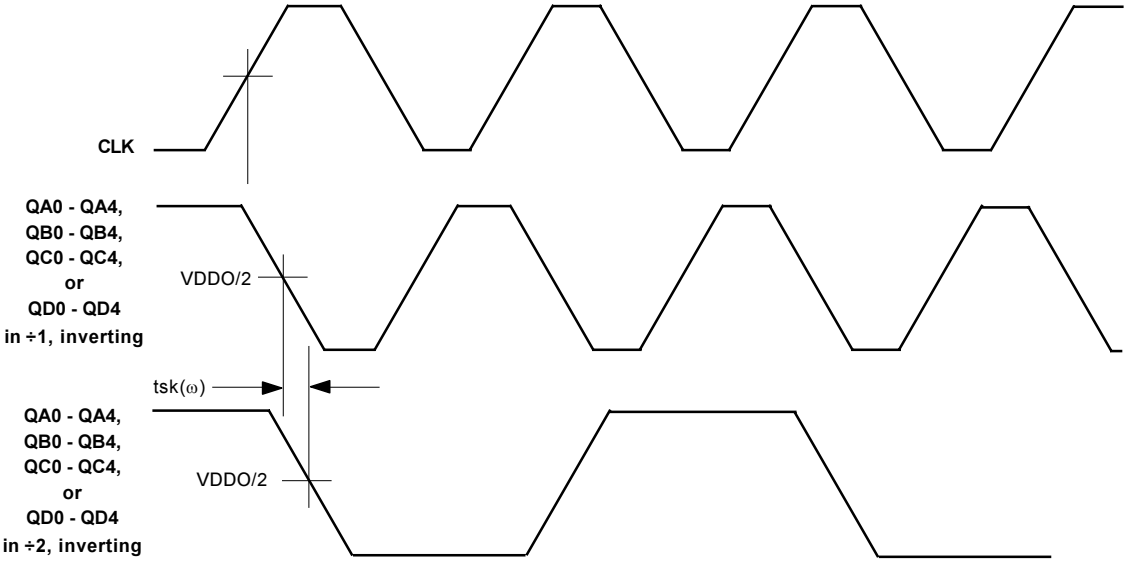



**FIGURE 3C - MULTIPLE FREQUENCY SKEW**

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

**Part to Part Skew -** Skew at different outputs switching in the same direction on different devices operating at the same supply voltages and with equal load conditions.

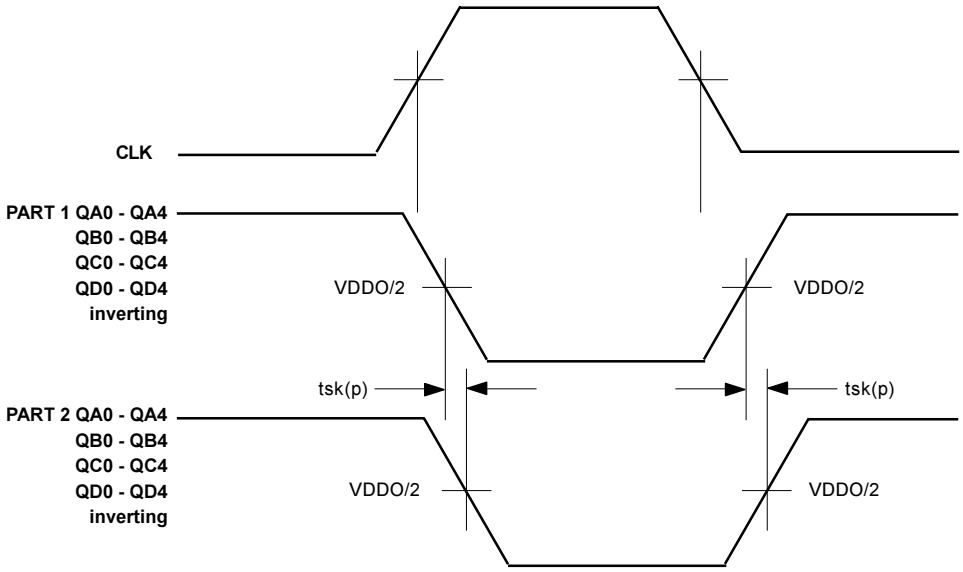
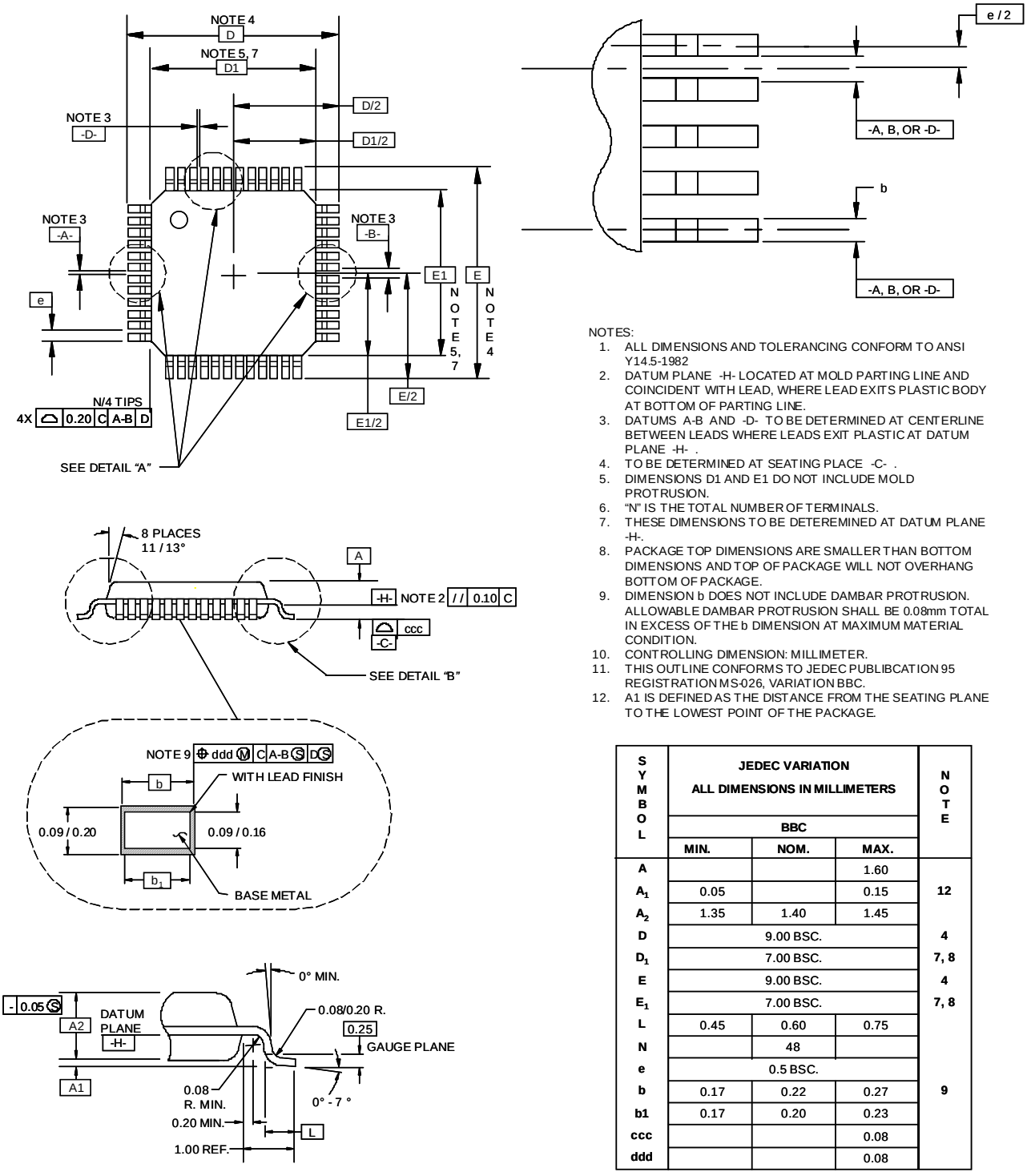



**FIGURE 3B - OUTPUT SKEW**

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

## PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX




NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLACE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETEREMINED AT DATUM PLANE -H-.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
10. CONTROLLING DIMENSION: MILLIMETER.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLIBCATION 95 REGISTRATION MS-026, VARIATION BBC.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.

| SYMBOL | JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | BBC | | | |
| | MIN. | NOM. | MAX. | |
| A | | | 1.60 | |
| $A_1$ | 0.05 | | 0.15 | 12 |
| $A_2$ | 1.35 | 1.40 | 1.45 | |
| D | | 9.00 BSC. | | 4 |
| $D_1$ | | 7.00 BSC. | | 7, 8 |
| E | | 9.00 BSC. | | 4 |
| $E_1$ | | 7.00 BSC. | | 7, 8 |
| L | 0.45 | 0.60 | 0.75 | |
| N | | 48 | | |
| e | | 0.5 BSC. | | |
| b | 0.17 | 0.22 | 0.27 | 9 |
| b1 | 0.17 | 0.20 | 0.23 | |
| ccc | | | 0.08 | |
| ddd | | | 0.08 | |

## ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS8701-01Y | ICS8701-01 | 48 Lead LQFP | 250 per tray | 0°C to 70°C |
| ICS8701-01YT | ICS8701-01 | 48 Lead LQFP on Tape and Reel | 2000 | 0°C to 70°C |