

HYS[64/72]D64x20HU-[5/6]-C  
HYS[64/72]D32x00HU-[5/6]-C  
HYS64D16x01HU-[5/6]-C

184-Pin Unbuffered Dual-In-Line Memory Modules  
Reg DIMM  
DDR SDRAM

Memory Products



N e v e r   s t o p   t h i n k i n g .

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Never stop thinking.

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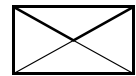
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Page	Subjects (major changes since last revision)
all	new data sheet template

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## 184-Pin Unbuffered Dual-In-Line Memory Modules Reg DIMM

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HYS64D16x01HU-[5/6]-C

# 1 Overview

## 1.1 Features

- 184-Pin Unbuffered Dual-In-Line Memory Modules (ECC and non-parity) for PC and Server main memory applications
- One rank 16M x 64, 32M x 64, 32M x 72 and two ranks 64M x 64, 64M x 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) Single +2.5V ( $\pm 0.2V$ ) power supply
- Built with 256 Mbit DDR SDRAM in P-TSOPII-66-1 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL\_2 compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- JEDEC standard MO-206 form factor: 133.35 mm x 31.75 mm x 4.00 mm max.
- Jedec standard reference layout
- Gold plated contacts
- DDR400 Speed Grade supported
- Lead-free

**Table 1 Performance**

Part Number Speed Code			-5	-6	Unit
Module Speed Grade			DDR400B	DDR333B	–
Component Module			PC3200-3033	PC2700-2533	–
max. Clock Frequency	@ CL = 3	$f_{CK3}$	200	166	MHz
	@ CL = 2.5	$f_{CK2.5}$	166	166	MHz
	@ CL = 2	$f_{CK2}$	133	133	MHz

## 1.2 Description

The HYS[64/72]D64x20HU-[5/6]-C, HYS[64/72]D32x00HU-[5/6]-C, and HYS64D16x01HU-[5/6]-C are industry standard 184-Pin Unbuffered Dual-In-Line Memory Modules (Reg DIMM) organized as 16M x 64, 32M x 64 and 64M x 64 for non-parity and 32M x 72 and 64M x 72 for ECC main memory applications. The memory array is designed with 256Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the printed circuit board. The DIMMs feature serial presence detect (SPD) based on a serial E<sup>2</sup>PROM device using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer

Table 2 Ordering Information



Type	Compliance Code	Description	SDRAM Technology
<b>PC3200 (CL=3)</b>			
HYS64D16301HU-5-C	PC3200U-30330-C0	one rank 128MB DIMM	256 Mbit (× 16)
HYS64D32300HU-5-C	PC3200U-30330-A0	one rank 256MB DIMM	256 Mbit (× 8)
HYS72D32300HU-5-C	PC3200U-30330-A0	one rank 256MB ECC-DIMM	256 Mbit (× 8)
HYS64D64320HU-5-C	PC3200U-30330-B0	two ranks 512MB DIMM	256 Mbit (× 8)
HYS72D64320HU-5-C	PC3200U-30330-B0	two ranks 512MB ECC-DIMM	256 Mbit (× 8)
<b>PC2700 (CL=2.5)</b>			
HYS64D16301HU-6-C	PC2700U-25330-C0	one rank 128MB DIMM	256 Mbit (× 16)
HYS64D32300HU-6-C	PC2700U-25330-A0	one rank 256MB DIMM	256 Mbit (× 8)
HYS72D32300HU-6-C	PC2700U-25330-A0	one rank 256MB ECC-DIMM	256 Mbit (× 8)
HYS64D64320HU-6-C	PC2700U-25330-B0	two ranks 512MB DIMM	256 Mbit (× 8)
HYS72D64320HU-6-C	PC2700U-25330-B0	two ranks 512MB ECC-DIMM	256 Mbit (× 8)

Note: All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D32000HU-6-C, indicating rev. C dies are used for SDRAM components. The Compliance Code is printed on the module labels describing the speed sort (for example "PC2700"), the latencies and SPD code definition (for example "20330" means CAS latency of 2.0 clocks, RCD<sup>1)</sup> latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definition version 0), and the Raw Card used for this module.

1) RCD: Row-Column-Delay

## 2 Pin Configuration

**Table 3 Pin Definitions and Functions**

Symbol	Type <sup>1)</sup>	Function
A0 - A12	I	Address Inputs
BA0, BA1	I	Bank Selects
DQ0 - DQ63	I/O	Data Input/Output
CB0 - CB7	I/O	Check Bits (× 72 organization only)
$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	I	Command Inputs
CKE0 - CKE1	I	Clock Enable
DQS0 - DQS8	I/O	SDRAM low data strobes
CK0 - CK2,	I	SDRAM clock (positive lines)
$\overline{\text{CK0}}$ - $\overline{\text{CK2}}$	I	SDRAM clock (negative lines)
DM0 - DM8	I	SDRAM low data mask/ high data strobes
DQS9 - DQS17	I/O	
$\overline{\text{S0}}$ , $\overline{\text{S1}}$	I	Chip Selects for Rank0 and Rank1
$V_{\text{DD}}$	PWR	Power (+2.5 V)
$V_{\text{SS}}$	GND	Ground
$V_{\text{DDQ}}$	PWR	I/O Driver power supply
$V_{\text{DDID}}$	PWR	VDD Identification flag
$V_{\text{REF}}$	AI	I/O reference supply
$V_{\text{DDSPD}}$	PWR	Serial EEPROM power supply
SCL	I	Serial bus clock
SDA	I/O	Serial bus data line
SA0 - SA2	I	slave address select
NC	NC	Not Connected

1) I: Input; O: Output; I/O: bidirectional In-/Output; AI: Analog Input; PWR: Power Supply; GND: Signal Ground; NC: Not Connected

*Note: S1 and CKE1 are used on two rank modules only*



Table 4 Pin Configuration

Frontside				Backside			
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	$V_{REF}$	48	A0	93	$V_{SS}$	140	NC / DM8/DQS17
2	DQ0	49	NC / CB2	94	DQ4	141	A10
3	$V_{SS}$	50	$V_{SS}$	95	DQ5	142	NC / CB6
4	DQ1	51	NC / CB3	96	$V_{DDQD}$	143	$V_{DDQD}$
5	DQS0	52	BA1	97	DM0/DQS9	144	NC / CB7
6	DQ2	<b>Key</b>		98	DQ6	<b>Key</b>	
7	$V_{DD}$			99	DQ7		
8	DQ3	53	DQ32	100	$V_{SS}$	145	$V_{SS}$
9	NC	54	$V_{DDQ}$	101	NC	146	DQ36
10	NC	55	DQ33	102	NC	147	DQ37
11	$V_{SS}$	56	DQS4	103	NC	148	$V_{DD}$
12	DQ8	57	DQ34	104	$V_{DDQ}$	149	DM4/DQS13
13	DQ9	58	$V_{SS}$	105	DQ12	150	DQ38
14	DQS1	59	BA0	106	DQ13	151	DQ39
15	$V_{DDQ}$	60	DQ35	107	DM1/DQS10	152	$V_{SS}$
16	CK1	61	DQ40	108	$V_{DD}$	153	DQ44
17	CK1	62	$V_{DDQ}$	109	DQ14	154	$\overline{RAS}$
18	$V_{SS}$	63	$\overline{WE}$	110	DQ15	155	DQ45
19	DQ10	64	DQ41	111	CKE1	156	$V_{DDQ}$
20	DQ11	65	$\overline{CAS}$	112	$V_{DDQ}$	157	$\overline{S0}$
21	CKE0	66	$V_{SS}$	113	NC (BA2)	158	$\overline{S1}$
22	$V_{DDQ}$	67	DQS5	114	DQ20	159	DM5/DQS14
23	DQ16	68	DQ42	115	NC / A12	160	$V_{SS}$
24	DQ17	69	DQ43	116	$V_{SS}$	161	DQ46
25	DQS2	70	$V_{DD}$	117	DQ21	162	DQ47
26	$V_{SS}$	71	NC	118	A11	163	NC
27	A9	72	DQ48	119	DM2/DQS11	164	$V_{DDQ}$
28	DQ18	73	DQ49	120	$V_{DD}$	165	DQ52
29	A7	74	$V_{SS}$	121	DQ22	166	DQ53
30	$V_{DDQ}$	75	CK2	122	A8	167	NC (A13)
31	DQ19	76	CK2	123	DQ23	168	$V_{DD}$
32	A5	77	$V_{DDQ}$	124	$V_{SS}$	169	DM6/DQS15
33	DQ24	78	DQS6	125	A6	170	DQ54
34	$V_{SS}$	79	DQ50	126	DQ28	171	DQ55
35	DQ25	80	DQ51	127	DQ29	172	$V_{DDQ}$
36	DQS3	81	$V_{SS}$	128	$V_{DDQ}$	173	NC
37	A4	82	$V_{DDID}$	129	DM3/DQS12	174	DQ60
38	$V_{DD}$	83	DQ56	130	A3	175	DQ61
39	DQ26	84	DQ57	131	DQ30	176	$V_{SS}$

**Table 4 Pin Configuration (cont'd)**

Frontside				Backside			
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
40	DQ27	85	V <sub>DD</sub>	132	V <sub>SS</sub>	177	DM7/DQS16
41	A2	86	DQS7	133	DQ31	178	DQ62
42	V <sub>SS</sub>	87	DQ58	134	NC / CB4	179	DQ63
43	A1	88	DQ59	135	NC / CB5	180	V <sub>DDQ</sub>
44	NC / CB0	89	V <sub>SS</sub>	136	V <sub>DDQ</sub>	181	SA0
45	NC / CB1	90	NC	137	CK0	182	SA1
46	V <sub>DD</sub>	91	SDA	138	$\overline{\text{CK0}}$	183	SA2
47	NC / DQS8	92	SCL	139	V <sub>SS</sub>	184	V <sub>DDSPD</sub>

Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC ("not connected") on ×64 organised non-ECC modules.

**Table 5 Address Format**

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
128MB	16M × 64	1	16M × 16	4	13/2/10	8K	64 ms	7.8 μs
256MB	32M × 64	1	32M × 8	8	13/2/11	8K	64 ms	7.8 μs
256MB	32M × 72	1	32M × 8	9	13/2/11	8K	64 ms	7.8 μs
512MB	64M × 64	2	32M × 8	16	13/2/11	8K	64 ms	7.8 μs
512MB	64M × 72	2	32M × 8	18	13/2/11	8K	64 ms	7.8 μs

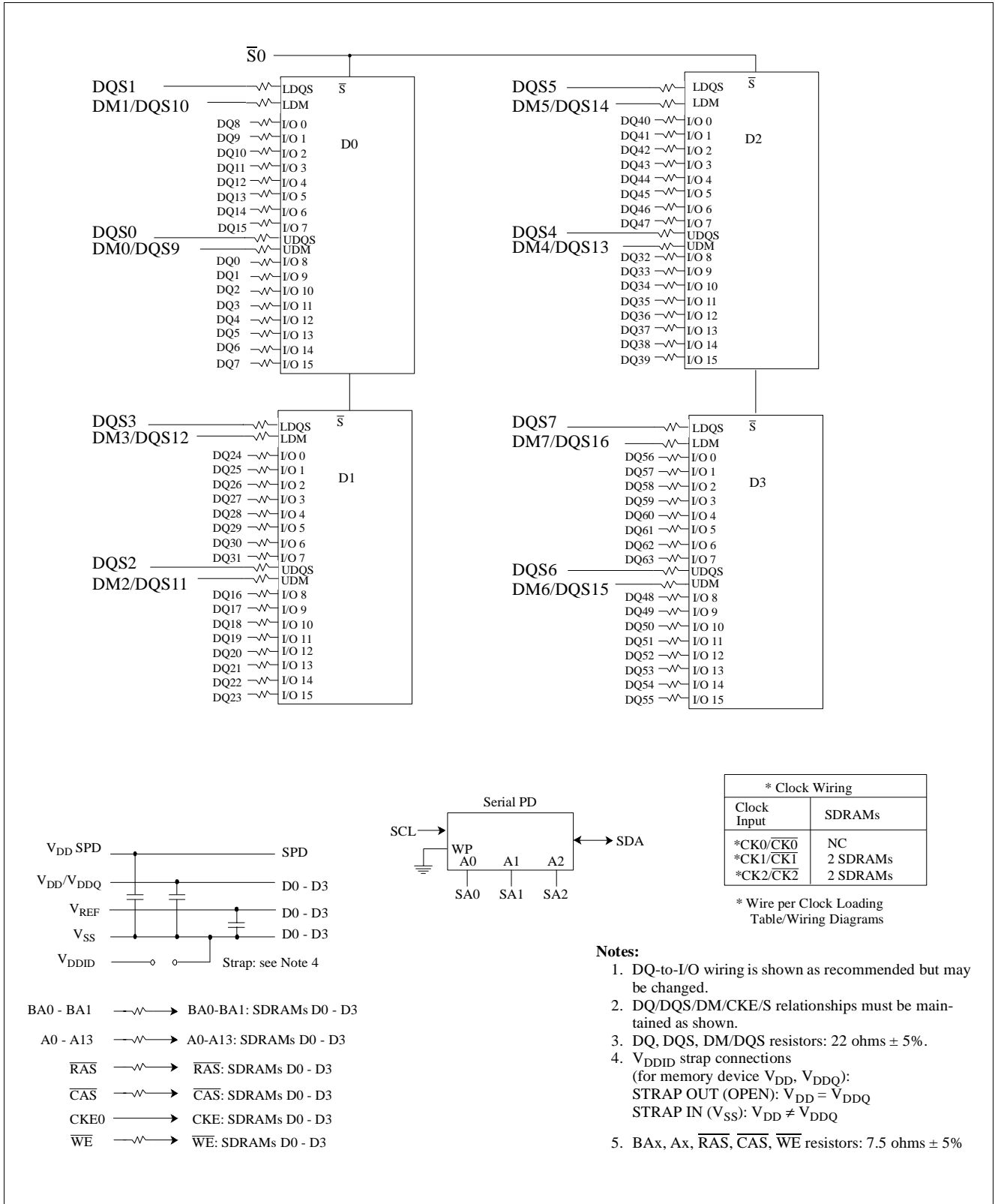
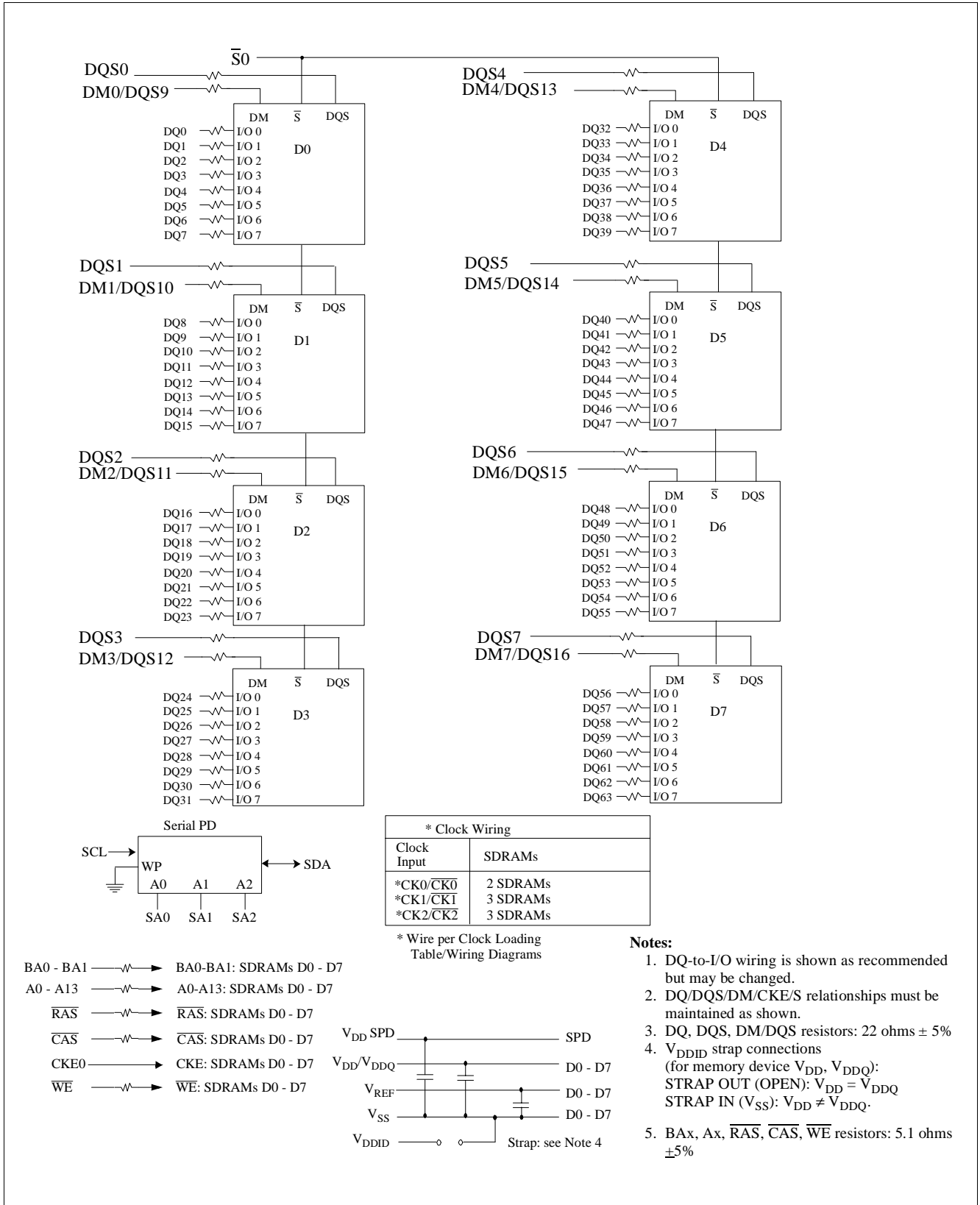


Figure 1 Block Diagram - One Rank 16M × 64 DDR SDRAM DIMM HYS64D16301GU using × 16 organized SDRAMs



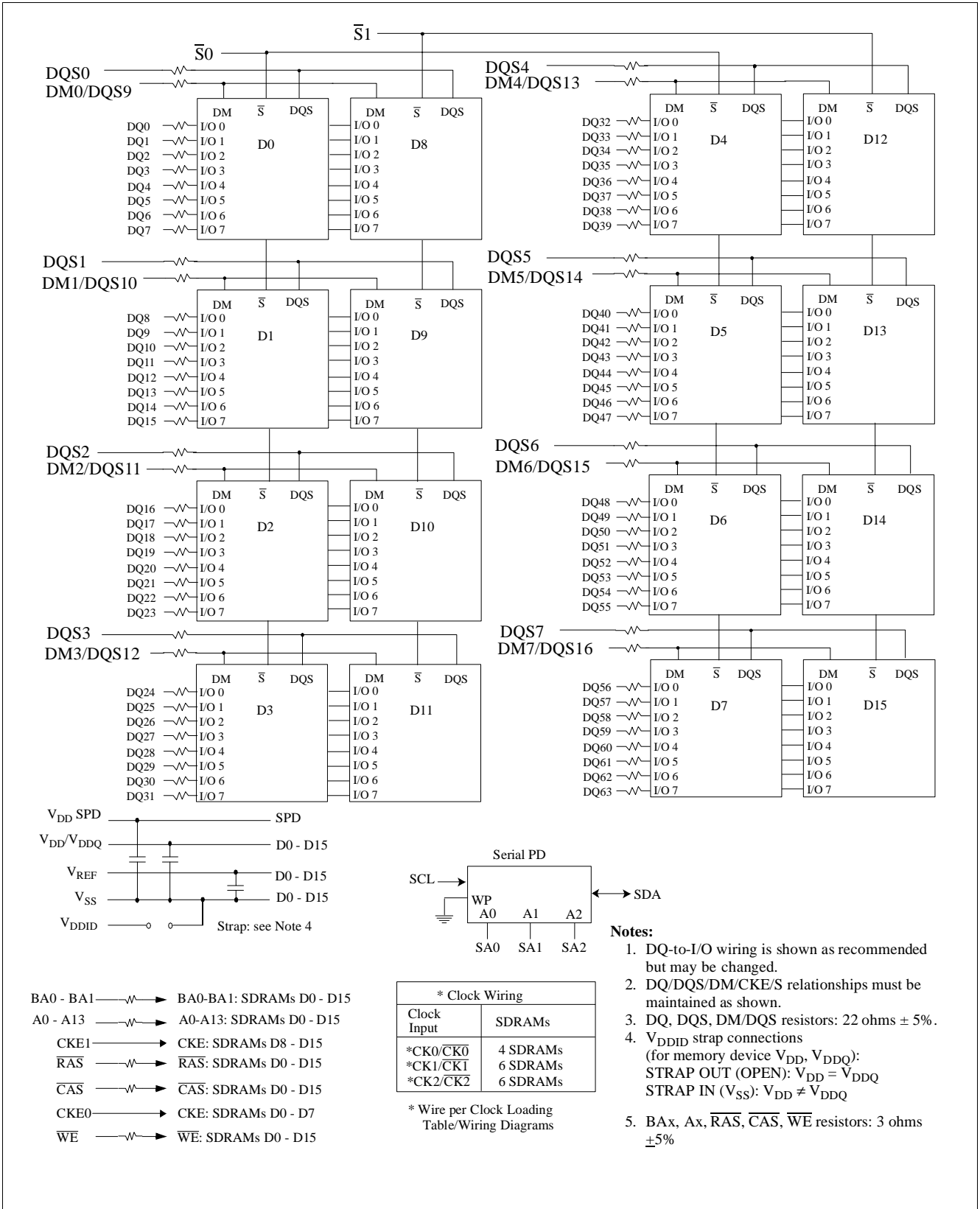


Figure 3 Block Diagram - Two Rank 64M x 64 DDR-I SDRAM DIMM HYS64D64x20GU using x8 Organized SDRAMs

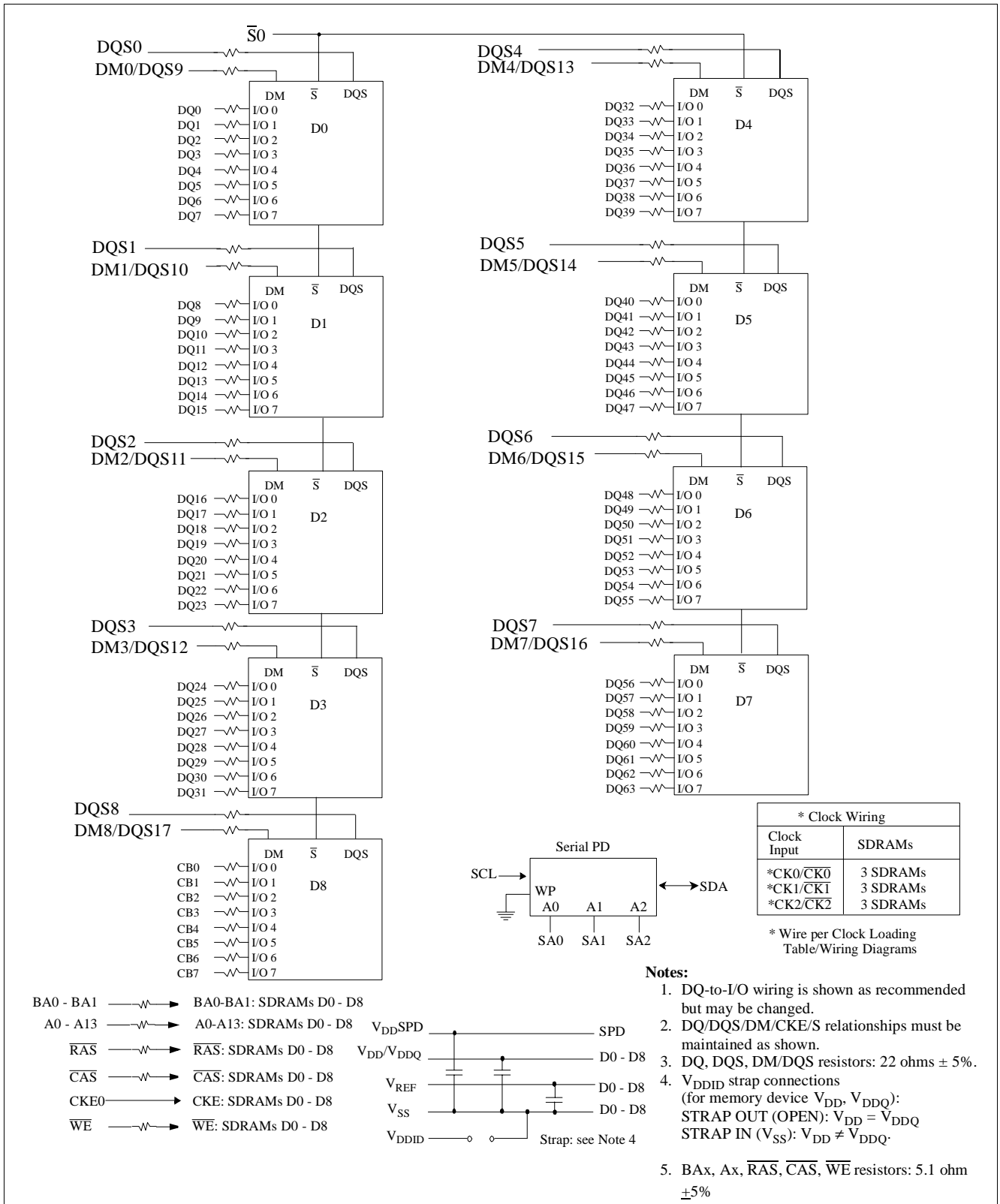


Figure 4 Block Diagram - One Rank 32M x 72 DDR-I SDRAM DIMM HYS72D32x00GU using x8 organized SDRAMs

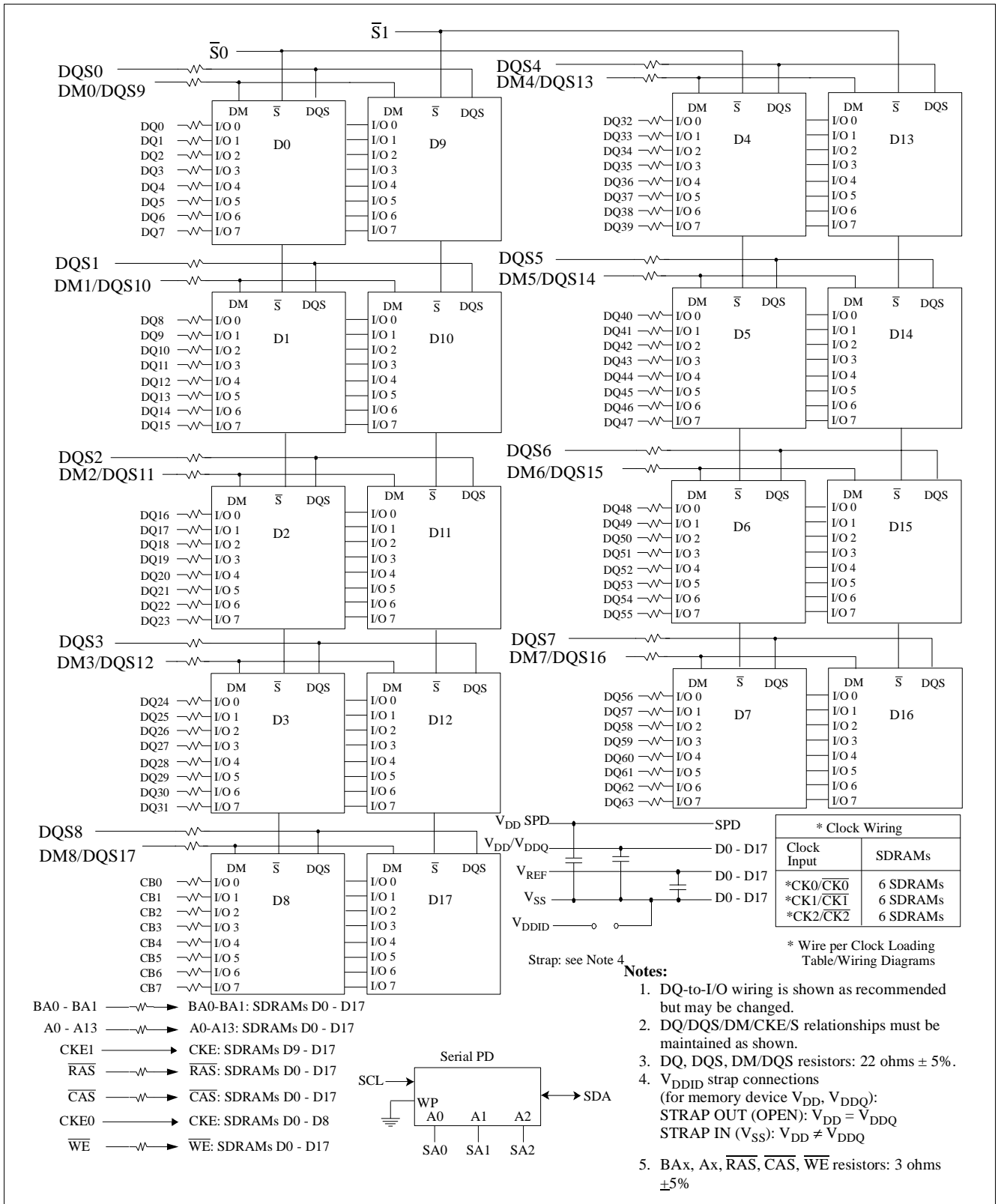


Figure 5 Block Diagram - Two Rank 64M x 72 DDR-I SDRAM DIMM HYS72D64x20GU using x8 Organized SDRAMs

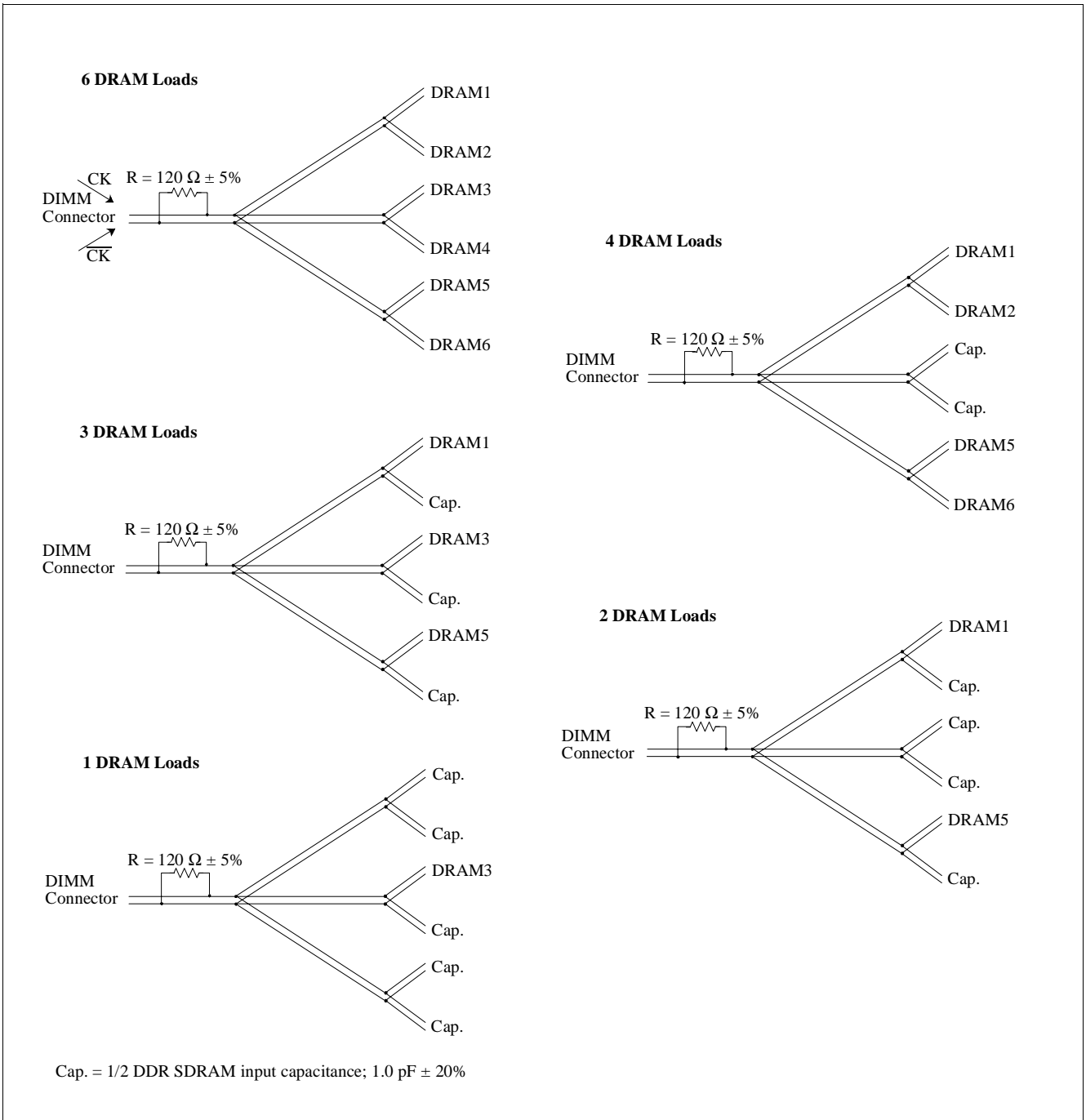


Figure 6 Clock Net Wiring



### 3 Electrical Characteristics

#### 3.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	–	$V_{DDQ} + 0.5$	V	–
Voltage on inputs relative to $V_{SS}$	$V_{IN}$	-1	–	+3.6	V	–
Voltage on $V_{DD}$ supply relative to $V_{SS}$	$V_{DD}$	-1	–	+3.6	V	–
Voltage on $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DDQ}$	-1	–	+3.6	V	–
Operating temperature (ambient)	$T_A$	0	–	+70	°C	–
Storage temperature (plastic)	$T_{STG}$	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	$P_D$	–	1	–	W	–
Short circuit output current	$I_{OUT}$	–	50	–	mA	–

**Attention: Permanent damage to the device may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.**

Table 7 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition <sup>1)</sup>
		Min.	Typ.	Max.		
Device Supply Voltage	$V_{DD}$	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz
Device Supply Voltage	$V_{DD}$	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz <sup>2)</sup>
Output Supply Voltage	$V_{DDQ}$	2.3	2.5	2.7	V	$f_{CK} \leq 166$ MHz <sup>3)</sup>
Output Supply Voltage	$V_{DDQ}$	2.5	2.6	2.7	V	$f_{CK} > 166$ MHz <sup>2)3)</sup>
EEPROM supply voltage	$V_{DDSPD}$	2.3	2.5	3.6	V	–
Supply Voltage, I/O Supply Voltage	$V_{SS}, V_{SSQ}$	0		0	V	–
Input Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	$f_{CK} \leq 166$ MHz <sup>4)</sup>
Input Reference Voltage	$V_{REF}$	$V_{DDQ} / 2 - 50$ mV	$V_{DDQ} / 2$	$V_{DDQ} / 2 + 50$ mV	V	$f_{CK} > 166$ MHz <sup>2)4)</sup>
I/O Termination Voltage (System)	$V_{TT}$	$V_{REF} - 0.04$		$V_{REF} + 0.04$	V	<sup>5)</sup>
Input High (Logic1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$		$V_{DDQ} + 0.3$	V	<sup>8)</sup>
Input Low (Logic0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.15$	V	<sup>8)</sup>
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	-0.3		$V_{DDQ} + 0.3$	V	<sup>8)</sup>
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		$V_{DDQ} + 0.6$	V	<sup>8)6)</sup>

**Table 7 Electrical Characteristics and DC Operating Conditions (cont'd)**

Parameter	Symbol	Values			Unit	Note/Test Condition <sup>1)</sup>
		Min.	Typ.	Max.		
VI-Matching Pull-up Current to Pull-down Current	$V_{I_{Ratio}}$	0.71		1.4	—	<sup>7)</sup>
Input Leakage Current	$I_I$	-2		2	$\mu A$	Any input $0 V \leq V_{IN} \leq V_{DD}$ ; All other pins not under test = 0 V <sup>8)9)</sup>
Output Leakage Current	$I_{OZ}$	-5		5	$\mu A$	DQs are disabled; $0 V \leq V_{OUT} \leq V_{DDQ}$ <sup>8)</sup>
Output High Current, Normal Strength Driver	$I_{OH}$	—		-16.2	mA	$V_{OUT} = 1.95 V$ <sup>8)</sup>
Output Low Current, Normal Strength Driver	$I_{OL}$	16.2		—	mA	$V_{OUT} = 0.35 V$ <sup>8)</sup>

- 1)  $0^\circ C \leq T_A \leq 70^\circ C$
- 2) DDR400 conditions apply for all clock frequencies above 166 MHz
- 3) Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .
- 4) Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF(DC)}$ .  $V_{REF}$  is also expected to track noise variations in  $V_{DDQ}$ .
- 5)  $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$ , and must track variations in the DC level of  $V_{REF}$ .
- 6)  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
- 7) The ration of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
- 8) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 9) Values are shown per DDR SDRAM component

### 3.2 Current Conditions and Specification

**Table 8**  $I_{DD}$  Conditions

Parameter	Symbol
<b>Operating Current 0</b> one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	$I_{DD0}$
<b>Operating Current 1</b> one bank; active/read/precharge; Burst Length = 4; see component data sheet.	$I_{DD1}$
<b>Precharge Power-Down Standby Current</b> all banks idle; power-down mode; $CKE \leq V_{IL,MAX}$	$I_{DD2P}$
<b>Precharge Floating Standby Current</b> $\overline{CS} \geq V_{IH,MIN}$ ; all banks idle; $CKE \geq V_{IH,MIN}$ ; address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD2F}$
<b>Precharge Quiet Standby Current</b> $\overline{CS} \geq V_{IH,MIN}$ ; all banks idle; $CKE \geq V_{IH,MIN}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM; address and other control inputs stable at $\geq V_{IH,MIN}$ or $\leq V_{IL,MAX}$ .	$I_{DD2Q}$
<b>Active Power-Down Standby Current</b> one bank active; power-down mode; $CKE \leq V_{IL,MAX}$ ; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	$I_{DD3P}$
<b>Active Standby Current</b> one bank active; $\overline{CS} \geq V_{IH,MIN}$ ; $CKE \geq V_{IH,MIN}$ ; $t_{RC} = t_{RAS,MAX}$ ; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	$I_{DD3N}$
<b>Operating Current Read</b> one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; $I_{OUT} = 0$ mA	$I_{DD4R}$
<b>Operating Current Write</b> one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	$I_{DD4W}$
<b>Auto-Refresh Current</b> $t_{RC} = t_{RFCMIN}$ ; distributed refresh	$I_{DD5}$
<b>Self-Refresh Current</b> $CKE \leq 0.2$ V; external clock on	$I_{DD6}$
<b>Operating Current 7</b> four bank interleaving with Burst Length = 4; see component data sheet.	$I_{DD7}$

Table 9  $I_{DD}$  Specification (PC2700, -6)

Part Number & Organization	HYS64D16301HU-6-C		HYS64D32000HU-6-C		HYS72D32000HU-6-C		HYS64D64020HU-6-C		HYS72D64020HU-6-C		Unit	Note <sup>1)2)</sup>
	128MB		256MB		256MB		512MB		512MB			
	× 64		× 64		× 72		× 64		× 72			
	1 Rank		1 Rank		1 Rank		2 Ranks		2 Ranks			
	-6		-6		-6		-6		-6			
Symbol	typ.	max.	typ.	max.	typ.	max.	typ.	max.	typ.	max.		
$I_{DD0}$	260	300	480	600	540	675	736	904	828	1017	mA	<sup>3)</sup>
$I_{DD1}$	320	380	560	680	630	765	816	984	918	1107	mA	<sup>3)4)</sup>
$I_{DD2P}$	14	18	28	36	31.5	40.5	56	72	63	81	mA	<sup>5)</sup>
$I_{DD2F}$	100	340	200	240	225	270	400	480	450	540	mA	<sup>5)</sup>
$I_{DD2Q}$	68	96	136	192	153	216	272	384	306	432	mA	<sup>5)</sup>
$I_{DD3P}$	44	60	88	120	99	135	176	240	198	270	mA	<sup>5)</sup>
$I_{DD3N}$	136	160	256	304	288	342	512	608	576	684	mA	<sup>5)</sup>
$I_{DD4R}$	340	400	560	680	630	765	816	984	918	1107	mA	<sup>3)4)</sup>
$I_{DD4W}$	360	440	600	720	675	810	856	1024	963	1152	mA	<sup>3)</sup>
$I_{DD5}$	540	640	1080	1280	1215	1440	1336	1584	1503	1782	mA	<sup>3)</sup>
$I_{DD6}$	5.6	11.2	11.2	22.4	12.6	25.2	44.8	22.4	25.2	25.2	mA	<sup>5)</sup>
$I_{DD7}$	820	960	1440	1720	1620	1935	1696	2024	1908	2277	mA	<sup>3)4)</sup>

- 1) Module  $I_{DD}$  values are calculated on the basis of component  $I_{DD}$  and can be measured differently according to DQ loading capacity.
- 2) Test condition for maximum values:  $V_{DD} = 2.7 \text{ V}$ ,  $T_A = 10 \text{ °C}$
- 3) The module  $I_{DDx}$  values are calculated from the  $I_{DDx}$  values of the component data sheet as follows:  
 $m \times I_{DDx}[\text{component}] + n \times I_{DD3N}[\text{component}]$  with  $m$  and  $n$  number of components of rank 1 and 2;  $n=0$  for 1 rank modules
- 4) DQ I/O ( $I_{DDQ}$ ) currents are not included in the calculations (see note 1)
- 5) The module  $I_{DDx}$  values are calculated from the component  $I_{DDx}$  data sheet values as:  $(m + n) \times I_{DDx}[\text{component}]$

Table 10  $I_{DD}$  Specification (PC3200, -5)

Part Number & Organization	HYS64D16301HU-5-C		HYS64D32000HU-5-C		HYS72D32000HU-5-C		HYS64D64020HU-5-C		HYS72D64020HU-5-C		Unit	Note <sup>1)2)</sup>
	128MB		256MB		256MB		512MB		512MB			
	× 64		× 64		× 72		× 64		× 72			
	1 Rank		1 Rank		1 Rank		2 Ranks		2 Ranks			
	-5		-5		-5		-5		-5			
Symbol	typ.	max.	typ.	max.	typ.	max.	typ.	max.	typ.	max.		
$I_{DD0}$	280	340	560	640	630	720	848	984	954	1107	mA	<sup>3)</sup>
$I_{DD1}$	340	420	640	760	720	855	928	1104	1044	1242	mA	<sup>3)4)</sup>
$I_{DD2P}$	14	18	28	36	31.5	40.5	56	72	63	81	mA	<sup>5)</sup>
$I_{DD2F}$	120	144	240	288	270	324	480	576	540	648	mA	<sup>5)</sup>
$I_{DD2Q}$	76	104	152	208	171	234	304	416	342	468	mA	<sup>5)</sup>
$I_{DD3P}$	48	64	96	128	108	144	192	256	216	288	mA	<sup>5)</sup>
$I_{DD3N}$	152	184	288	344	324	387	576	688	648	774	mA	<sup>5)</sup>
$I_{DD4R}$	400	480	680	800	765	900	968	1144	1089	1287	mA	<sup>3)4)</sup>
$I_{DD4W}$	420	520	720	840	810	945	1008	1184	1134	1332	mA	<sup>3)</sup>
$I_{DD5}$	600	720	1200	1440	1350	1620	1488	1784	1674	2007	mA	<sup>3)</sup>
$I_{DD6}$	6	11.6	12	23.2	13.5	26.1	24	46.4	27	52.2	mA	<sup>5)</sup>
$I_{DD7}$	900	1060	1600	1920	1800	2160	1888	2264	2124	2547	mA	<sup>3)4)</sup>

- 1) Module  $I_{DD}$  values are calculated on the basis of component  $I_{DD}$  and can be measured differently according to DQ loading capacity.
- 2) Test condition for maximum values:  $V_{DD} = 2.7 \text{ V}$ ,  $T_A = 10 \text{ °C}$
- 3) The module  $I_{DDx}$  values are calculated from the  $I_{DDx}$  values of the component data sheet as follows:  
 $m \times I_{DDx}[\text{component}] + n \times I_{DD3N}[\text{component}]$  with  $m$  and  $n$  number of components of rank 1 and 2;  $n=0$  for 1 rank modules
- 4) DQ I/O ( $I_{DDQ}$ ) currents are not included in the calculations (see note 1)
- 5) The module  $I_{DDx}$  values are calculated from the component  $I_{DDx}$  data sheet values as:  $(m + n) \times I_{DDx}[\text{component}]$

### 3.3 AC Characteristics

Table 11 AC Timing - Absolute Specifications –6/–5

Parameter	Symbol	–6		–5		Unit	Note/ Test Condition <sup>1)</sup>
		DDR333		DDR400B			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/ $\overline{\text{CK}}$	$t_{AC}$	–0.7	+0.7	–0.6	+0.6	ns	2)3)4)5)
DQS output access time from CK/ $\overline{\text{CK}}$	$t_{DQSCK}$	–0.6	+0.6	–0.5	+0.5	ns	2)3)4)5)
CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	$t_{CK}$	2)3)4)5)
Clock Half Period	$t_{HP}$	min. ( $t_{CL}$ , $t_{CH}$ )		min. ( $t_{CL}$ , $t_{CH}$ )		ns	2)3)4)5)
Clock cycle time	$t_{CK}$	6	12	5	12	ns	CL = 3.0 <sup>2)3)4)5)</sup>
		6	12	6	12	ns	CL = 2.5 <sup>2)3)4)5)</sup>
		7.5	12	7.5	12	ns	CL = 2.0 <sup>2)3)4)5)</sup>
DQ and DM input hold time	$t_{DH}$	0.45	—	0.4	—	ns	2)3)4)5)
DQ and DM input setup time	$t_{DS}$	0.45	—	0.4	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	$t_{IPW}$	2.2	—	tbd	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	$t_{DIPW}$	1.75	—	tbd	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/ $\overline{\text{CK}}$	$t_{HZ}$	–0.7	+0.7	–0.6	+0.6	ns	2)3)4)5)7)
Data-out low-impedance time from CK/ $\overline{\text{CK}}$	$t_{LZ}$	–0.7	+0.7	–0.6	+0.6	ns	2)3)4)5)7)
Write command to 1 <sup>st</sup> DQS latching transition	$t_{DQSS}$	0.75	1.25	0.75	1.25	$t_{CK}$	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	$t_{DQSQ}$	—	+0.40	—	+0.40	ns	TFBGA <sup>2)3)4)5)</sup>
		—	+0.45	—	+0.40	ns	TSOPII <sup>2)3)4)5)</sup>
Data hold skew factor	$t_{QHS}$	—	+0.50	—	+0.50	ns	TFBGA <sup>2)3)4)5)</sup>
		—	+0.55	—	+0.50	ns	TSOPII <sup>2)3)4)5)</sup>
DQ/DQS output hold time	$t_{QH}$	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	$t_{CK}$	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	0.2	—	$t_{CK}$	2)3)4)5)
Mode register set command cycle time	$t_{MRD}$	2	—	2	—	$t_{CK}$	2)3)4)5)
Write preamble setup time	$t_{WPRES}$	0	—	0	—	ns	2)3)4)5)8)
Write postamble	$t_{WPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)9)
Write preamble	$t_{WPRE}$	0.25	—	0.25	—	$t_{CK}$	2)3)4)5)
Address and control input setup time	$t_{IS}$	0.75	—	0.6	—	ns	fast slew rate 3)4)5)6)10)
		0.8	—	0.7	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	$t_{IH}$	0.75	—	0.6	—	ns	fast slew rate 3)4)5)6)10)
		0.8	—	0.7	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$	2)3)4)5)

Table 11 AC Timing - Absolute Specifications –6/–5 (cont'd)

Parameter	Symbol	–6		–5		Unit	Note/ Test Condition <sup>1)</sup>
		DDR333		DDR400B			
		Min.	Max.	Min.	Max.		
Read postamble	$t_{RPST}$	0.40	0.60	0.40	0.60	$t_{CK}$	2)3)4)5)
Active to Precharge command	$t_{RAS}$	42	70E+3	40	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	$t_{RC}$	60	—	55	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	$t_{RFC}$	72	—	65	—	ns	2)3)4)5)
Active to Read or Write delay	$t_{RCD}$	18	—	15	—	ns	2)3)4)5)
Precharge command period	$t_{RP}$	18	—	15	—	ns	2)3)4)5)
Active to Autoprecharge delay	$t_{RAP}$	18	—	15	—	ns	2)3)4)5)
Active bank A to Active bank B command	$t_{RRD}$	12	—	10	—	ns	2)3)4)5)
Write recovery time	$t_{WR}$	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	$t_{DAL}$					$t_{CK}$	2)3)4)5)11)
Internal write to read command delay	$t_{WTR}$	1	—	1	—	$t_{CK}$	2)3)4)5)
Exit self-refresh to non-read command	$t_{XSNR}$	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	$t_{XSRD}$	200	—	200	—	$t_{CK}$	2)3)4)5)
Average Periodic Refresh Interval	$t_{REFI}$	—	7.8	—	7.8	$\mu$ s	2)3)4)5)12)

- 1)  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{DDQ} = 2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$  (DDR333);  $V_{DDQ} = 2.6\text{V} \pm 0.1\text{V}$ ,  $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$  (DDR400)
- 2) Input slew rate  $\geq 1\text{V/ns}$  for DDR400, DDR333
- 3) The CK/ $\overline{\text{CK}}$  input reference level (for timing reference to CK/ $\overline{\text{CK}}$ ) is the point at which CK and  $\overline{\text{CK}}$  cross: the input reference level for signals other than CK/ $\overline{\text{CK}}$ , is  $V_{REF}$ . CK/ $\overline{\text{CK}}$  slew rate are  $\geq 1.0\text{V/ns}$ .
- 4) Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
- 5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is  $V_{TT}$ .
- 6) These parameters guarantee device timing, but they are not necessarily tested on each device.
- 7)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
- 8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on  $t_{DQSS}$ .
- 9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 10) Fast slew rate  $\geq 1.0\text{V/ns}$ , slow slew rate  $\geq 0.5\text{V/ns}$  and  $< 1\text{V/ns}$  for command/address and CK &  $\overline{\text{CK}}$  slew rate  $> 1.0\text{V/ns}$ , measured between  $V_{OH(ac)}$  and  $V_{OL(ac)}$ .
- 11) For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  is equal to the actual system clock cycle time.
- 12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

## 4 SPD Contents

Table 12 SPD Codes for PC2700 Modules “-6”

Byte#	Description	Part Number & Organization	HYS64D16301HU-6-C	HYS64D32300HU-6-C	HYS72D32300HU-6-C	HYS64D64320HU-6-C	HYS72D64320HU-6-C
			128MB	256MB	256MB	512MB	512MB
			× 64	× 64	× 72	× 64	× 72
			1 Rank	1 Rank	1 Rank	2Ranks	2Ranks
			-6	-6	-6	-6	-6
HEX	HEX	HEX	HEX	HEX			
0	Programmed SPD Bytes in E2PROM	128	80	80	80	80	80
1	Total number of Bytes in E2PROM	256	08	08	08	08	08
2	Memory Type DDR-I = 07h	DDR SDRAM	07	07	07	07	07
3	# of Row Addresses	13	0D	0D	0D	0D	0D
4	# Number of Column Addresses	9/10	09	0A	0A	0A	0A
5	# of DIMM Banks	1/2	01	01	01	02	02
6	Data Width (LSB)	× 64/× 72	40	40	48	40	48
7	Data Width (MSB)	0	00	00	00	00	00
8	Interface Voltage Levels	SSTL_2.5	04	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	6 ns	60	60	60	60	60
10	tAC SDRAM @ CLmax (Byte 18) [ns]	0.75 ns	70	70	70	70	70
11	DIMM Configuration Type (non- / ECC)	non-ECC/ECC	00	00	02	00	02
12	Refresh Rate	Self-Refresh 7.8 μs	82	82	82	82	82
13	Primary SDRAM width	× 16/× 8	10	08	08	08	08
14	Error Checking SDRAM width	na/× 8	00	00	08	00	08
15	tCCD [cycles]	t <sub>CCD</sub> = 1 CLK	01	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM	4	04	04	04	04	04
18	CAS Latency	CAS latency = 2 & 2.5	0C	0C	0C	0C	0C
19	CS Latency	CS latency = 0	01	01	01	01	01
20	WE (Write) Latency	Write latency = 1	02	02	02	02	02
21	DIMM Attributes	unbuffered	20	20	20	20	20



Table 12 SPD Codes for PC2700 Modules “-6” (cont'd)

Byte#	Description	Part Number & Organization	HYS64D16301HU-6-C	HYS64D32300HU-6-C	HYS72D32300HU-6-C	HYS64D64320HU-6-C	HYS72D64320HU-6-C
			128MB	256MB	256MB	512MB	512MB
			×64	×64	×72	×64	×72
			1 Rank	1 Rank	1 Rank	2Ranks	2Ranks
			-6	-6	-6	-6	-6
HEX	HEX	HEX	HEX	HEX			
22	Component Attributes	—	C1	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	7.5 ns	75	75	75	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	0.70 ns	70	70	70	70	70
25	tCK @ CLmax -1 (Byte 18) [ns]	not supported	00	00	00	00	00
26	tAC SDRAM @ CLmax -1 [ns]	not supported	00	00	00	00	00
27	tRPmin (ns)	18 ns	48	48	48	48	48
28	tRRDmin [ns]	12 ns	30	30	30	30	30
29	tRCDmin [ns]	18 ns	48	48	48	48	48
30	tRASmin [ns]	42 ns	2A	2A	2A	2A	2A
31	Module Density per Bank	128 MByte/ 256 MByte	20	40	40	40	40
32	tAS, tCS [ns]	0.75 ns	75	75	75	75	75
33	tAH, TCH [ns]	0.75 ns	75	75	75	75	75
34	tDS [ns]	0.45 ns	45	45	45	45	45
35	tDH [ns]	0.45 ns	45	45	45	45	45
36 to 40	not used	—	00	00	00	00	00
41	tRCmin [ns]	60 ns	3C	3C	3C	3C	3C
42	tRFCmin [ns]	72 ns	48	48	48	48	48
43	tCKmax [ns]	12 ns	30	30	30	30	30
44	tDQSQmax [ns]	0.45 ns	2D	2D	2D	2D	2D
45	tQHSmax [ns]	0.55 ns	55	55	55	55	55
46 to 61	not used	—	00	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00	00
63	Checksum of Byte 0-62 (LSB only)	—	E8	01	13	02	14
64	JEDEC ID Code for Infineon	—	C1	C1	C1	C1	C1
65 to 71	JEDEC ID Code for Infineon	—	00	00	00	00	00

Table 12 SPD Codes for PC2700 Modules “-6” (cont'd)

Byte#	Description	Part Number & Organization	HYS64D16301HU-6-C	HYS64D32300HU-6-C	HYS72D32300HU-6-C	HYS64D64320HU-6-C	HYS72D64320HU-6-C
			128MB	256MB	256MB	512MB	512MB
			×64	×64	×72	×64	×72
			1 Rank	1 Rank	1 Rank	2Ranks	2Ranks
			-6	-6	-6	-6	-6
			HEX	HEX	HEX	HEX	HEX
72	Module Manufacturer Location	—	xx	xx	xx	xx	xx
73	Part Number, Char 1	—	36	36	37	36	37
74	Part Number, Char 2	—	34	34	32	34	32
75	Part Number, Char 3	—	44	44	44	44	44
76	Part Number, Char 4	—	31	33	33	36	36
77	Part Number, Char 5	—	36	32	32	34	34
78	Part Number, Char 6	—	33	33	33	33	33
79	Part Number, Char 7	—	30	30	30	32	32
80	Part Number, Char 8	—	31	30	30	30	30
81	Part Number, Char 9	—	48	48	48	48	48
82	Part Number, Char 10	—	55	55	55	55	55
83	Part Number, Char 11	—	36	36	36	36	36
84	Part Number, Char 12	—	43	43	43	43	43
85	Part Number, Char 13	—	20	20	20	20	20
86	Part Number, Char 14	—	20	20	20	20	20
87	Part Number, Char 15	—	20	20	20	20	20
88	Part Number, Char 16	—	20	20	20	20	20
89	Part Number, Char 17	—	20	20	20	20	20
90	Part Number, Char 18	—	20	20	20	20	20
91	Module Revision Code	—	xx	xx	xx	xx	xx
92	Test Program Revision Code	—	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	—	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	—	xx	xx	xx	xx	xx
95 to 98	Module Serial Number	—	xx	xx	xx	xx	xx
99 to 127	not used	—	00	00	00	00	00

Table 13 SPD Codes for PC3200 Modules “-5”

Byte#	Description	Part Number & Organization	HYS64D16301HU-5-C	HYS64D32300HU-5-C	HYS72D32300HU-5-C	HYS64D64320HU-5-C	HYS72D64320HU-5-C
			128MB × 64 1 Rank -5	256MB × 64 1 Rank -5	256MB × 72 1 Rank -5	512MB × 64 2Ranks -5	512MB × 72 2Ranks -5
Byte#	Description		HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	128	80	80	80	80	80
1	Total number of Bytes in E2PROM	256	08	08	08	08	08
2	Memory Type DDR-I = 07h	DDR SDRAM	07	07	07	07	07
3	# of Row Addresses	13	0D	0D	0D	0D	0D
4	# Number of Column Addresses	9/10	09	0A	0A	0A	0A
5	# of DIMM Banks	1/2	01	01	01	02	02
6	Data Width (LSB)	× 64/× 72	40	40	48	40	48
7	Data Width (MSB)	0	00	00	00	00	00
8	Interface Voltage Levels	SSTL_2.5	04	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	5 ns	50	50	50	50	50
10	tAC SDRAM @ CLmax (Byte 18) [ns]	0.50 ns	50	50	50	50	50
11	DIMM Configuration Type (non- / ECC)	non-ECC/ECC	00	00	02	00	02
12	Refresh Rate	Self-Refresh 7.8 μs	82	82	82	82	82
13	Primary SDRAM width	× 16/ × 8	10	08	08	08	08
14	Error Checking SDRAM width	na/ × 8	00	00	08	00	08
15	tCCD [cycles]	t <sub>CCD</sub> = 1 CLK	01	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E	0E
17	Number of Banks on SDRAM	4	04	04	04	04	04
18	CAS Latency	CAS latency = 2, 2.5, 3	1C	1C	1C	1C	1C
19	CS Latency	CS latency = 0	01	01	01	01	01
20	WE (Write) Latency	Write latency = 1	02	02	02	02	02
21	DIMM Attributes	unbuffered	20	20	20	20	20
22	Component Attributes	—	C1	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	6.0 ns	60	60	60	60	60

Table 13 SPD Codes for PC3200 Modules “-5” (cont'd)

Byte#	Description	Part Number & Organization	HYS64D16301HU-5-C	HYS64D32300HU-5-C	HYS72D32300HU-5-C	HYS64D64320HU-5-C	HYS72D64320HU-5-C
			128MB ×64 1 Rank -5	256MB ×64 1 Rank -5	256MB ×72 1 Rank -5	512MB ×64 2Ranks -5	512MB ×72 2Ranks -5
			HEX	HEX	HEX	HEX	HEX
24	tAC SDRAM @ CLmax -0.5 [ns]	0.50 ns	50	50	50	50	50
25	tCK @ CLmax -1 (Byte 18) [ns]	7.5 ns	75	75	75	75	75
26	tAC SDRAM @ CLmax -1 [ns]	0.50 ns	50	50	50	50	50
27	tRPmin (ns)	15 ns	3C	3C	3C	3C	3C
28	tRRDmin [ns]	10 ns	28	28	28	28	28
29	tRCDmin [ns]	15 ns	3C	3C	3C	3C	3C
30	tRASmin [ns]	40 ns	28	28	28	28	28
31	Module Density per Bank	128 MByte/ 256 MByte	20	40	40	40	40
32	tAS, tCS [ns]	0.60 ns	60	60	60	60	60
33	tAH, TCH [ns]	0.60 ns	60	60	60	60	60
34	tDS [ns]	0.40 ns	40	40	40	40	40
35	tDH [ns]	0.40 ns	40	40	40	40	40
36 to 40	not used	—	00	00	00	00	00
41	tRCmin [ns]	55 ns	37	37	37	37	37
42	tRFCmin [ns]	65 ns	41	41	41	41	41
43	tCKmax [ns]	10 ns	28	28	28	28	28
44	tDQSQmax [ns]	0.40 ns	28	28	28	28	28
45	tQHSmax [ns]	0.50 ns	50	50	50	50	50
46 to 61	not used	—	00	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00	00
63	Checksum of Byte 0-62 (LSB only)	—	E4	FD	0F	FE	10
64	JEDEC ID Code for Infineon	—	C1	C1	C1	C1	C1
65 to 71	JEDEC ID Code for Infineon	—	00	00	00	00	00
72	Module Manufacturer Location	—	xx	xx	xx	xx	xx
73	Part Number, Char 1	—	36	36	37	36	37
74	Part Number, Char 2	—	34	34	32	34	32
75	Part Number, Char 3	—	44	44	44	44	44
76	Part Number, Char 4	—	31	33	33	36	36
77	Part Number, Char 5	—	36	32	32	34	34

Table 13 SPD Codes for PC3200 Modules “-5” (cont'd)

Byte#	Description	Part Number & Organization	HYS64D16301HU-5-C	HYS64D32300HU-5-C	HYS72D32300HU-5-C	HYS64D64320HU-5-C	HYS72D64320HU-5-C
			128MB ×64 1 Rank -5	256MB ×64 1 Rank -5	256MB ×72 1 Rank -5	512MB ×64 2Ranks -5	512MB ×72 2Ranks -5
			HEX	HEX	HEX	HEX	HEX
78	Part Number, Char 6	—	33	33	33	33	33
79	Part Number, Char 7	—	30	30	30	32	32
80	Part Number, Char 8	—	31	30	30	30	30
81	Part Number, Char 9	—	48	48	48	48	48
82	Part Number, Char 10	—	55	55	55	55	55
83	Part Number, Char 11	—	35	35	35	35	35
84	Part Number, Char 12	—	43	43	43	43	43
85	Part Number, Char 13	—	20	20	20	20	20
86	Part Number, Char 14	—	20	20	20	20	20
87	Part Number, Char 15	—	20	20	20	20	20
88	Part Number, Char 16	—	20	20	20	20	20
89	Part Number, Char 17	—	20	20	20	20	20
90	Part Number, Char 18	—	20	20	20	20	20
91	Module Revision Code	—	xx	xx	xx	xx	xx
92	Test Program Revision Code	—	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	—	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	—	xx	xx	xx	xx	xx
95 to 98	Module Serial Number	—	xx	xx	xx	xx	xx
99 to 127	not used	—	0	0	0	0	0

## 5 Package Outlines

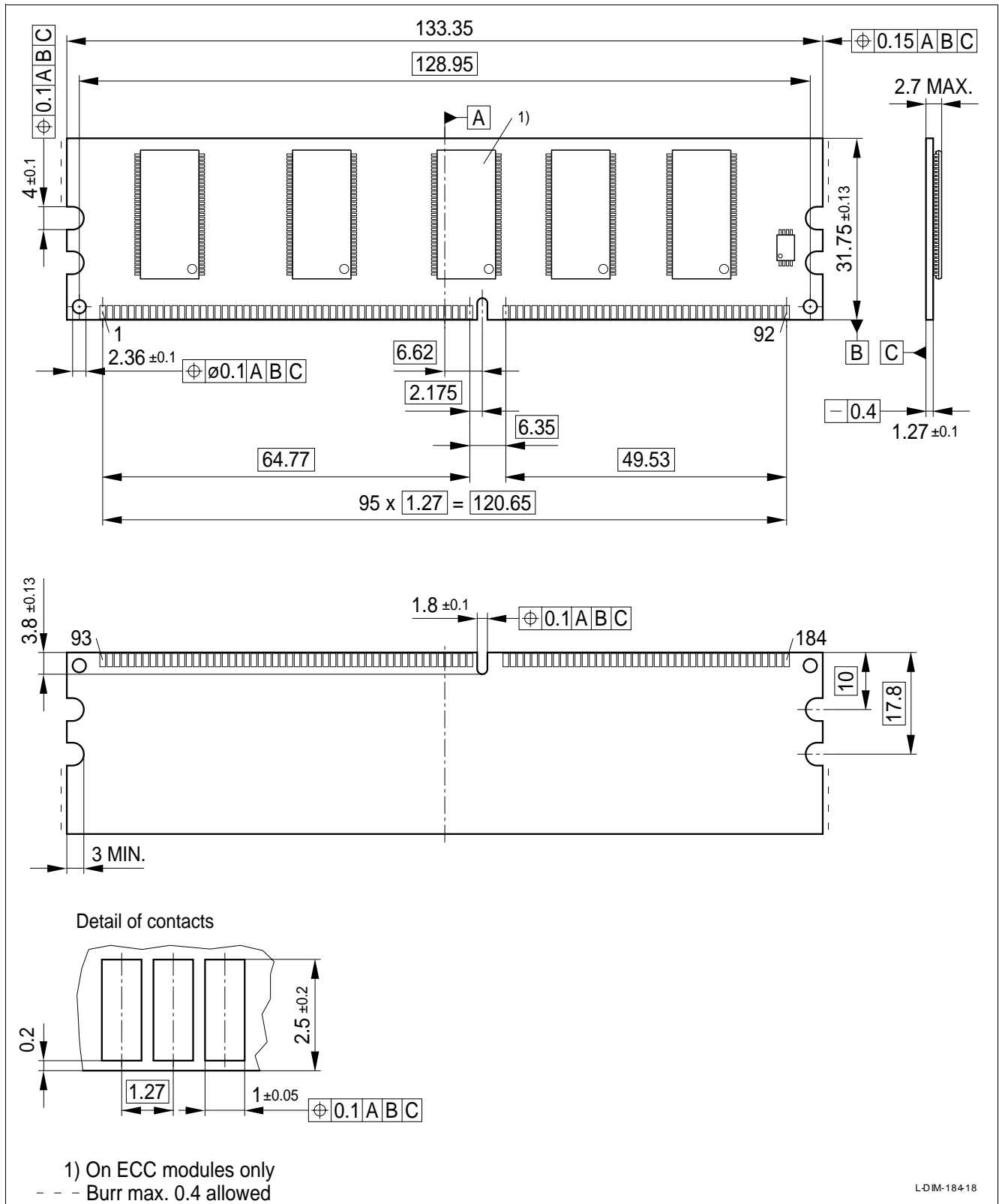


Figure 7 Package Outlines - Raw Card C (128 MByte, 1 Rank Module)

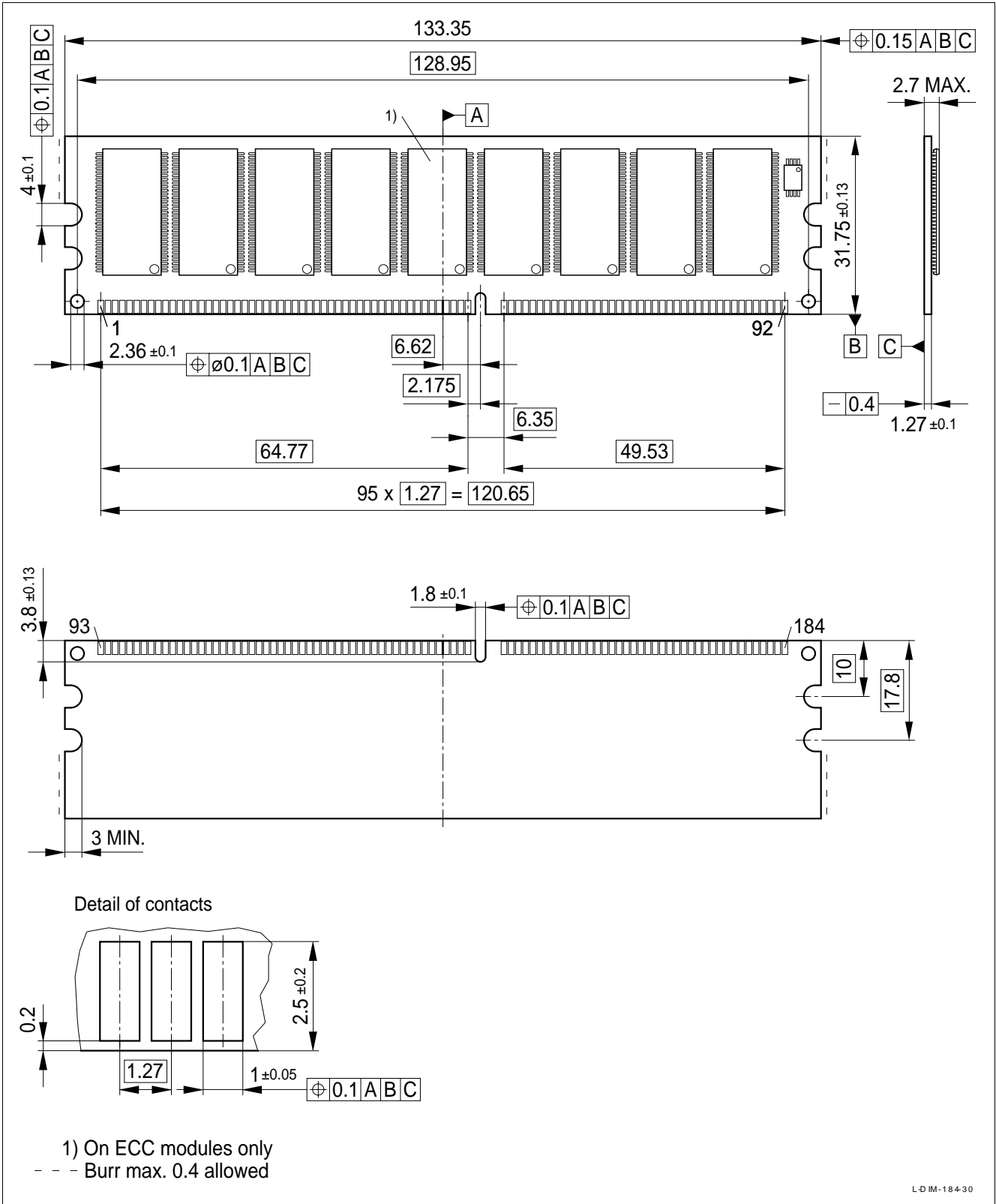


Figure 8 Package Outline - Raw Card A (256 MByte, 1 Rank Module, -5 and -6, ECC)









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