

**75A, 55V, 0.014 Ohm, N-Channel UltraFET Power MOSFETs**



These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology

achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75337.

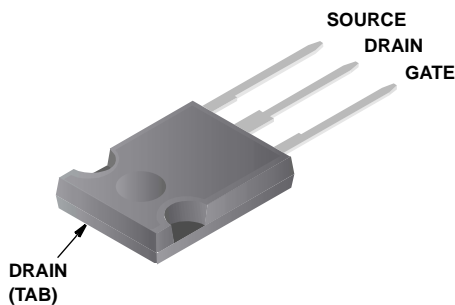
**Ordering Information**

PART NUMBER	PACKAGE	BRAND
HUF75337G3	TO-247	75337G
HUF75337P3	TO-220AB	75337P
HUF75337S3S	TO-263AB	75337S

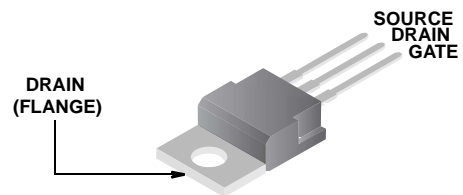
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75337S3ST.

**Packaging**

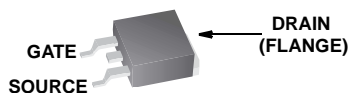
JEDEC STYLE TO-247



JEDEC TO-220AB



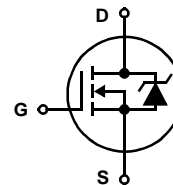
JEDEC TO-263AB



**Features**

- 75A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Models
  - SPICE and SABER Thermal Impedance Models Available on the web at: [www.fairchildsemi.com](http://www.fairchildsemi.com)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>  
For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

# HUF75337G3, HUF75337P3, HUF75337S3S

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	55 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	55 V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$ V
Drain Current		
Continuous (Figure 2) . . . . .	$I_D$	75 A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figure 6
Power Dissipation . . . . .	$P_D$	175 W
Derate Above $25^\circ\text{C}$ . . . . .		1.17 W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 175 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260 $^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>OFF STATE SPECIFICATIONS</b>							
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$	
		$V_{DS} = 45\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA	
<b>ON STATE SPECIFICATIONS</b>							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 75\text{A}, V_{GS} = 10\text{V}$ (Figure 9)	-	0.011	0.014	$\Omega$	
<b>THERMAL SPECIFICATIONS</b>							
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	0.85	$^\circ\text{C}/\text{W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C}/\text{W}$	
		TO-220AB, TO-263AB	-	-	62	$^\circ\text{C}/\text{W}$	
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 10\text{V}</math>)</b>							
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}, I_D \cong 75\text{A}, R_L = 0.4\Omega, V_{GS} = 10\text{V}, R_{GS} = 6.2\Omega$	-	-	100	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	13	-	ns	
Rise Time	$t_r$		-	56	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	31	-	ns	
Fall Time	$t_f$		-	28	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	88	ns	
<b>GATE CHARGE SPECIFICATIONS</b>							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to $20\text{V}$	$V_{DD} = 30\text{V}, I_D \cong 75\text{A}, R_L = 0.4\Omega, I_g(\text{REF}) = 1.0\text{mA}$ (Figure 13)	-	91	109	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0\text{V}$ to $10\text{V}$		-	51	61	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $2\text{V}$		-	3.4	4.1	nC
Gate to Source Gate Charge	$Q_{gs}$			-	9	-	nC
Reverse Transfer Capacitance	$Q_{gd}$			-	23	-	nC

# HUF75337G3, HUF75337P3, HUF75337S3S

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>CAPACITANCE SPECIFICATIONS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$ (Figure 12)	-	1775	-	pF
Output Capacitance	$C_{OSS}$		-	625	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	150	-	pF

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 75\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 75\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	85	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 75\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	180	nC

## Typical Performance Curves

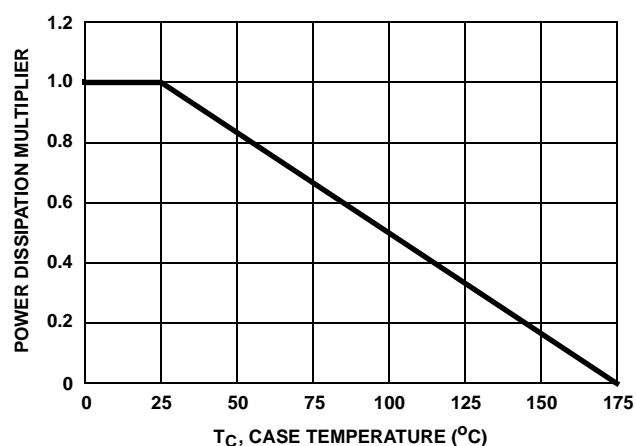


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

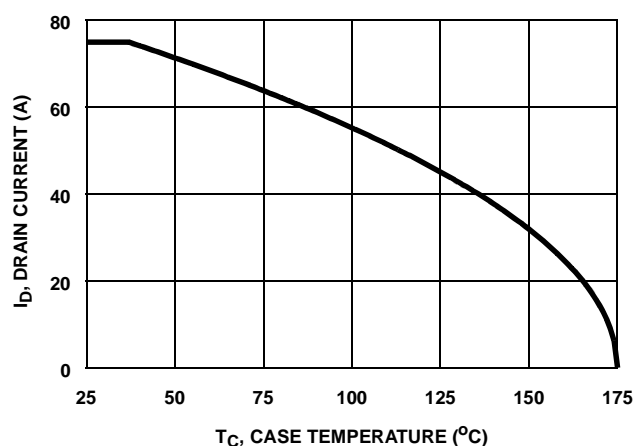


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

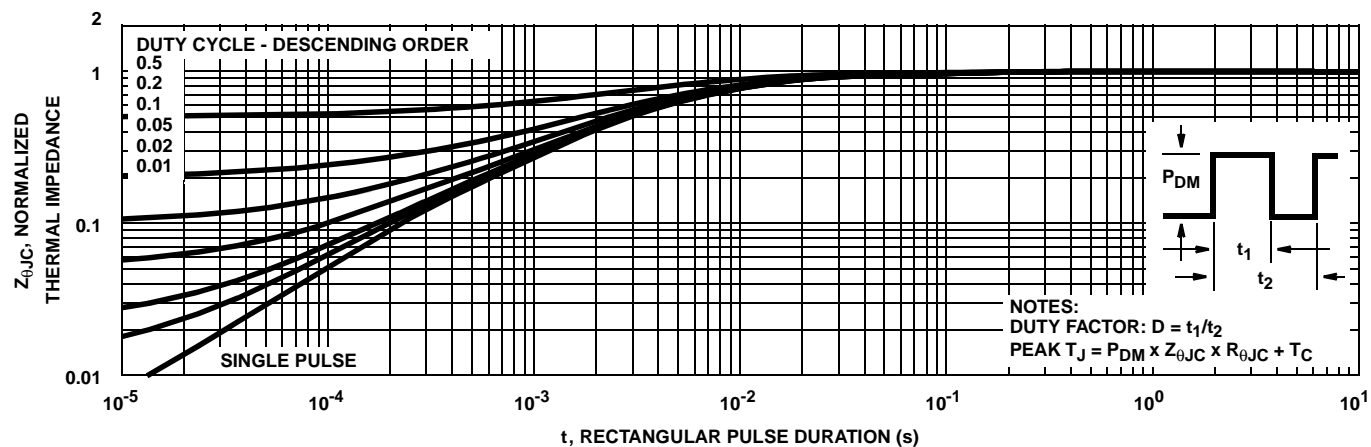


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

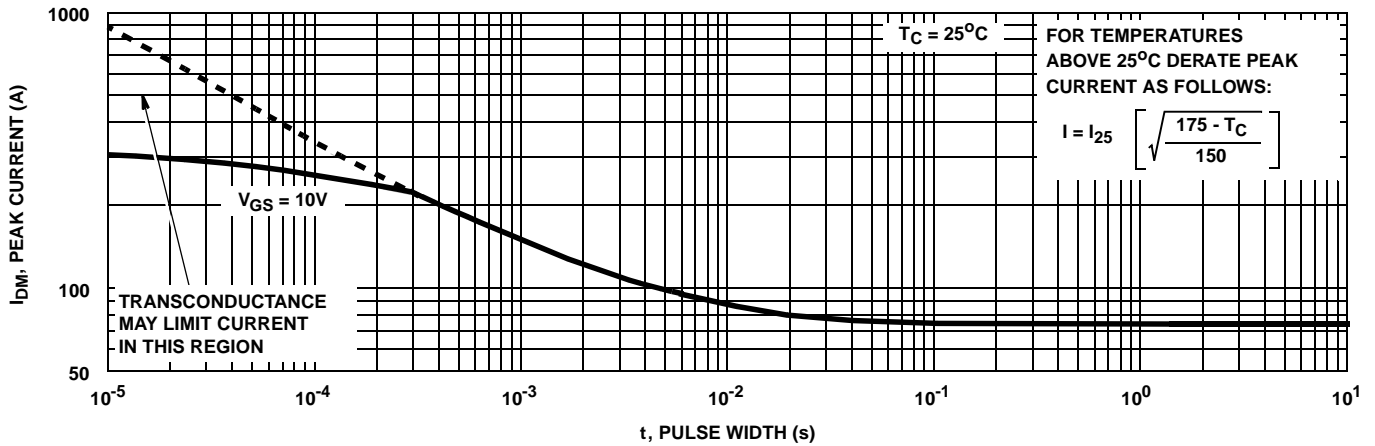


FIGURE 4. PEAK CURRENT CAPABILITY

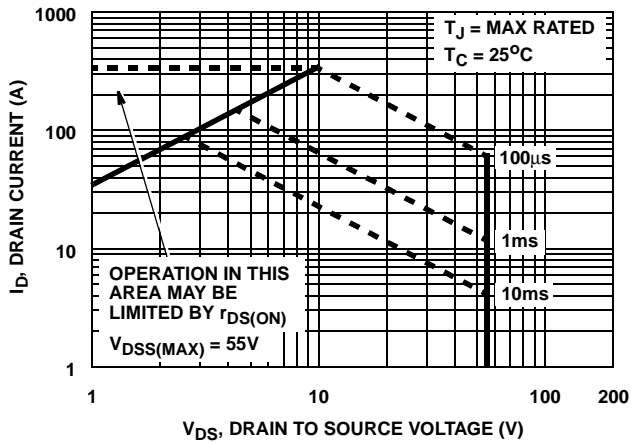
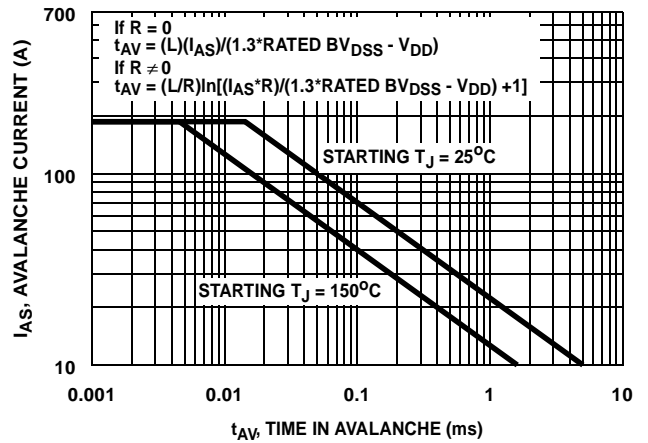


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.  
 FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

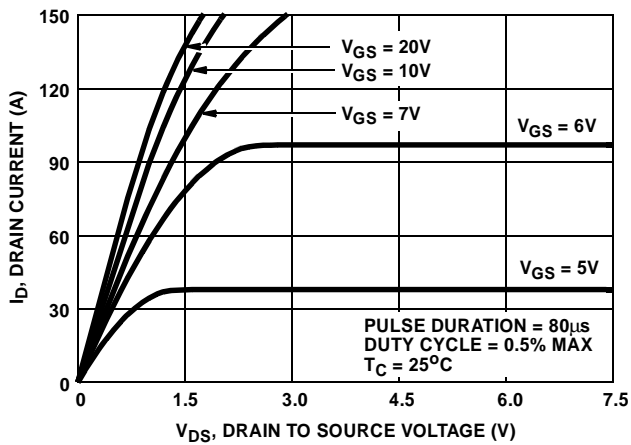


FIGURE 7. SATURATION CHARACTERISTICS

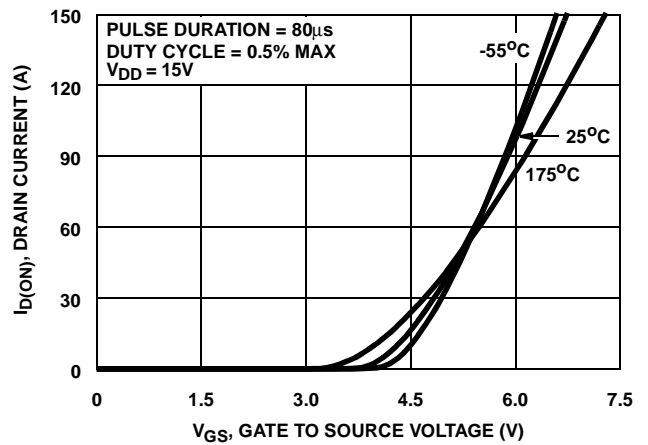


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

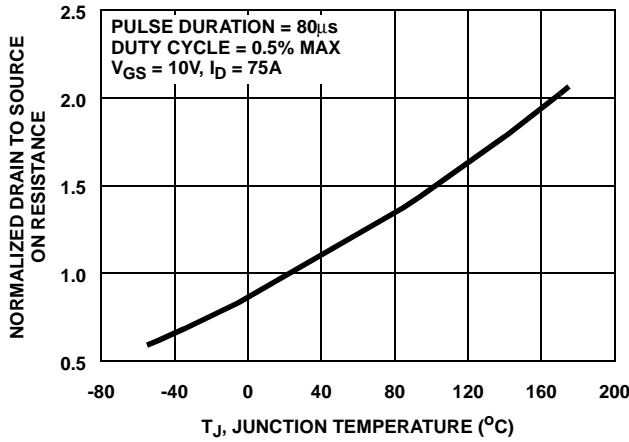


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

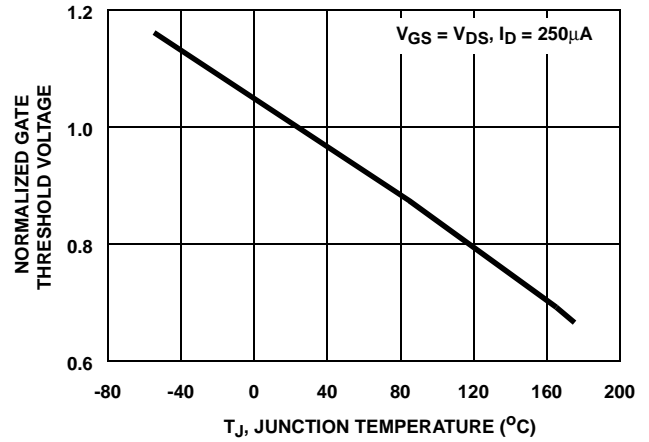


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

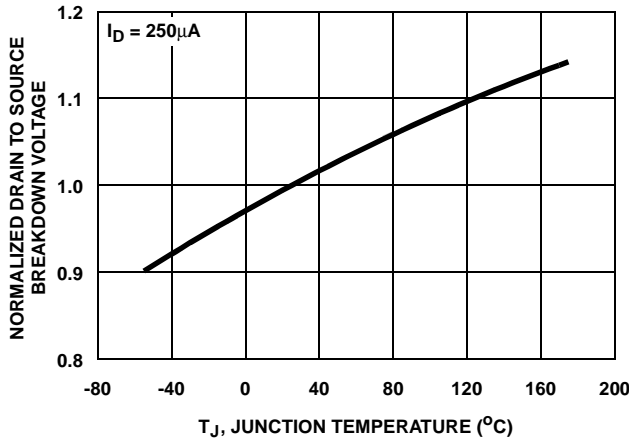


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

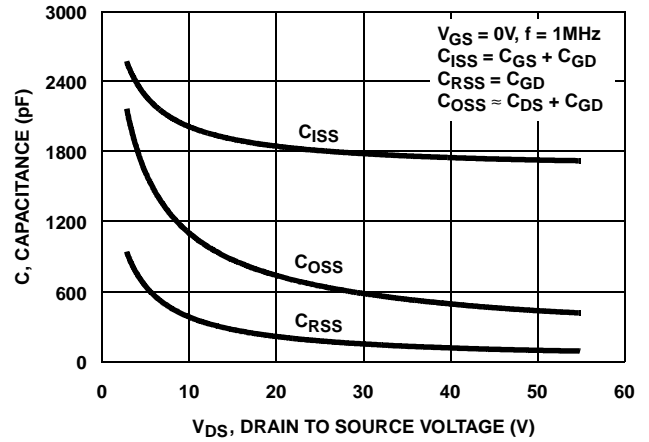
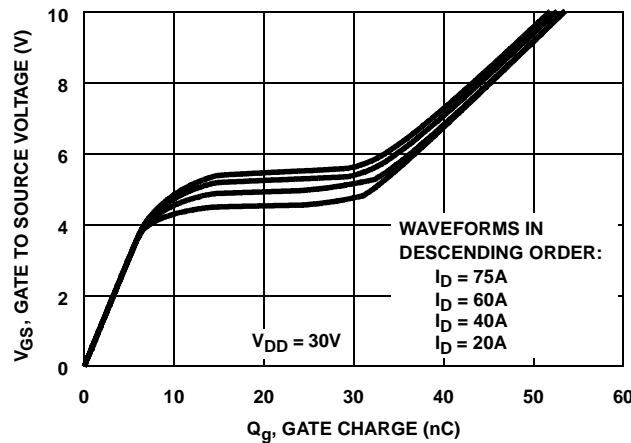


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

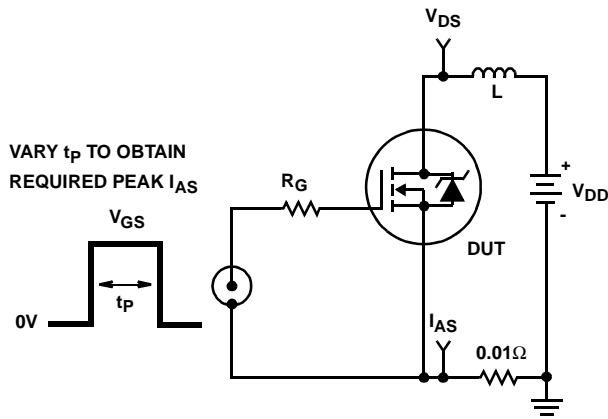


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

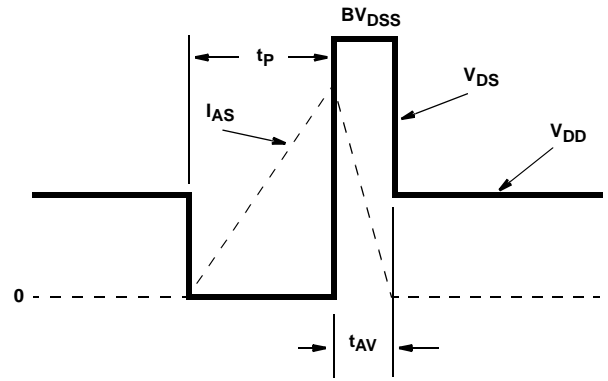


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

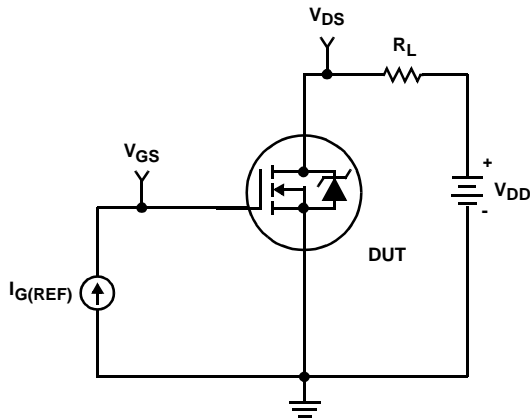


FIGURE 16. GATE CHARGE TEST CIRCUIT

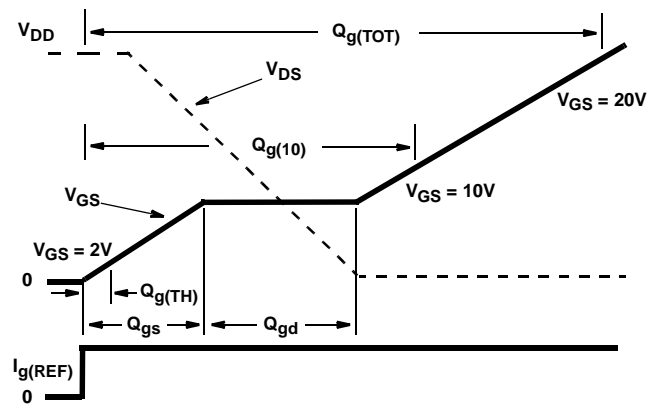


FIGURE 17. GATE CHARGE WAVEFORM

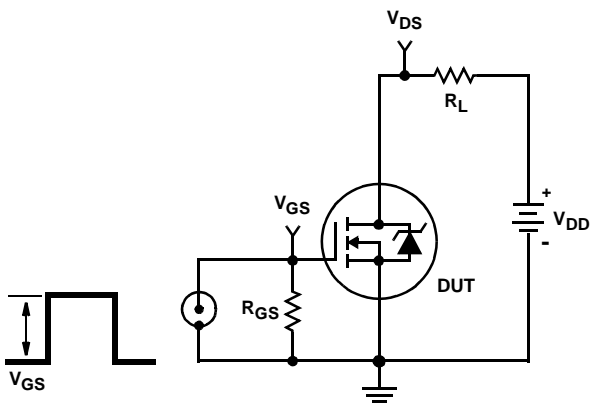


FIGURE 18. SWITCHING TIME TEST CIRCUIT

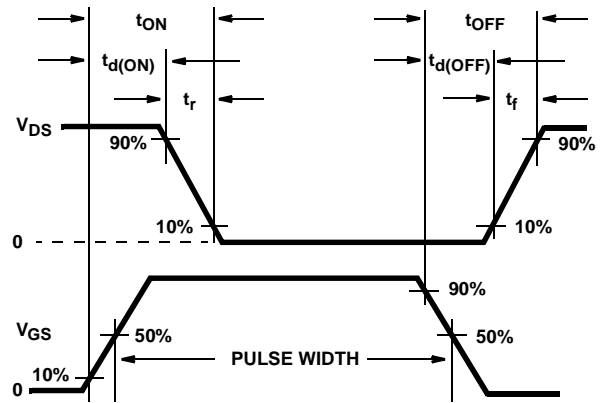


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS







## SPICE Thermal Model

REV February 1999

HUF75337

CTHERM1 th 6 8.0e-7  
 CHERM2 6 5 1.6e-6  
 CHERM3 5 4 4.8e-3  
 CHERM4 4 3 7.6e-3  
 CHERM5 3 2 2.4e-2  
 CHERM6 2 tl 1.5

R THERM1 th 6 1.3e-4  
 R THERM2 6 5 1.8e-3  
 R THERM3 5 4 3.7e-2  
 R THERM4 4 3 2.3e-1  
 R THERM5 3 2 3.4e-1  
 R THERM6 2 tl 6.4e-2

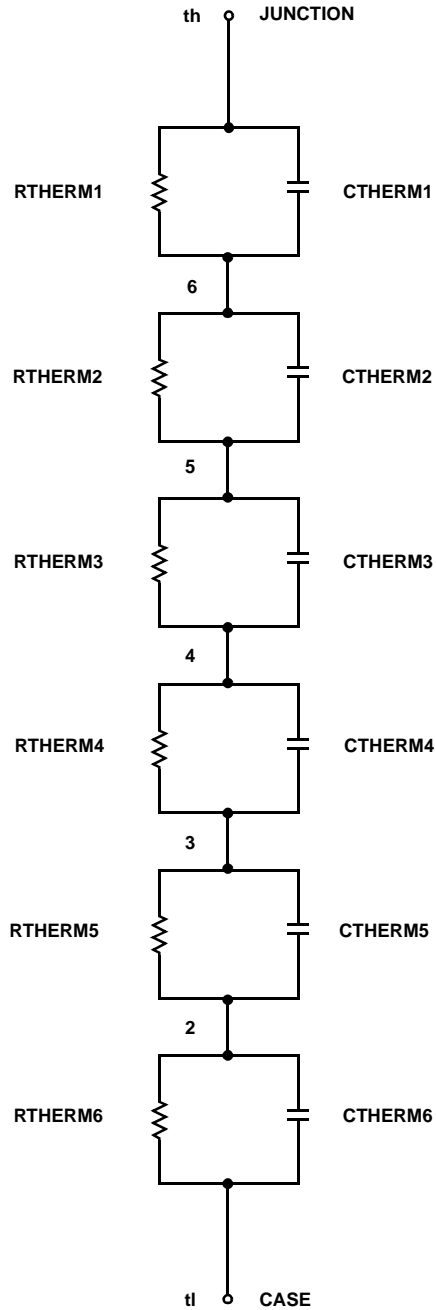
## SABER Thermal Model

SABER thermal model HUF75337

template thermal\_model th tl  
 thermal\_c th, tl

```
{
ctherm.ctherm1 th 6 = 8.0e-7
ctherm.ctherm2 6 5 = 1.6e-6
ctherm.ctherm3 5 4 = 4.8e-3
ctherm.ctherm4 4 3 = 7.6e-3
ctherm.ctherm5 3 2 = 2.4e-2
ctherm.ctherm6 2 tl = 1.5
```

```
rtherm.rtherm1 th 6 = 1.3e-4
rtherm.rtherm2 6 5 = 1.8e-3
rtherm.rtherm3 5 4 = 3.7e-2
rtherm.rtherm4 4 3 = 2.3e-1
rtherm.rtherm5 3 2 = 3.4e-1
rtherm.rtherm6 2 tl = 6.4e-2
}
```



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Bottomless <sup>TM</sup>	FAST <sub>r</sub> <sup>TM</sup>	OPTOPLANAR <sup>TM</sup>	STAR*POWER <sup>TM</sup>	
CoolFET <sup>TM</sup>	FRFET <sup>TM</sup>	PACMAN <sup>TM</sup>	Stealth <sup>TM</sup>	
CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	POPT <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
DenseTrench <sup>TM</sup>	GTO <sup>TM</sup>	Power247 <sup>TM</sup>	SuperSOT <sup>TM</sup> -6	
DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
EcoSPARK <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	QFET <sup>TM</sup>	SyncFET <sup>TM</sup>	
E <sup>2</sup> CMOS <sup>TM</sup>	LittleFET <sup>TM</sup>	QST <sup>TM</sup>	TinyLogic <sup>TM</sup>	
EnSigna <sup>TM</sup>	MicroFET <sup>TM</sup>	QT Optoelectronics <sup>TM</sup>	TruTranslation <sup>TM</sup>	
FACT <sup>TM</sup>	MicroPak <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>	
FACT Quiet Series <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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