HSP45256/883

December 1999

OBSOLETE PRODUCT
FOR A POSSIBLE SUBSTITUTE PRODUCT
call Central Applications 1-888-INTERSIL
or email: centapp@intersil.com

Binary Correlator

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Reconfigurable 256 Stage Binary Correlator**
- **1-Bit Reference x 1, 2, 4, or 8-Bit Data**
- **Separate Control and Reference Interfaces**
- **Configurable for 1-D and 2-D Operation**
- **Double Buffered Mask and Reference**
- **Programmable Output Delay**
- **Cascadable**
- **Standard Microprocessor Interface**

Applications

- **Radar/Sonar**
- **Spread Spectrum Communications**
- **Pattern/Character Recognition**
- **Error Correction Coding**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP45256GM-20/883	-55 to 125	85 Ld CPGA	G85.A
HSP45256GM-25/883	-55 to 125	85 Ld CPGA	G85.A

Description

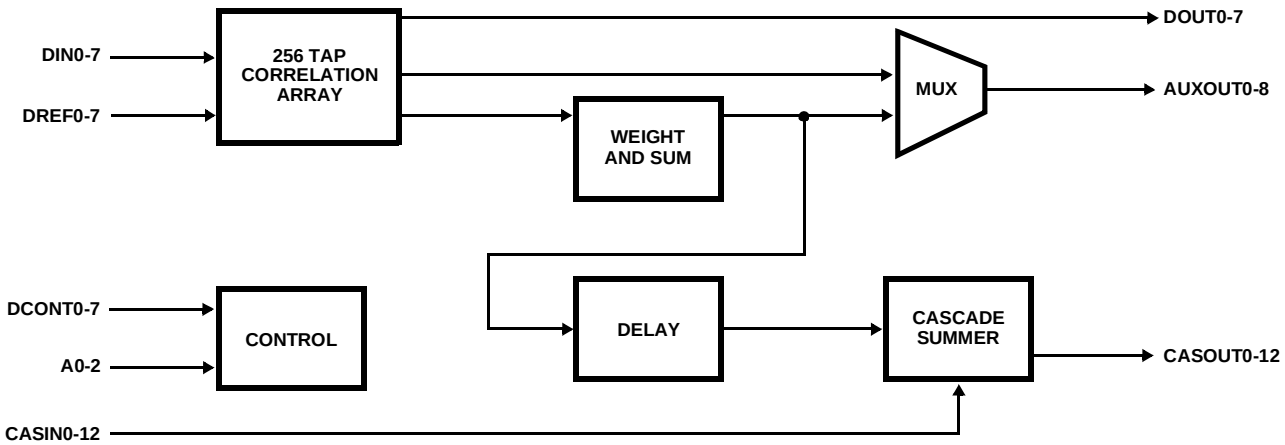
The Intersil HSP45256/883 is a high-speed, 256 tap binary correlator. It can be configured to perform one-dimensional or two-dimensional correlations of selectable data precision and length. Multiple HSP45256's can be cascaded for increased correlation length. Unused taps can be masked out for reduced correlation length.

The correlation array consists of eight 32-tap stages. These may be cascaded internally to compare 1, 2, 4 or 8-bit input data with a 1-bit reference. Depending on the number of bits in the input data, the length of the correlation can be up to 256, 128, 64, or 32 taps. The HSP45256 can also be configured as two separate correlators with window sizes from 4 by 32 to 1 by 128 each. The Mask Register can be used to prevent any subset of the 256 bits from contributing to the correlation score.

The9- output of the correlation array (correlation score) feeds the weight and sum logic, which gives added flexibility to the data format. In addition, an offset register is provided so that a preprogrammed value can be added to the correlation score. This result is then passed through a user programmable delay stage to the cascade summer. The delay stage simplifies the cascading of multiple correlators by compensating for the latency of previous correlators.

The Binary Correlator is configured by writing a set of control registers via a standard microprocessor interface. To simplify operation, both the Control and Reference Registers are double buffered. This allows the user to load new mask and reference data while the current correlation is in progress.

Block Diagram

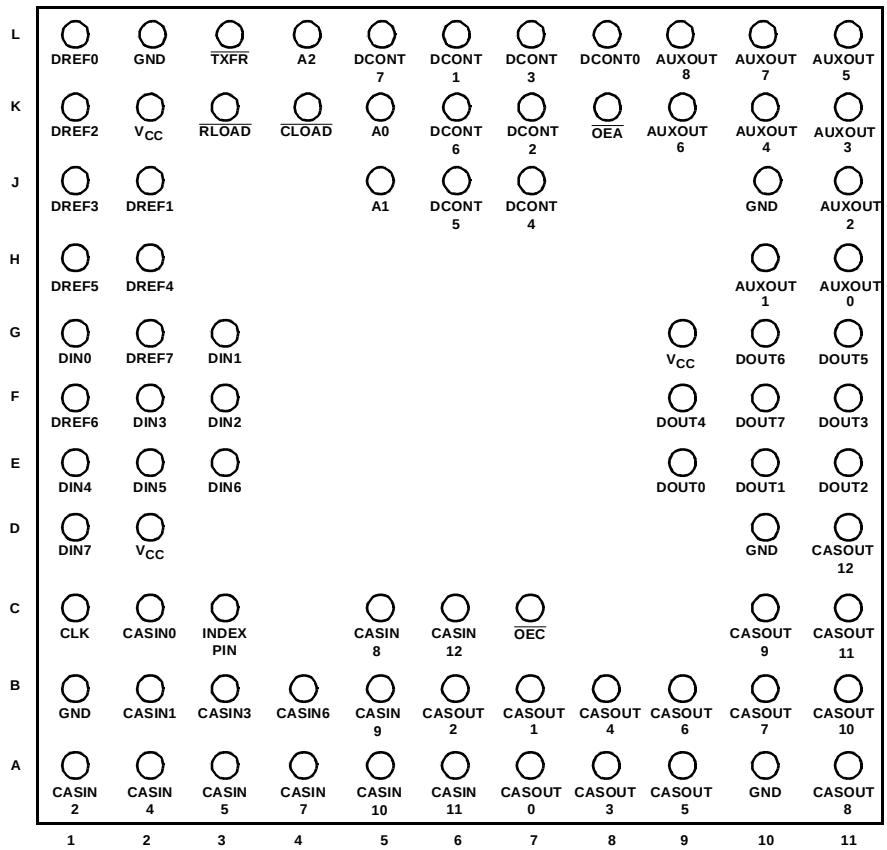


Pinouts

85 PIN PGA
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	CASIN 2	CASIN 4	CASIN 5	CASIN 7	CASIN 10	CASIN 11	CASOUT 0	CASOUT 3	CASOUT 5	GND	CASOUT 8
B	GND	CASIN 1	CASIN 3	CASIN 6	CASIN 9	CASOUT 2	CASOUT 1	CASOUT 4	CASOUT 6	CASOUT 7	CASOUT 10
C	CLK	CASIN 0	INDEX PIN		CASIN 8	CASIN 12	$\overline{OEC}$			CASOUT 9	CASOUT 11
D	DIN7	V_{CC}								GND	CASOUT 12
E	DIN4	DIN5	DIN6						DOUT0	DOUT1	DOUT2
F	DREF 6	DIN3	DIN2						DOUT 4	DOUT 7	DOUT 3
G	DIN0	DREF 7	DIN1						V_{CC}	DOUT 6	DOUT 5
H	DREF 5	DREF 4								AUXOUT 1	AUXOUT 0
J	DREF 3	DREF 1			A1	DCONT 5	DCONT 4			GND	AUXOUT 2
K	DREF 2	V_{CC}	$\overline{RLOAD}$	$\overline{CLOAD}$	A0	DCONT 6	DCONT 2	$\overline{OEA}$	AUXOUT 6	AUXOUT 4	AUXOUT 3
L	DREF 0	GND	$\overline{TXFR}$	A2	DCONT 7	DCONT 1	DCONT 3	DCONT 0	AUXOUT 8	AUXOUT 7	AUXOUT 5

85 PIN PGA
BOTTOM VIEW



Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	D2, G9, K2		The +5V power supply pin.
GND	A10, B1, D10, J10, L2		Ground.
DIN0-7	D1, E1-E3, F2, F3, G1, G3	I	The DIN0-7 bus consists of eight single data input pins. The assignment of the active pins is determined by the configuration. Data is loaded synchronous to the rising edge of CLK. DIN0 is the LSB.
DOUT0-7	E9-E11, F9-F11, G10, G11	O	The DOUT0-7 bus is the data output of the correlation array. The format of the output is dependent on the window configuration and bit weighting. DOUT0 is the LSB.
CLK	C1	I	System Clock. Positive edge triggered.
CASIN0-12	A1-A6, B2-B5, C2, C5, C6	I	CASIN0-12 allows multiple correlators to be cascaded by connecting CASOUT0-12 of one correlator to CASIN0-12 of another. The CASIN bus is added internally to the correlation score to form CASOUT. CASIN0 is the LSB.
CASOUT0-12	A7-A9, A11, B6-B11, C10, C11, D11	O	CASOUT0-12 is the output correlation score. This value is the delayed sum of all the 256 taps of one chip and CASIN0-12. When the part is configured to act as two independent correlators, CASOUT0-8 represents the correlation score for the first correlator while the second correlation score is available on the AUXOUT0-8 bus. In this configuration, the cascading feature is no longer an option. CASOUT0 is the LSB.
$\overline{OEC}$	C7	I	$\overline{OEC}$ is the output enable for CASOUT0-12. When $\overline{OEC}$ is high, the output is three-stated. Processing is not interrupted by this pin (active low).
$\overline{TXFR}$	L3	I	$\overline{TXFR}$ is a synchronous clock enable signal that allows the loading of the reference and mask inputs from the preload register to the correlation array. Data is transferred on the rising edge of CLK while $\overline{TXFR}$ is low (active low).
DREF0-7	F1, G2, H1, H2, J1, J2, K1, L1	I	DREF0-7 is an 8-bit wide data reference input. This is the input data bus used to load the reference data. $\overline{RLOAD}$ going active initiates the loading of the reference registers. This input bus is used to load the reference registers of the correlation array. The manner in which the reference data is loaded is determined by the window configuration. If the window configuration is 1 x 256, the reference bits are loaded one at a time over DREF7. When the HSP45256 is configured as an 8 x 32 array, the data is loaded into all stages in parallel. In this case, DREF7 is the reference data for the first stage and DREF0 is the reference data for the eighth stage. The contents of the reference data registers are not affected by changing the window configuration. DREF0 is the LSB.
$\overline{RLOAD}$	K3	I	$\overline{RLOAD}$ enables loading of the reference registers. Data on DREF0-7 is loaded into the preload registers on the rising edge of $\overline{RLOAD}$. This data is transferred into the correlation array by $\overline{TXFR}$ (active low).
DCONT0-7	J6, J7, K6, K7, L5-L8	I	DCONT0-7 is the control data input, which is used to load the mask bit for each tap as well as the configuration registers. The mask data is sequentially loaded into the eight stages in the same manner as the reference data. DCONT0 is the LSB.
CLOAD#	K4	I	$\overline{CLOAD}$ enables the loading of the data on DCONT0-7. The destination of this data is controlled by A0-2 (active low).
A0-2	J5, K5, L4	I	A0-2 is a 3-bit address that determines what function will be performed when $\overline{CLOAD}$ is active. This address bus is set up with respect to the rising edge of the load signal, $\overline{CLOAD}$. A0 is the LSB.
AUXOUT0-8	H10, H11, J11, K9-K11, L9-L11	O	AUXOUT0-8 is a 9-bit bus that provides either the data reference output or the 9-bit correlation score of the second correlator, depending on the configuration. When the user programs the chip to be two separate correlators, the score of the second correlator is output on this bus. When the user has programmed the chip to be one correlator, AUXOUT0-7 represents the reference data out, with the state of AUXOUT0-8 undefined. AUXOUT0 is the LSB.
$\overline{OEA}$	K8	I	The $\overline{OEA}$ signal is the output enable for the AUXOUT0-8 output. When $\overline{OEA}$ is high, the output is disabled. Processing is not interrupted by this pin (active low).
Index Pin	C3		Used for orienting pin in socket or printed circuit board. Must be left as a no connect in circuit.

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC
Voltage Range (Typical) . . . . . +4.5V to +5.5V

Reliability Information

Thermal Resistance (Typical, Note 1). . . θ_{JA} θ_{JC}
PGA Package . . . . . $36^oC/W$ $10^oC/W$
Maximum Package Power Dissipation at 125^oC
PGA Package 1.39W
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature. . . . . 175^oC
Maximum Lead Temperature (Soldering 10s). . . . . 300^oC
Gate Count . . . . . 13,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (^oC)	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	0.8	V
Logical One Input Voltage Clock	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	3.0	-	V
Logical Zero Input Voltage Clock	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC} = 4.5V (Note 2)	1, 2, 3	$-55 \le T_A \le 125$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC} = 4.5V (Note 2)	1, 2, 3	$-55 \le T_A \le 125$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5V, Outputs Open	1, 2, 3	$-55 \le T_A \le 125$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 20 MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.5V (Note 3)	1, 2, 3	$-55 \le T_A \le 125$	-	140	mA
Functional Test	FT	(Note 4)	7, 8	$-55 \le T_A \le 125$	-	-	-

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating Supply Current is proportional to frequency, typical rating is 7mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} (clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, $V_{OH} \ge 1.5V$, and $V_{OL} \le 1.5V$.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested (Note 5)

PARAMETER	SYMBOL	(NOTE 5) NOTES	GROUP A SUB-GROUPS	TEMPERATURE (^oC)	-25 (25.6MHz)		-20 (20MHz)		UNITS
					MIN	MAX	MIN	MAX	
CLK Period	t_{CP}		9, 10, 11	$-55 \le T_A \le 125$	39	-	50	-	ns
CLK High	t_{CH}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
CLK Low	t_{CL}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
$\overline{\text{CLOAD}}$ Cycle Time	t_{CLC}		9, 10, 11	$-55 \le T_A \le 125$	39	-	50	-	ns
$\overline{\text{CLOAD}}$ High	t_{CLH}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
$\overline{\text{CLOAD}}$ Low	t_{CLL}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
$\overline{\text{RLOAD}}$ Cycle Time	t_{RLC}		9, 10, 11	$-55 \le T_A \le 125$	39	-	50	-	ns
$\overline{\text{RLOAD}}$ High	t_{RLH}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
$\overline{\text{RLOAD}}$ Low	t_{RLL}		9, 10, 11	$-55 \le T_A \le 125$	15	-	20	-	ns
Set-up Time; DIN to CLK High	t_{DS}		9, 10, 11	$-55 \le T_A \le 125$	13	-	15	-	ns
Hold Time; DIN to CLK High	t_{DH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	1	-	ns
Set-up Time; DREF to RLOAD High	t_{RS}		9, 10, 11	$-55 \le T_A \le 125$	14	-	15	-	ns
Hold Time; DREF to RLOAD High	t_{RH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	1	-	ns
DCONT Set up Time	t_{DCS}		9, 10, 11	$-55 \le T_A \le 125$	13	-	15	-	ns
DCONT Hold Time	t_{DCH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	1	-	ns
Address Set up Time	t_{AS}		9, 10, 11	$-55 \le T_A \le 125$	13	-	15	-	ns
Address Hold Time	t_{AH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	1	-	ns
$\overline{\text{TXFR}}$ Set up Time	t_{TS}		9, 10, 11	$-55 \le T_A \le 125$	13	-	15	-	ns
$\overline{\text{TXFR}}$ Hold Time	t_{TH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	1	-	ns
CLK to Output Delay DOUT, AUXOUT, CASOUT	t_{DO}		9, 10, 11	$-55 \le T_A \le 125$	-	20	-	25	ns
Output Enable Time	t_{OE}	Note 6	9, 10, 11	$-55 \le T_A \le 125$	-	20	-	20	ns
$\overline{\text{TXFR}}$ High to CLK Low	t_{THCL}	Note 7	9, 10, 11	$-55 \le T_A \le 125$	3	-	4	-	ns
CLK Low to $\overline{\text{RLOAD}}$, $\overline{\text{CLOAD}}$ High	t_{CLLH}	Note 7	9, 10, 11	$-55 \le T_A \le 125$	1	-	1	-	ns

NOTES:

5. AC testing is performed as follows: V_{CC} = 4.5V and 5.5V. Input levels (CLK input) 4.0V and 0V; input levels (all other inputs) 3.0V and 0V; Timing reference levels (CLK) 2.0V; all others 1.5V. Output load per test load circuit with C_L = 40pF. Output transition is measured at $V_{OH} \ge 1.5V$ and $V_{OL} \le 1.5V$.
6. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, C_L = 40pF.
7. Applicable only when $\overline{\text{TXFR}}$ and $\overline{\text{RLOAD}}$ or $\overline{\text{CLOAD}}$ are active on the same cycle of CLK.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE (^oC)	-25		-20		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz All measurements are referenced to device GND.	8	$-55 \le T_A \le 125$	-	10	-	10	pF
Output Capacitance	C_{OUT}		8	$-55 \le T_A \le 125$	-	10	-	10	pF
Output Disable Time	t_{OD}		8, 9	$-55 \le T_A \le 125$	-	20	-	20	ns
Output Rise Time	t_R	From 0.8V to 2.0V	8, 9	$-55 \le T_A \le 125$	-	8	-	8	ns
Output Fall Time	t_F	From 2.0V to 0.8V	8, 9	$-55 \le T_A \le 125$	-	8	-	8	ns

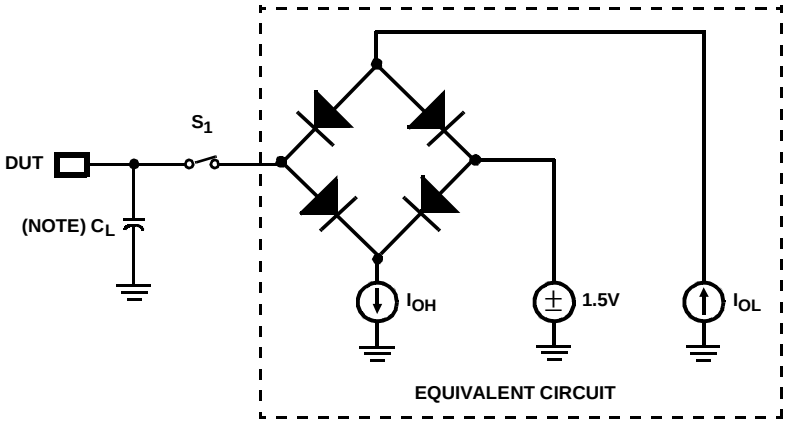
NOTES:

8. The parameters in Table 3 are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
9. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Test Load Circuit



SWITCH S_1 OPEN FOR I_{CCSB} AND I_{CCOP} TEST

NOTE: Includes stray and jig capacitance.

Timing Waveforms

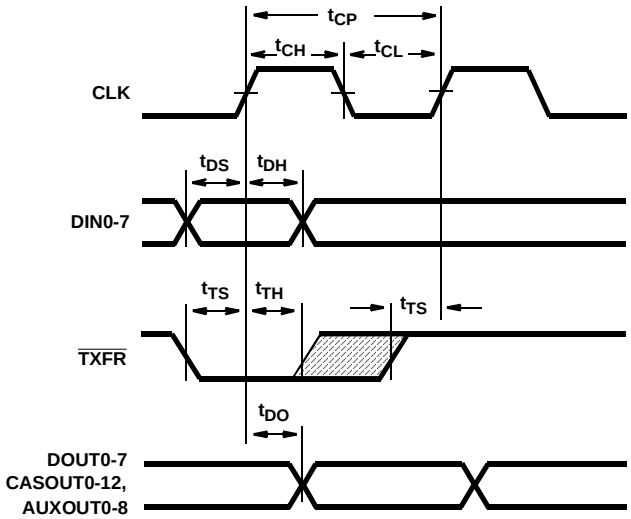


FIGURE 1. INPUT, OUTPUT TIMING

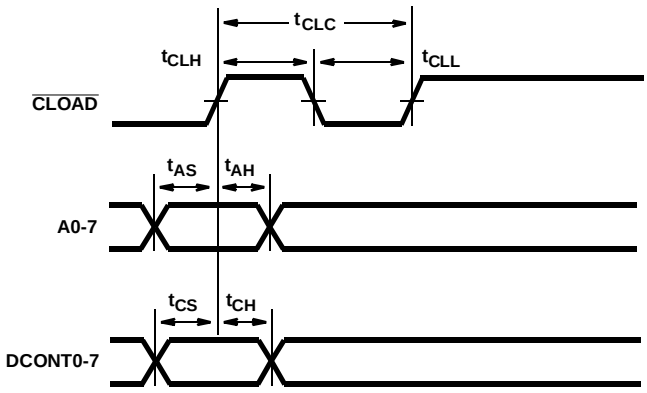


FIGURE 2.

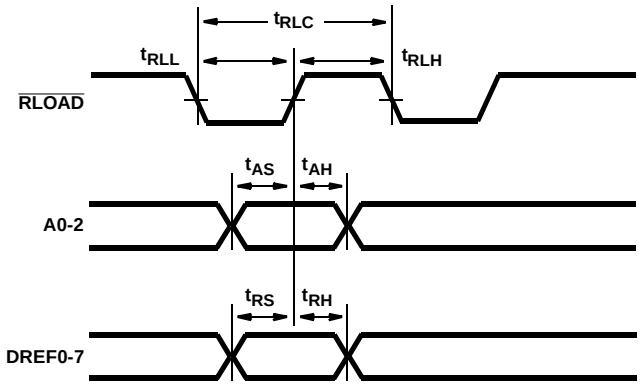


FIGURE 3.

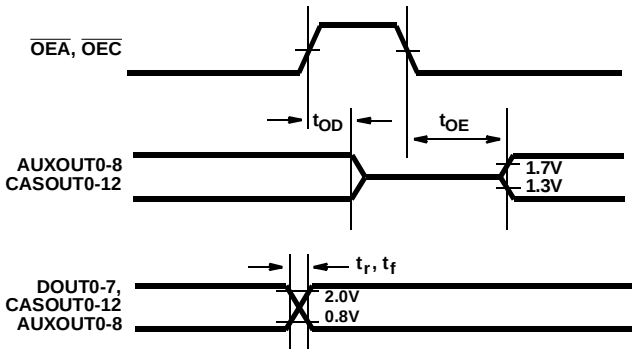


FIGURE 4.

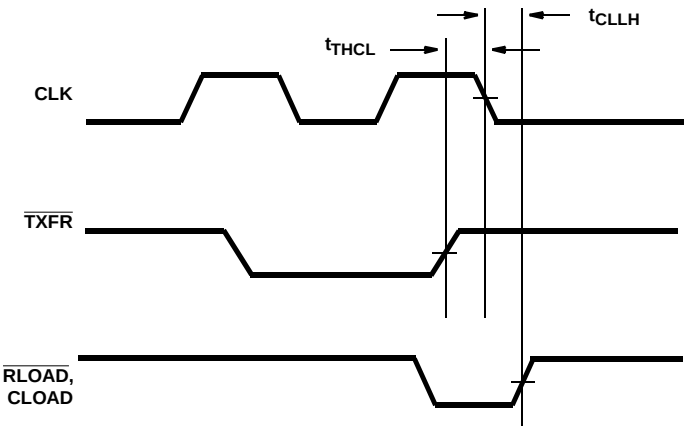


FIGURE 5. TRANSFER, LOAD TIMING WHEN BOTH OCCUR ON A SINGLE CYCLE

Burn-In Circuits

85 PIN PGA
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	CASIN 2	CASIN 4	CASIN 5	CASIN 7	CASIN 10	CASIN 11	CAS OUT 0	CAS OUT 3	CAS OUT 5	GND	CAS OUT 8
B	GND	CASIN 1	CASIN 3	CASIN 6	CASIN 9	CAS OUT 2	CAS OUT 1	CAS OUT 4	CAS OUT 6	CAS OUT 7	CAS OUT 10
C	CLK	CASIN 0	INDEX PIN		CASIN 8	CASIN 12	$\overline{OEC}$			CAS OUT 9	CAS OUT 11
D	DIN7	V_{CC}								GND	CAS OUT 12
E	DIN4	DIN5	DIN6						DOUT0	DOUT1	DOUT2
F	DREF 4	DIN3	DIN2						DOUT 4	DOUT 7	DOUT 3
G	DIN0	DREF 7	DIN1						V_{CC}	DOUT 6	DOUT 5
H	DREF 5	DREF 4								AUX OUT 1	AUX OUT 0
J	DREF 3	DREF 1			A1	DCONT 5	DCONT 4			GND	AUX OUT 2
K	DREF 2	V_{CC}	$\overline{R_{LOAD}}$	$\overline{C_{LOAD}}$	A0	DCONT 6	DCONT 2	$\overline{OEA}$	AUX OUT 6	AUX OUT 4	AUX OUT 3
L	DREF 0	GND	$\overline{TXFR}$	A2	DCONT 7	DCONT 1	DCONT 3	DCONT 0	AUX OUT 8	AUX OUT 7	AUX OUT 5

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	CASIN2	F3	B11	CASOUT10	$V_{CC}/2$	F9	DOUT4	$V_{CC}/2$	K2	V_{CC}	V_{CC}
A2	CASIN4	F5	C1	CLK	F0	F10	DOUT7	$V_{CC}/2$	K3	$\overline{RLOAD}$	F3
A3	CASIN5	F6	C2	CASIN0	F1	F11	DOUT3	$V_{CC}/2$	K4	$\overline{CLOAD}$	F3
A4	CASIN7	F1	C5	CASIN8	F2	G1	DIN0	F1	K5	A0	F9
A5	CASIN10	F4	C6	CASIN12	F6	G2	DREF7	F8	K6	DCONT6	F7
A6	CASIN11	F5	C7	$\overline{OEC}$	F11	G3	DIN1	F2	K7	DCONT2	F6
A7	CASOUT0	$V_{CC}/2$	C10	CASOUT9	$V_{CC}/2$	G9	V_{CC}	V_{CC}	K8	$\overline{OEA}$	F11
A8	CASOUT3	$V_{CC}/2$	C11	CASOUT11	$V_{CC}/2$	G10	DOUT6	$V_{CC}/2$	K9	AUXOUT6	$V_{CC}/2$
A9	CASOUT5	$V_{CC}/2$	D1	DIN7	F8	G11	DOUT5	$V_{CC}/2$	K10	AUXOUT4	$V_{CC}/2$
A10	GND	GND	D2	V_{CC}	V_{CC}	H1	DREF5	F6	K11	AUXOUT3	$V_{CC}/2$
A11	CASOUT8	$V_{CC}/2$	D10	GND	GND	H2	DREF4	F8	L1	DREF0	F4
B1	GND	GND	D11	CASOUT12	$V_{CC}/2$	H10	AUXOUT1	$V_{CC}/2$	L2	GND	GND
B2	CASIN1	F2	E1	DIN4	F5	H11	AUXOUT0	$V_{CC}/2$	L3	$\overline{TXFR}$	F2

(Continued)

PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL	PGA PIN	PIN NAME	BURN-IN SIGNAL
B3	CASIN3	F4	E2	DIN5	F6	J1	DREF3	F7	L4	A2	F11
B4	CASIN6	F7	E3	DIN6	F7	J2	DREF1	F5	L5	DCONT7	F8
B5	CASIN9	F3	E9	DOUT0	$V_{CC}/2$	J5	A1	F10	L6	DCONT1	F5
B6	CASOUT2	$V_{CC}/2$	E10	DOUT1	$V_{CC}/2$	J6	DCONT5	F6	L7	DCONT3	F7
B7	CASOUT1	$V_{CC}/2$	E11	DOUT2	$V_{CC}/2$	J7	DCONT4	F8	L8	DCONT0	F4
B8	CASOUT4	$V_{CC}/2$	F1	DREF6	F7	J10	GND	GND	L9	AUXOUT8	$V_{CC}/2$
B9	CASOUT6	$V_{CC}/2$	F2	DIN3	F4	J11	AUXOUT2	$V_{CC}/2$	L10	AUXOUT7	$V_{CC}/2$
B10	CASOUT7	$V_{CC}/2$	F3	DIN2	F3	K1	DREF2	F6	L11	AUXOUT5	$V_{CC}/2$

NOTES:

10. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
11. 47kΩ (±20%) resistor connected to all pins except V_{CC} and GND.
12. V_{CC} = 5.5 ± 0.5V.
13. 0.1µF (min) capacitor between V_{CC} and GND per position.
14. FO = 100kHz ± 10%, F1 = F0/2, F2 = F1/2 . . . F11 = F10/2, 40 - 60% Duty Cycle.
15. Input Voltage Limits: V_{IL} = 0.8V max, V_{IH} = 4.5 ± 10%.

Metal Topology

DIE DIMENSIONS:
254 mils x 214 mils x 19 ± 1 mil

METALLIZATION:
Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
0.96×10^5 A/cm^2