HDMI Receiver IP Core DVD Mobile Digital TV Imaging

Product Brief

Zoran Corporation 1390 Kifer Road Sunnyvale, CA 94086-5305 Tel 408.523.6500 Fax 408.523.6501 www.zoran.com



IP Cores

Benefits Overview

Zoran's HDM-R1 is a silicon efficient, cost effective intellectual property core for IC designs requiring the HDMI Receive function. The HDM-R1 decodes the HDMI standard into high definition digital video formats (YCbCr or RGB) and multi-channel audio. High Definition

Content Protection (HDCP) decryption is supported. HDM-R1 includes digital link, analog Phy and reference software to provide a complete solution for the HDMI Receive function. HDM-R1 is proven in silicon.

Features

- · HDMI version 1.1 compliant
- · HDCP version 1.1 compliant
- Supports EIA/CEA 861b video formats including 480i, 480p, 576i, 576p, 720p, 1080i, and up to 1360 x 768
- Up to 8 channels uncompressed LPCM audio up to 192 kHz
- Pass through for compressed audio including Dolby Digital, MPEG-2, MP-3, etc.MPEG-2, MP-3, etc.
- · HDCP authentication and link verification

- · Audio clock regeneration
- · Video format detection
- · Color space conversion
- · Audio mute
- · Internal color bar & square wave generators
- · Generic Host Bus Interface for core configuration and control
- · Onboard debug and test support

Digital Link and Analog PHY Solution

HDM-R1 is a complete solution including the digital link layer and analog Phy. Initially targeted to a TSMC 0.18 micron process, HDM-R1 can be ported to other popular processes.

Reference Software

The HDM-R1 IP Core includes reference software which facilitates the implementation, verification and validation of the core. It can also be used as an example for further software system development. Provided as source code, the reference software is highly portable and can easily be adapted to any specific system.

The reference software consists of the following functions:

- · Hardware configuration and system interface
- Authentication

Integrated Circuit Applications

- · LCD Display Processors
- Digital TVs
- · Set-top boxes

- · DVD recorders
- A/V Receivers
- · Any IC requiring the HDMI receive function

Deliverables

Digital Link

- · Synthesizable RTL code (Verilog)
- · Bit accurate C model
- · Synopsis synthesis scripts
- · Test bench with suite of test cases

Analog Phy

- GDS2
- · CDL Netlist for LVS/DRC
- Verilog behavioural model (without timing)
- · Synopsys .lib model
- · Cadence .lef file (for integration and top level Place and Route).
- Cadence .tlf file (timing information for top level place and route)
- · Layout recommendations/guidelines
- · Package/PCB design recommendations

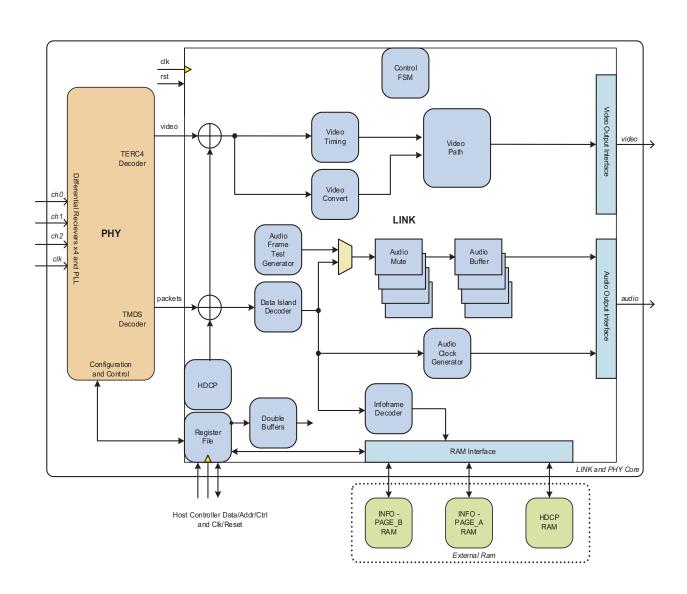
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HDM-R1 Block Diagram



For more information, contact Zoran's Sunnyvale office or the office nearest you:

Shanghai, China	Shenzhen, China	Hong Kong	Israel	Japan	Korea	Taiwan
Zoran China Office	Zoran China Office	Zoran Asia Pacific Ltd.	Zoran Microelectronics Ltd.	Zoran Japan Office	Zoran Korea Office	Zoran Taiwan Office
Tel: 86-21-6469-9799	Tel: 86-755-8281-5777	Tel: +852-2620-5838	Tel: +972-4-8545-777	Tel: +81-3-5475-1051	Tel: +82-2-761-7471	Tel: +886-2-2659-9797
Fax: 86-21-6427-0545	Fax: 86-755-8322-0889	Fax: +852-2620-5238	Fax: +972-4-8551-550	Fax: +81-3-5475-1053	Fax: +82-2-761-7472	Fax: +886-2-2659-9595

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