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# HD74LVC2244A

Octal Buffers / Line Drivers with 3-state Outputs

## HITACHI

ADE-205-234 (Z)  
Preliminary  
1st. Edition  
December 1998

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### Description

The HD74LVC2244A has eight line drivers with three state outputs in a 20 pin package. This device is a noninverting buffer and has two active low enables ( $\overline{1G}$  and  $\overline{2G}$ ). Each enable independently controls four buffers.

All outputs, which are designed to sink up to 12 mA, include equivalent 26  $\Omega$  resistors to reduce overshoot and undershoot.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high impedance state during power up or power down.

Low voltage and high speed operation is suitable at battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 1.65$  to 5.5 V
- All inputs  $V_{IH}(\text{Max}) = 5.5$  V (@ $V_{CC} = 0$  to 5.5 V)
- All outputs  $V_O(\text{Max}) = 5.5$  V (@ $V_{CC} = 0$  V or output off state)
- Typical  $V_{OL}$  ground bounce < 0.8 V (@ $V_{CC} = 3.3$  V,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot > 2.0 V (@ $V_{CC} = 3.3$  V,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 12$  mA (@ $V_{CC} = 3.0$  to 5.5 V)
- All outputs have equivalent 26  $\Omega$  series resistors, so no external resistors are required

# HD74LVC2244A

## Function Table

Inputs		Output Y
$\overline{G}$	A	Z
H	X	Z
L	H	H
L	L	L

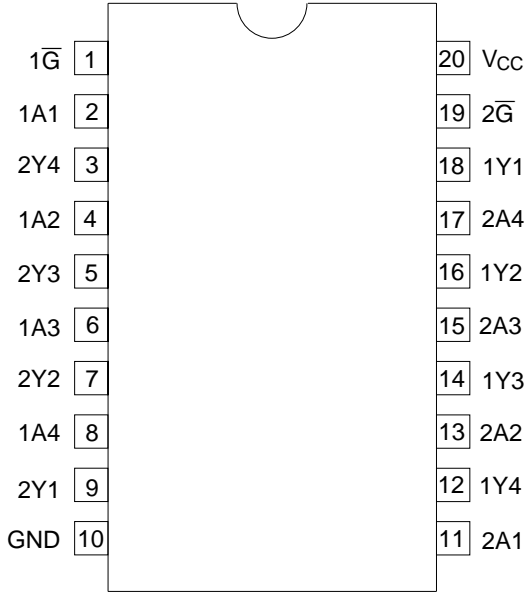
H : High level

L : Low level

X : Immaterial

Z : High impedance

## Pin Arrangement



(Top view)

**Absolute Maximum Ratings**

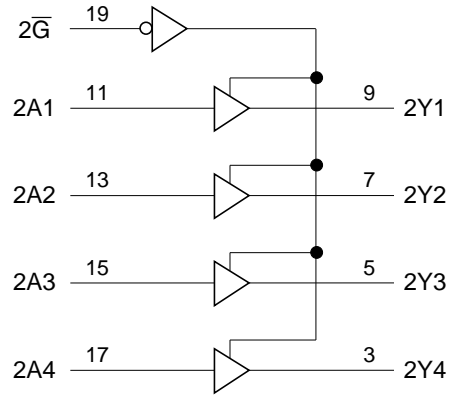
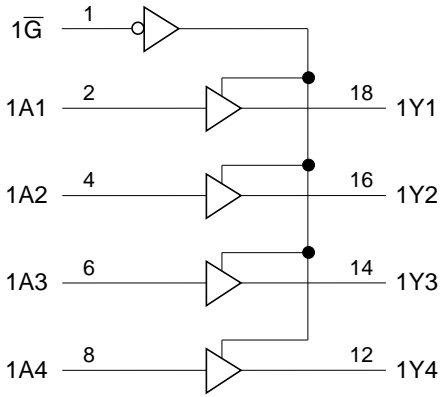
Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 7.0	V	
Input voltage	$V_I$	-0.5 to 7.0	V	
Output voltage	$V_O$	-0.5 to 7.0 -0.5 to $V_{CC}+0.5$	V	Output "Z" or $V_{CC}$ : OFF Output "H" or "L"
Input diode current	$I_{IK}$	-50	mA	$V_I < 0$
Output diode current	$I_{OK}$	-50	mA	$V_O < 0$
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Storage temperature	Tstg	-65 to 150	°C	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

**Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	1.65 to 5.5 1.5 to 5.5	V	At operation Data retention only
Input voltage	$V_I$	0 to 5.5	V	
Output voltage	$V_O$	0 to 5.5 0 to $V_{CC}$	V	Output "Z" or $V_{CC}$ : OFF Output "H" or "L"
Output current	$I_{OH}$	-2 -4 -8 -12	mA	$V_{CC} = 1.65$ V $V_{CC} = 2.3$ V $V_{CC} = 2.7$ V $V_{CC} = 3.0$ to 5.5 V
	$I_{OL}$	2 4 8 12		$V_{CC} = 1.65$ V $V_{CC} = 2.3$ V $V_{CC} = 2.7$ V $V_{CC} = 3.0$ to 5.5 V
Input rise / fall time	$t_r, t_f$	0 to 6	ns / V	
Operating temperature	Ta	-40 to +85	°C	

**Logic Diagram**





## Switching Characteristics (Ta = -40 to 85°C)

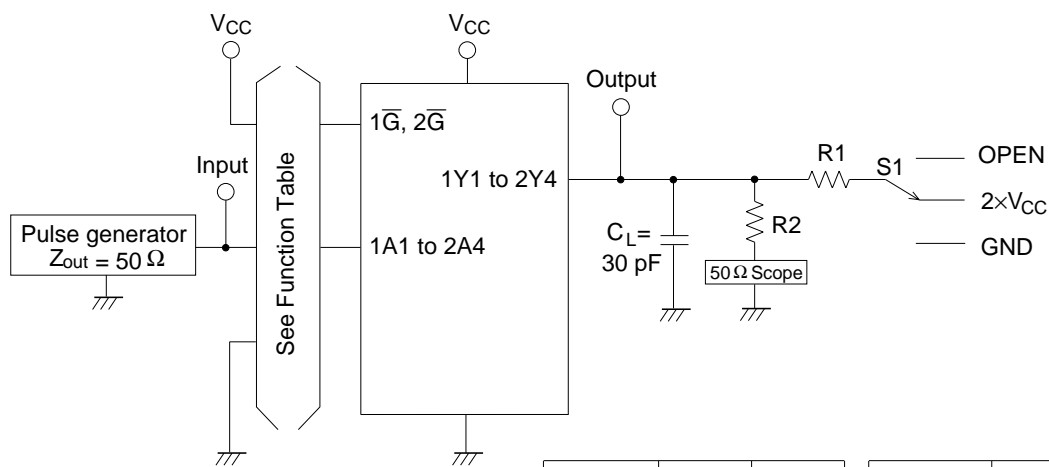
Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Propagation delay time	t <sub>PLH</sub>	1.8±0.15	TBD	TBD	TBD	ns	A	Y
	t <sub>PHL</sub>	2.5±0.2	TBD	TBD	TBD			
		2.7	—	—	6.4			
		3.3±0.3	1.5	—	5.5			
		5.0±0.5	—	—	4.1			
Output enable time	t <sub>ZH</sub>	1.8±0.15	TBD	TBD	TBD	ns	$\bar{G}$	Y
	t <sub>ZL</sub>	2.5±0.2	TBD	TBD	TBD			
		2.7	—	—	8.1			
		3.3±0.3	1.0	—	7.1			
		5.0±0.5	—	—	5.6			
Output disable time	t <sub>HZ</sub>	1.8±0.15	TBD	TBD	TBD	ns	$\bar{G}$	Y
	t <sub>LZ</sub>	2.5±0.2	TBD	TBD	TBD			
		2.7	—	—	7.3			
		3.3±0.3	1.5	—	6.8			
		5.0±0.5	—	—	5.7			
Between output pin skew <sup>1</sup>	t <sub>OSLH</sub>	1.8±0.15	TBD	TBD	TBD	ns		
	t <sub>OSHL</sub>	2.5±0.2	TBD	TBD	TBD			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			

Note : 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

**Test Circuit**

( $V_{CC} = 1.8 \pm 0.15 \text{ V}$ ,  $V_{CC} = 2.5 \pm 0.2 \text{ V}$ )



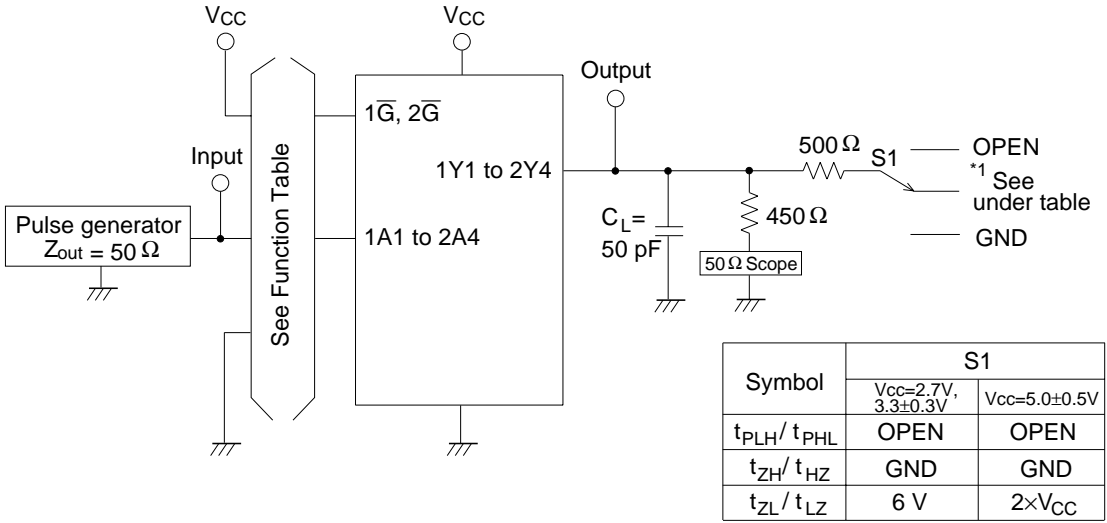
$V_{CC}$ (V)	R1	R2
$1.8 \pm 0.15$	1 k $\Omega$	950 $\Omega$
$2.5 \pm 0.2$	500 $\Omega$	450 $\Omega$

Symbol	S1
$t_{PLH} / t_{PHL}$	OPEN
$t_{ZH} / t_{HZ}$	GND
$t_{ZL} / t_{LZ}$	$2 \times V_{CC}$

Note: 1.  $C_L$  includes probe and jig capacitance.

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( $V_{CC} = 2.7\text{ V}$ ,  $V_{CC} = 3.3 \pm 0.3\text{ V}$ ,  $V_{CC} = 5.0 \pm 0.5\text{ V}$ )

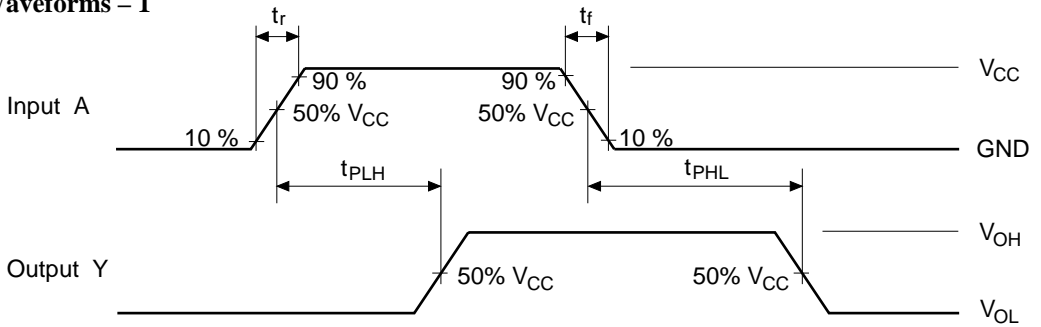


Note: 1.  $C_L$  includes probe and jig capacitance.

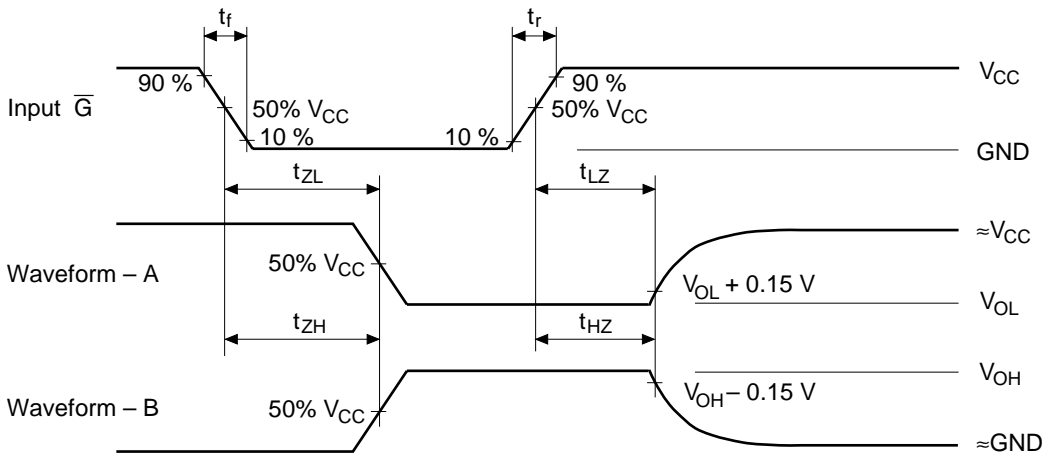


( $V_{CC} = 1.8 \pm 0.15 \text{ V}$ ,  $V_{CC} = 2.5 \pm 0.2 \text{ V}$ )

• Waveforms – 1



• Waveforms – 2

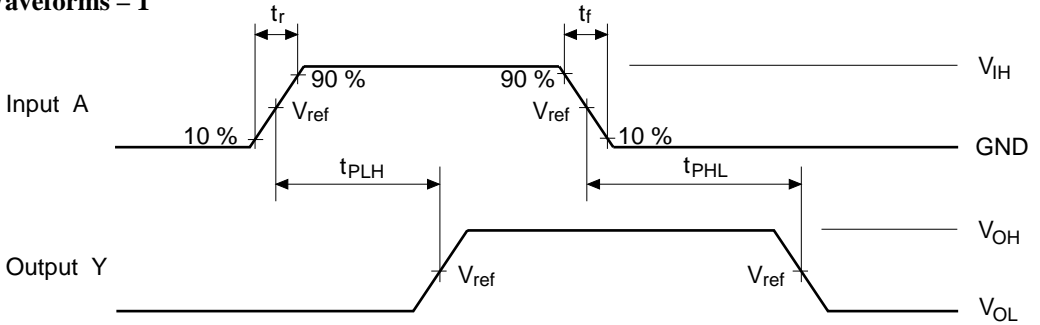


- Notes:
1. Input waveform : PRR = 10 MHz, duty cycle 50%,  $t_r = 2.0 \text{ ns}$ ,  $t_f = 2.0 \text{ ns}$
  2. Waveform – A shows input conditions such that the output is “L” level when enabled by the output control.
  3. Waveform – B shows input conditions such that the output is “H” level when enabled by the output control.

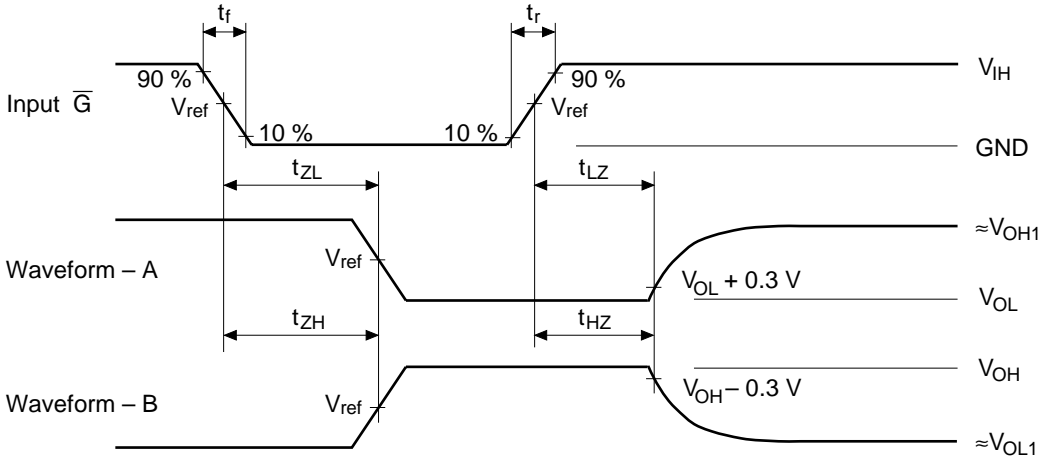
# HD74LVC2244A

( $V_{CC} = 2.7\text{ V}$ ,  $V_{CC} = 3.3 \pm 0.3\text{ V}$ ,  $V_{CC} = 5.0 \pm 0.5\text{ V}$ )

## • Waveforms – 1



## • Waveforms – 2

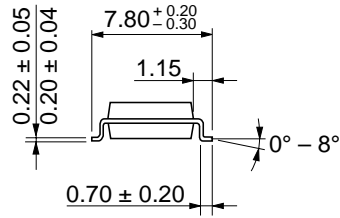
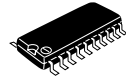
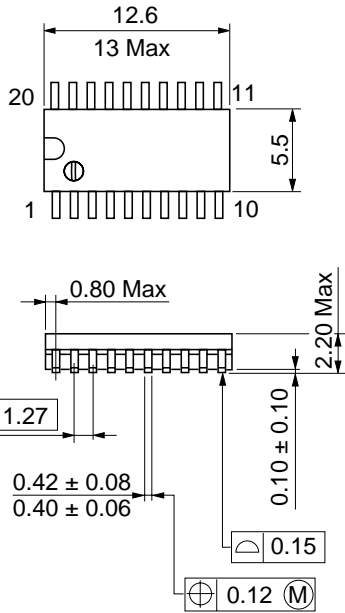


TEST	$V_{CC}=2.7\text{V}$ , $3.3 \pm 0.3\text{V}$	$V_{CC}=5.0 \pm 0.5\text{V}$
$V_{IH}$	2.7 V	$V_{CC}$
$V_{ref}$	1.5 V	50% $V_{CC}$
$V_{OH1}$	3 V	$V_{CC}$
$V_{OL1}$	GND	GND

- Notes:
1. Input waveform : PRR = 10 MHz, duty cycle 50%,  $t_r = 2.5\text{ ns}$ ,  $t_f = 2.5\text{ ns}$
  2. Waveform – A shows input conditions such that the output is “L” level when enabled by the output control.
  3. Waveform – B shows input conditions such that the output is “H” level when enabled by the output control.

Package Dimensions

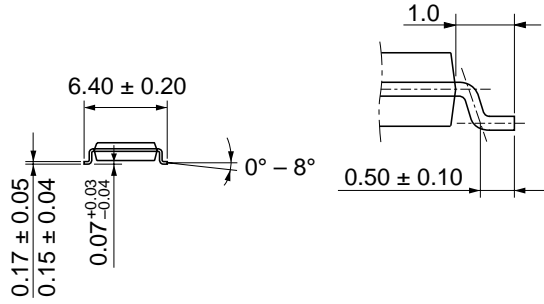
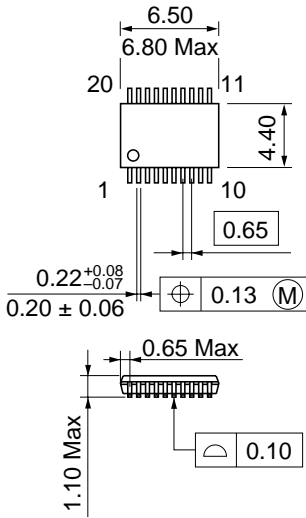
Unit : mm



Dimension including the plating thickness  
Base material dimension

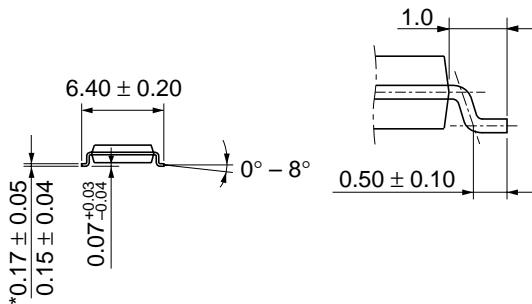
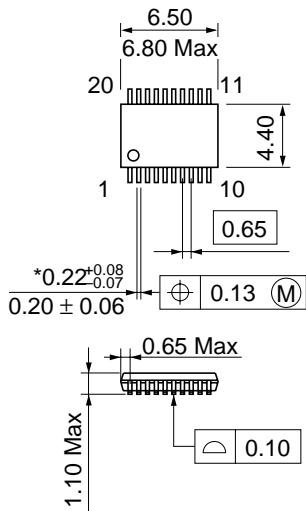
Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

# HD74LVC2244A



Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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